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Reliable selection of hot-swap FETs

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ABSTRACT

Hot Swapping causes a sudden change in the loading conditions of the system which in turn affects the current drawn. Hot Swap circuits which are used to protect the end equipment employ an external FET which must survive the sudden stress generated from the inrush current. Selection of MOSFET for a hot swap application is a highly iterative and time-consuming process. This report gives an overview of the concepts and calculations that need to be considered to decide the right MOSFET for the application.

Keywords*: MOSFET, SOA margin, Hot Swap, Start-up, Inrush current.*

1. INTRODUCTION

Hot swapping refers to addition or replacement of components to a system without stopping it or shutting it down. This causes a sudden change in the loading condition and hence, the current drawn. The sudden change in current may affect the other components of the system, leading to equipment failure or even permanent damage.

A Hot Swap circuit is specially designed to protect the end equipment from high inrush currents generated from fault conditions. It employs an external MOSFET to act as a pass switch. The MOSFET gate is controlled to turn off if the controller senses a current level across a calculated threshold. It is placed on the input of a plug-in card to manage inrush current and to protect the main bus and the load during faults. In addition to providing inrush current control, some hot swap controllers also provide undervoltage and overvoltage lockout settings.

The figure below shows a typical hot swap application schematic for LM25066 hot swap controller from Texas Instruments. This controller is commonly used for 12V applications and supports undervoltage lockout, overvoltage lockout and power good settings in addition to inrush current control.

The current limit threshold is set by a sense resistor, R_{SNS}, connected across the voltage sensing pins of the hot swap controller. A resistive divider can be used to tune the sense resistance. To sense the over-current, a minimum voltage difference must be observed across the sense resistor. Hence, in high current applications, a low sense resistor is better as it dissipates less power. The external MOSFET should operate in its safe operating area during the entire fault duration for a robust design. To do so, the MOSFET should have a minimum recommended SOA margin. Accurate calculations of power dissipation, junction temperature and SOA margin are necessary to ensure that the MOSFET survives the fault conditions.

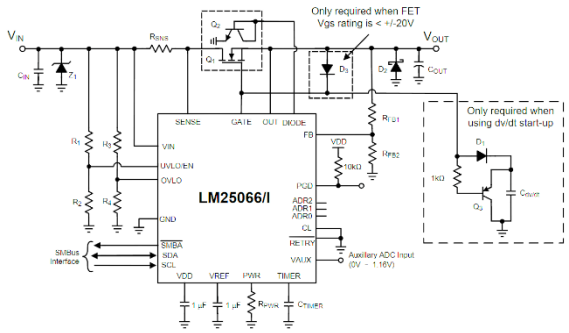

Fig. 1: Hot Swap application schematic with LM25066 Hot Swap controller

2. KEY FAULT SCENARIOS IN HOT SWAPS

There are three key fault scenarios in Hot Swaps viz., start-up, start-up-into-short and hot-short. During a fault condition, the hot swap controller regulates the gate voltage of the MOSFET to control the power dissipation until the timer expires. At low V_{DS}, the controller regulates the current to be held below the current limit value, $I_{LIM,CL}$. As V_{DS} increases, the hot swap controller shifts to regulating the power dissipation to be maintained below the power limit P_{LIM} across the MOSFET until the timer expires and then turns it off. The limiting current I_{LIM} through the MOSFET can be given by the following equation:

$$I_{LIM} = MIN\left(I_{LIM,CL}, \frac{P_{LIM}}{V_{DS}}\right) \quad (1)$$

To avoid error due to offsets, a minimum sense voltage must be observed across the sense resistor R_{SNS} for proper functioning of the circuit. This value depends on the power limit and current limit settings and is computed using the formula below:

$$V_{SNS,PL,MIN} = \frac{P_{LIM} \times V_{SNS,CL}}{V_{DS,MAX} \times I_{LIM,CL}} \qquad (2)$$

In start-up with only power limit, for a purely capacitive load, the timer duration depends on the input voltage, current and power limit values and the output capacitance and is given by the following equation:

$$T_{START} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2}\right] \qquad (3)$$

As the output capacitance gets charged up, the inrush current increases as the \$V_{OUT}\$ increases, because V_{DS} of the MOSFET will decrease. The stress on the MOSFET is roughly P_{LIM} watts for T_{START} milliseconds. Power Limit start-up is usually preferred in designs with low output capacitance, as the charging time is lower with low capacitance.

In start-up-into-short and hot-short, output is at 0 V and entire input voltage appears across the MOSFET ($V_{DS} = V_{IN}, V_{OUT} = 0$), leading to minimal current drawn, $\left(I_{LIM} = \frac{P_{LIM}}{V_{DS}}\right)$. Hence, start-up-into-short and hot-short have longer timer duration, T_{TIMER}, since low current takes longer time to charge the output capacitance. The timer duration, T_{TIMER} and electrical stress of P_{LIM} watts for T_{TIMER} duration is same for both start-up-into-short and hot-short. However, hot-short scenario is the most stressful case of the three, since the MOSFET is hotter due to initial load current flow.

3. SOA CONSIDERATIONS

MOSFET SOA curve is used to determine whether the selected MOSFET can survive the fault conditions or not. The margin calculations need to be done keeping hot-short scenario in mind, to get accurate results. An SOA margin of at least 30\% is usually recommended to ensure the MOSFET survives any unexpected transients. A MOSFET with higher SOA margin may easily survive the fault condition, however the hot swap solution may not be economical.

The figure below is the datasheet SOA for CSD19536KTT from Texas Instruments. A typical SOA graph shows the maximum power than can be handled by the MOSFET for a particular pulse duration.

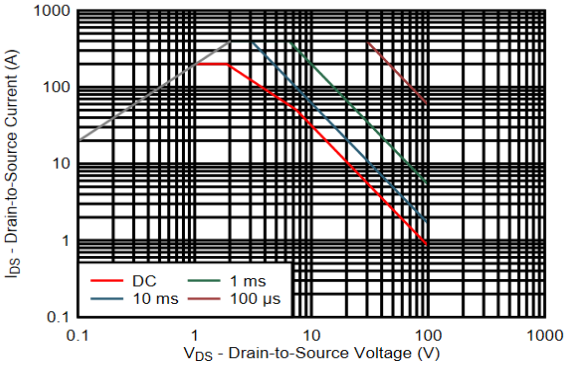

Fig. 2: Datasheet SOA for CSD19536KTT

Usually, transient events occur for an arbitrary duration, while MOSFET datasheets provide SOA data for specific pulse durations only as shown in the figure above. Accurate estimation of power dissipation at the arbitrary duration through mathematical models is necessary to get the correct margin at the pulse duration. A logarithmic model can be used if there are at least two test data points available. Below is an example plot for SOA vs. time for PSMN4R8-100BSE MOSFET from Nexperia.

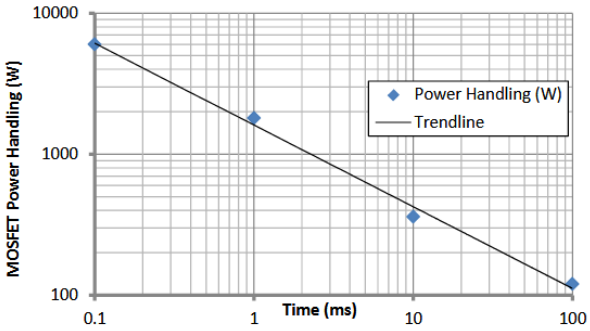

Fig. 3: SOA vs. time for $V_{DS} = 60V$ (PSMN4R8-100BSE)

Considering any two data points from a similar graph, the logarithmic model can be applied. For pulse duration t_1 and t_2, the logarithmic model is given by the equations below. The coefficients 'a' and 'm' can be computed using the two data points.

$$SOA(t) = a \times t^m$$

$$m = \frac{ln[SOA(t_1)/SOA(t_2)]}{ln[t_1/t_2]} \; ; \; a = \frac{SOA(t_1)}{t_1^m} \qquad (4)$$

In addition to having an arbitrary duration, a transient pulse may not necessarily be a square pulse. In such case, the transient waveform must be converted into its equivalent square waveform to compare it on the MOSFET SOA curve, before proceeding to estimate the power dissipation at the arbitrary duration.

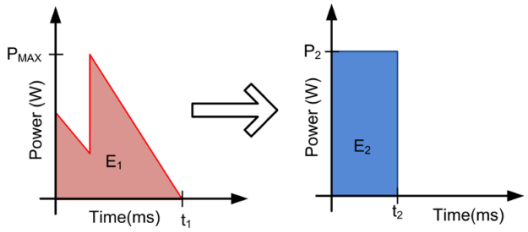

Fig. 4: Approximating FET stress for non-square pulse

$$E_2 = E_1 = \int_o^{t_1} P(t)dt \; ; \; P_2 = P_{MAX}$$
$$t_2 = E_2/P_2 \qquad (5)$$

The equivalent square pulse is computed as having the same energy. From the figure, the MOSFET can handle more energy if it is spread over a longer time. This approach is conservative as the energy handled by the MOSFET is equal however, it is applied over a shorter duration.

A simplified thermal model for MOSFET for Hot Swap design is as shown in the following figure. Where, T_J represents the junction temperature, T_C is the case temperature, T_A is the ambient temperature, C_J is the thermal capacitance of the junction, C_C is the thermal capacitance of the FET and P_{FET} is the power generated on the die.

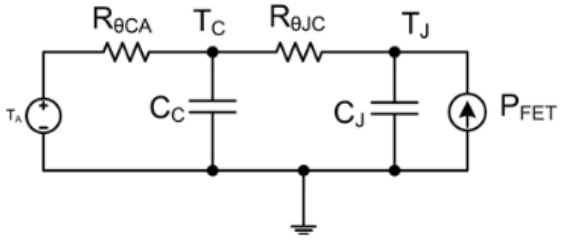

Fig. 5: Simplified MOSFET Thermal Model

When the load current is constant and the FET is fully enhanced, P_{FET} is constant and T_J and T_C are purely a function of $R_{\theta CA}$ and $R_{\theta JC}$. In usual application, T_C will be much hotter than 25°C and hence, needs to be derated.

$R_{\theta CA}$ and $R_{\theta JC}$ are lumped together and called $R_{\theta JA}$ which is the junction to ambient thermal resistance. $R_{\theta CA}$ is a function of layout and $R_{\theta JC}$ is a function of the package. In addition, $R_{\theta JC}$ is typically much lower than $R_{\theta CA}$ MOSFETs with a thermal pad and hence, $R_{\theta CA}$ and $R_{\theta JA}$ are very similar and get used interchangeably. Also, C_C is quite large and thus T_C can be assumed to be constant during transient thermal events such as a hot short.

The stress handling capacity of the MOSFET needs to be properly estimated to ensure it operates in its SOA region. The ON resistance, $R_{DS(ON)}$ of the MOSFET is a function of the junction temperature. Hence, the following equation needs to be solved iteratively until $R_{DS(ON)}$ and T_C converge.

$$T_C = T_A + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DS(ON)}(T_J) \quad (6)$$

Further calculations should be done after converging the junction temperature. High power designs may need more than one MOSFET to be connected in parallel to reduce the junction temperature. In such case, for 'n' MOSFETs connected in parallel, equation (6) becomes:

$$T_C = T_A + R_{\theta CA} \times \left(\frac{I_{LOAD,MAX}}{n}\right)^2 \times R_{DS(ON)}(T_J) \quad (7)$$

Once T_C is known, the SOA can be derated accordingly using the following equation, assuming T_C stays constant during thermal transient.

$$SOA(T_C) = SOA(25°C) \times \frac{T_{J,ABSMAX} - T_C}{T_{J,ABSMAX} - 25°C} \quad (8)$$

During start-up, start-up-into-short or hot-short condition, MOSFETs operate in saturation region (large V_{DS} and V_{GS} close to V_T). In saturation region, current through the MOSFET is a strong function of its $V_{GST} = V_{GS} - V_T$. Hence, threshold voltage mismatch in the paralleled MOSFETs causes a change in the V_{GST} which affects the current drawn, leading to only one MOSFET taking up the entire stress during fault conditions.

At higher temperatures, MOSFET draws more current. With an increase in temperature, the MOSFET starts drawing more current leading to further increase in temperature, creating a positive feedback loop. Each of the paralleled MOSFETs must have an acceptable SOA margin to survive the fault conditions.

Load sharing would take place only when the MOSFETs are fully enhanced. MOSFET ON resistance does not vary more than 25% and shows positive temperature coefficient. If one MOSFET draws more current, it heats up, increasing its ON resistance and in turn balancing the current drawn. This would also keep the junction temperature at a minimal value.

4. SYSTEM STARTUP

Systems with low output capacitance charge up quickly and need a short timer. Most MOSFETs usually survive the fault conditions in such systems. However, for systems with high output capacitance, the charging time is longer and hence need a longer timer. This puts a greater stress on the MOSFET and only a few high power MOSFETs may survive the faults safely. In such case controlling the gate voltage of the MOSFET using a soft start control as shown in the figure below can be done.

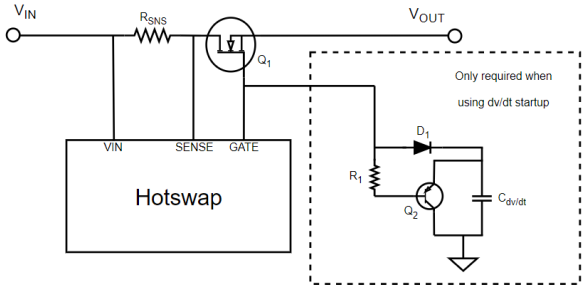

Fig. 6: Circuit to control output dv/dt rate

With Soft start-up control, the timer duration can be programmed and current ramp up can be controlled. This startup mode puts less stress on the MOSFET and makes it easier to survive the fault conditions. With the help of soft start control, the MOSFET will be able to handle the fault conditions, without over-stressing. The limiting current, ramp rate and the capacitance required are related and given by the following equation:

$$I_{LIM,CL} = C_{dv/dt}\left(\frac{dv}{dt}\right) \quad (9)$$

Where $\frac{dv}{dt}$ is the required ramp rate or slew rate and $C_{dv/dt}$ is the required capacitance that needs to be computed for the limiting current $I_{LIM,CL}$. And the fault timer duration can be back calculated using the following equation:

$$T_{FAULT} = \frac{V_{IN}}{\left(\frac{dv}{dt}\right)} \quad (10)$$

Hence, for required fault timer duration, the slew rate can be calculated using the timer duration and input voltage. With the slew rate and the limiting current value, the required soft start capacitance is calculated.

5. CONCLUSION

SOA margin is an important factor which determines whether the MOSFET survives the fault conditions or not. An SOA margin of at least 30% is usually recommended. Transient pulses are usually of an arbitrary duration and waveform and need to be converted into equivalent square pulses before computing the power dissipation. Accurate estimation of power dissipation for the transient duration is necessary to get the best results. The obtained SOA data needs to be derated to the junction temperature before calculating the margin. High power designs may need more than one MOSFET to be connected in parallel. In such cases, it must be ensured that each MOSFET must have an acceptable SOA margin for a robust design. For systems with large output capacitance, soft start-up mode is preferable as it allows the designer to program the timer duration and allows the MOSFET to survive the fault conditions more easily.

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