INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact Factor: 6.078
(Volume 7, Issue 3 - V7I3-1783)
Available online at: https://www.ijariit.com

Different multipliers and a new architecture of multiplier and accumulator based on radix-2 MBA

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ABSTRACT

This Paper consist of detailed review of five multiplier compared with respect to their parameters speed, area, power consumption and circuit complexity namely they are array multiplier, modified booth multiplier, Wallace multiplier and modified booth Wallace multiplier also in this project experimental analysis of Multiplier and Accumulator (MAC) with the help of modified booth Wallace multiplier is proposed to perform the arithmetic operation with high speed, the performance was elevated when two operation multiplication and accumulation was combined and devised with the carry save adder(CSA). Because of the accumulator propagation delay which is largest after merging CSA and MAC it results in improved performance. Radix-2 modified booth algorithm based on 1's complement has been used in proposed CSA design the bit density of multiplier and multiplicand are going to increase by using the modified booth algorithm. To decrease the number of input bits, carries propagates through the LSB of partial products so has to generate the LSB in advance. Pipeline scheme has been introduced in the architecture proposed for MAC in order to accumulate the intermediate result in the form of sum and carry so that the performance of architecture get improved. While keeping the clock frequency same the proposed architecture is twice efficient as of previous design.

Keywords— *Multiplier and Accumulator, Booth Multiplier, Carry save adder, Carry look ahead adder, Digital Signal Processing*

1. INTRODUCTION

In present time world we know how our data processing through various multimedia, communication system, real time processing has advancing in rapid way and increasing in demand. The digital signal processing contains various fundamental elements, but the element matter the most is multiplier and accumulator(MAC) it is sole responsible for the efficient performance of the signal processing it decides how fast the information or data can be transferred. The performance speed is depending upon the arithmetic operation like multiplication and addition but the multiplier has the longest critical path in entire arithmetic operation so propagation delay is decided by multiplier in general.

2. LITERATURE REVIEW

For performing the operation Booth's algorithm is used in the multiplier. Where Booth's ecoder consist of string of full adders or Wallace multiplier. This multiplier on the basis of its functionality can be divided into three parts; Booth Encoder:- For the generation of partial products.

- Wallace Multiplier: For the compression of partial Products.
- Final adder: Forproducing the final result. [1].

Multiplier result has been effectively increased by the significant reduction in the partial products since multiplication function with string of summation of partial products this is where radix-2 based booth encoder introduced for reduction in formation of partial products, the modified booth encoder performs its role mainly with Wallace multiplier to speed up the partial product addition [2]. Elguibaly is the scientist who has designed the MAC with very advanced features in this architecture carry save adder is merged with the accumulation operation for the compression of partial products, Elguibaly pro- posed design work so that the critical path get reduced and the number of inputs for the final adder get decreased[3].Somehow the Elguibaly design has better performance because of reduction in critical path length as if we make a comparison with previously designed MAC but there is necessity to increase the output rate because of use of final adder for accumulation operation[4].A scientist namely Zicari proposed a design of MAC architecture introduced a merging method for the full utilization of 4-2 compressor, he used this compressor for multiplier as a building block[5]. The various kind of multiplier is compared and come with the conclusion of their advantages and disadvantages with respect to the parameter area, circuit complexity, power consumption and delay[6].

3. ARRAY MULTIPLIER

It is a multiplier based on regular structure which we commonly used in basic mathematical operation based on a working process of add and shift, bit multiplication has applied and results in the partial products. This multiplier has the property of partial product outcome are equal to the multiplier bits.

$$
\begin{array}{rrrrrrrr}
 & & & a_3 & a_2 & a_1 & a_0 & \\
 & & \times & b_3 & b_2 & b_1 & b_0 & \\
\hline
 & & & p_{30} & p_{20} & p_{10} & p_{00} & \\
 & & p_{31} & p_{21} & p_{11} & p_{01} & \times & \\
 & p_{32} & p_{22} & p_{12} & p_{02} & \times & \times & \\
p_{33} & p_{23} & p_{13} & p_{03} & \times & \times & \times & \\
\hline
s_7 & s_6 & s_5 & s_4 & s_3 & s_2 & s_1 & s_0
\end{array}
$$

Fig. 1. Array Multiplication

4. WALLACE MULTIPLIER

In this multiplier the multiplication of two digits occurs in a high-speed manner. Wallace multiplier. There are three steps proposed two work with this multiplier method for two number multiplication and they are: in step1 bit by bit products are produce, step2 has product matrix reduced in two row, final outcome is produced in last step where with the help of high-speed adder addition of two resulting rows performed.

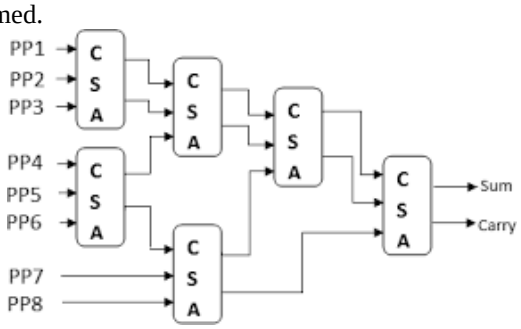

Fig. 2. Wallace Tree Multiplication

5. MODIFIED BOOTH WALLACE MULTIPLIER

This technique has been used in this project, basically when radix-2, radix-4 or radix-8 multiplier bits encoded with booth encoder, there is four basic steps in this method;

- Booth encoder
- PPG (Partial product generator)
- Wallace Multiplier
- CLA (carry look ahead adder)

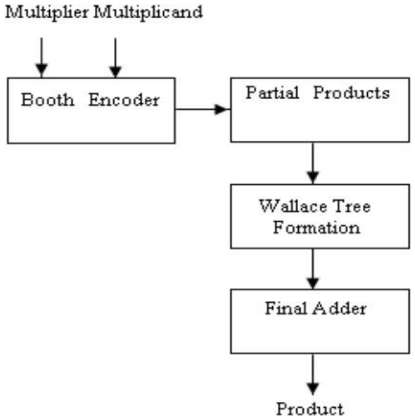

Fig. 3. Wallace Tree Multiplication

6. GDI TECHNIQUE

Gate diffusion input (GDI) technique is the latest and advance method introduced in the architecture for reducing power consumption, area and propagation delay in main block design.

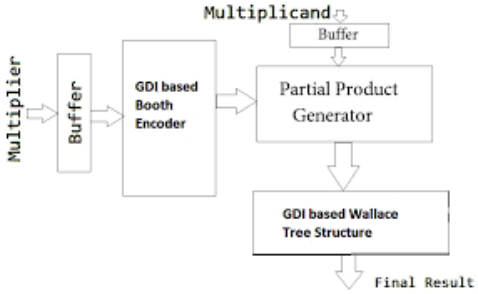

Fig. 4. GDI based booth Wallace architecture

This GDI based multiplier design work in two stages mentioned below;

- GDI Based booth encoder design taken the 1st stage corresponding to which the partial product generator block is attached.
- Partial products are compressed and merged into the next block to give the final result.

In this paper multiplier and accumulator combined with reverse logic function with modified CLA is proposed. CLA function is to control the propagation delay of MAC, the advantage of including reversible logic information or data loss is eliminated during high-speed signal processing.

7. DESIGN FLOW EXPLANATION AND ALGORITHMS

We can understand the design method of the proposed MAC in a way that the multiplier computed with accumulator along with a modified CSA which is controlling the critical path and have contribution towards the fast output result. The architecture has uses the 1's complement based modified booth algorithm and to increase the density of operand used in algorithm sign bit with advance architecture is utilized. To improve the performance of final adder, carry look ahead adder is used with carry save adder tree such that the number of input bits get reduced. Pipelining is introduced to speed up the output and intermediate products are in the form of sum and carry accumulated instead of going to final adder: We can understand the working of the multiplier in a very basic way which is comprises into three steps mentioned below;

- **Step 1:** Operation starts with modified booth encoding based on radix-2 in which multiplier and multiplicand results in partial product.
- **Step 2:** In this step string of adder compresses the partial product and merge them into the sum and carry form.

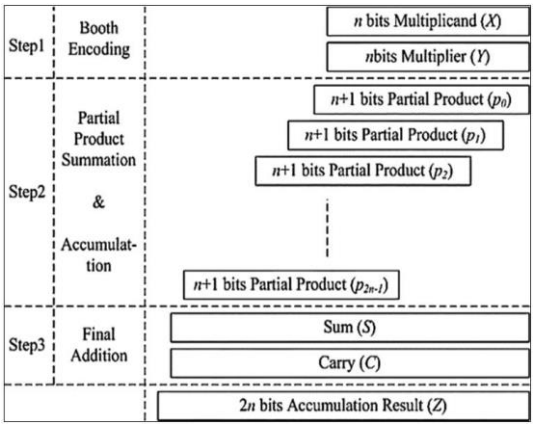

Fig. 5. Advanced Multiplication and Accumulation Operation

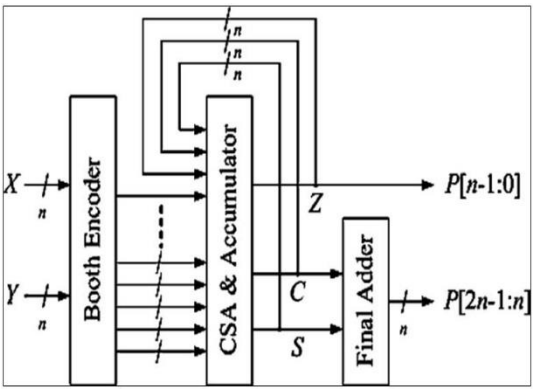

Fig. 6. Hardware Architecture of Proposed MAC

- **Step 3:** Final summation of multiplication result take place with outcome in sum and carry form.

We can say that total operation has a extra step if we consider the accumulation operation explicitly. Basic hardware design is given in the figure 3 which is used in previously discussed method.

8. PROPOSED CARRY SAVE ADDER

When we have to add three or more binary numbers, there is a digital adder which can comprehensively compute this operation is known as carry save adder. It has two or more output number and if we are adding this output together the result of original summation can be obtained. Binary multiplier generally uses the carry save adder, because binary multiplier after the multiplication result includes the summation of greater than two binary numbers. Whichever the big adder framed from the motivation of this technique is faster than the normal adders which we generally use. The Carry Save Adder (CSA) which is combined with the planned design of new MAC (Multiplier-Accumulator) is presented below in the Figure.7 which results in operation of 8×8-bit. Looking to the Figure.7 Sj is computing the sign expansion and converting the 1's complement instruction into 2's complement instruction. The sum and carry of feedback for the jth bit is represented as S[j] and C[j] respectively. Z'[j] previous outcome added in advance with Z[j] which is addition of lower bits of every partial product for jth bit. While Pk[j] is referring to jth bit of kth partial product. Because multiplier i.e., proposed for 8-bit, results in four partial product because of radix-2 method i.e. (P0[7:0] P3[7:0]) from Booth Encoder. As we can see from the given Figure.7 the architecture of CSA for four partial products demands minimum four rows of Full Adders (FAs). Since there is accumulation operation is also so we need one extra row of a full adders that sums up to to total five rows of full adders are required. For computing MAC (multiplier and accumulation) operation of n×n-bit, CSA level is needed of (n/2+1). HA(half adder) and FA(full adder) is represented as gray and white respectively in the given Figure.7. 2-bit carry look ahead adder (CLA) having five inputs with rectangular design is shown in Figure.7. The 2-bit CLA have the responsibility to determine the critical path in carry save adder (CSA). However, it is possible that without the help of carry look ahead adder we can implement the CSA with the help of full adder (FA). We have to take in consideration that partial product lower bits generated previously should processed in advance by carry look ahead adder otherwise the final will be facing the greater number of inputs which is going to degrade the MAC performance.

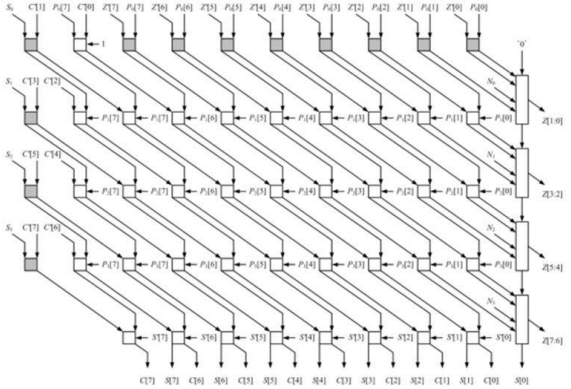

Fig. 7. Proposed CSA Architecture

9. METHOD USED

In this algorithm basically we are encoding the Radix- 2, Radix-4 and Radix-8 multiplier bits with the booth encoder. Hence it named as modified booth encoder. The advantage of modified booth encoder is it eliminated the partial product drastically. Here in this project, we are using Radix-2 modified booth algorithm. Let's understand it in this way, The multiplier has two stages; the first stage consists of booth encoders which drive partial product generators which in turn drive a carry-save addition array to produce two final partial products. In the second stage, the two final products are added to form the final product through a ripple-carry adder. The multiplication architecture is shown in below Figure.

Table I: Partial Product Selection

Operation Multiplicand	Y1	Y0
X*0	0	0
X*1	0	1
$X << 1$	1	0
$X + (X << 1)$	1	1

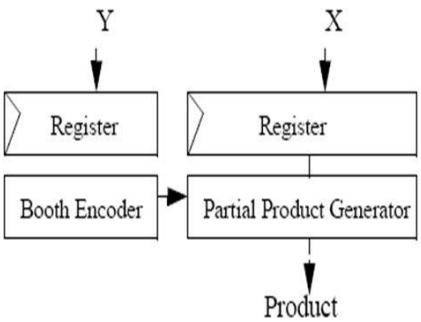

Fig. 8. Multiplication Architecture

9.1 Exp-Normal Multiplication

Here with 4×4-bit normal multiplication four partial product are generated with one position shifting in left direction.

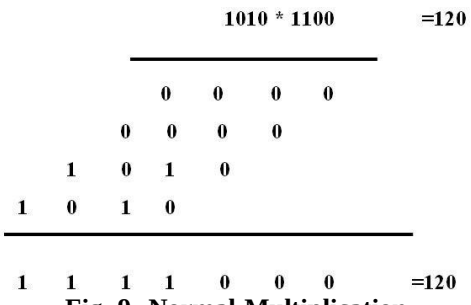

Fig. 9. Normal Multiplication

9.2 Exp- Radix-2 Multiplication

But in Radix-2 modified booth algorithm only two partial product is generated with two postion left shifting addi- tion so we can see the speed is increased by two times.

```
              1010 * 1100                 =120
            ________________
              0    0    0    0            PP1
    1    1    1    1    0                 PP2
  _______________________________
  1    1    1    1    0    0    0         =120
```

Fig. 10. Radix-2 Multiplication

10. RESULT

For MAC a new design is proposed to carry out multiplication and accumulation work which is a very important function in digital signal processing and various communication and real time processing system. So, we learn that by eliminating whole accumulation step which consist the longest critical path and so as propagation delay. By comparing it with previous work its performance elevated almost twice.

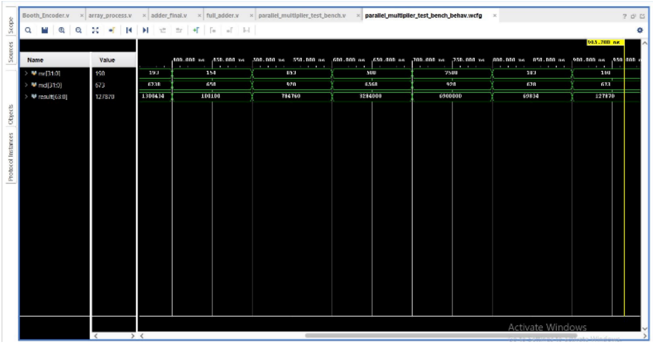

Fig. 11. Result Waveform

11. CONCLUSION

This Paper concluded with the comparison of different multipliers on the parameters of speed, power, area and circuit complexity with each other. This paper also consists the experimental result with taking the multiplier and multiplicand 32-bit each and generating the output result of 64-bit with the help of modified booth Wallace tree multiplier as we can see the simulation result waveform in figure 9. Among the multipliers array multiplier has low speed and less area with simplest circuit design. While the modified booth Wallace multiplier have fastest operation time with moderate power consumption with less area which is highly recommended in digital signal processing application.

Table II: Comparison of Different Multipliers

Multipliers	Speed	Area	Power	Circuit Complexity
Array Multiplier	Low	Small	Most	Simple
Modified Booth Multiplier	High	Medium	Less	Complex
Wallace Tree Multiplier	Higher	Large	More	Medium
Modified Booth Wallace Multiplier	Highest	Largest	More	More Complex

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