INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X

Impact Factor: 6.078

(Volume 7, Issue 3 - V7I3-1781)

Available online at: https://www.ijariit.com

D Flip Flop circuits: Review of different architectures

Nagaraj N.
nagarajn.ec17@rvce.edu.in
RV College of Engineering, Bengaluru, Karnataka

Nithin M.
nithinm@rvce.edu.in
RV College of Engineering, Bengaluru, Karnataka

ABSTRACT

The detailed architectural study of different types of flip flop designs are presented. This includes the conventional transmission gate flip flop topology (TGFF), Sense amplifier-based flip flop architecture (SAFF), Clock pulse-based Flip Flop design and the Dynamic Flip Flop architecture. The fundamental working principles of each topology is discussed along with the operation principles. Important comparisons are made between the architectures and are also presented as a part of this work.

Keywords: *Setup time, Clock-to-Q delay*

1. INTRODUCTION

Flip Flops directly contribute to the constraints on the maximum clock frequency of operation in a given timing path by directly contributing to the delay in the form of Setup time and Clock to Q delay. The other important parameters that characterize a Flip Flop are Power and Area which along with the timing parameters is used to quote the performance of the Flip Flop. Different architectures and modifications have been proposed in literature to improve these three specifications and thus the work presented is an effort to understand and study different types of Flip Flop architectures and their implementations.

2. CONVENTIONAL TGFF

The conventional TGFF uses two latches that operate with complemented clocks in a master slave configuration as shown in the Figure 1. The back-to-back connected inverters is used to store the data through the transmission gate in the feedback during the store half cycle and the forward transmission gate is used to force the data into the latch during the write half cycle. Due to the operation of the latches in opposite clock cycles, the input data is captured at the output Q during the clock edge and the data is stored during the entire clock cycle. The timing diagram for a single transition is shown in the Figure 2. The signals shown include the clock input 'Clk', the data input 'D', the output at the master stage and the output at the slave stage.

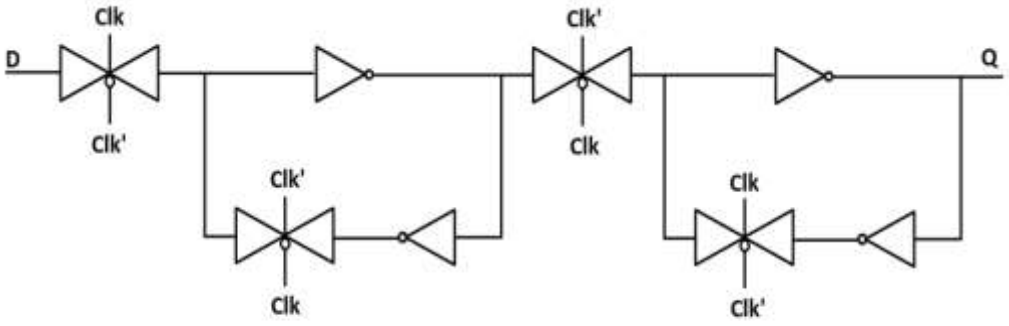

Fig. 1: Conventional TGFF topology

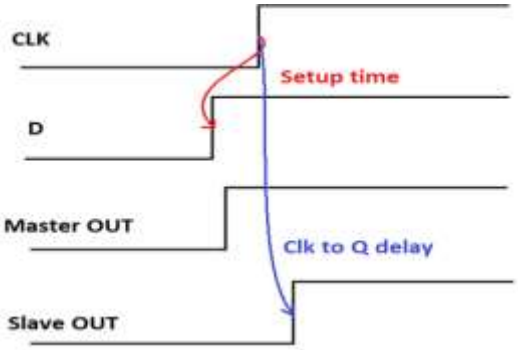

Fig. 2: Timing diagram for TGFF operation

The data input to the flip flop is made stable before the setup time of the flip flop and is immediately captured by the master stage after a certain delay of the master. However, the slave output which is the actual output of the flip flop remains at its previous value. As the clock input transitions from 0 to 1, the slave stage is activated and the data at the master output is captured by the slave after a certain delay which forms the clock-to-Q delay of the Flip Flop. Thus, the slave output captures the data only once during the entire clock period at the clock edge. Major improvements and modifications have been reported in literature from time to time using the master slave topology and few of the recent works have been studied form [1] to [4]. A comparative study of D Flip flops is provided in [5].

3. CLOCK PULSE BASED FLIP FLOP

The Clock pulse-based Flip Flop employs a Clock pulse generator circuit and a Latch stage in series to achieve an edge triggered operation. The Clock pulse generator generates a clock pulse by taking the actual clock input. The complemented delayed version of the clock is generated with the help of odd number of inverters in the chain and is fed to the NAND gate with other input being the actual clock input signal. The NAND generates a complemented clock pulse due to the small delay given by the inverter chain and the actual clock pulse is obtained after another inverter stage. This clock pulse is directly fed to the latch stage. The latch is used to hold the data during the entire clock cycle. Due to the presence of a clock pulse of a very small pulse width, the operation closely resembles the edge triggered operation and hence, operates differently when compared to the other topologies discussed.

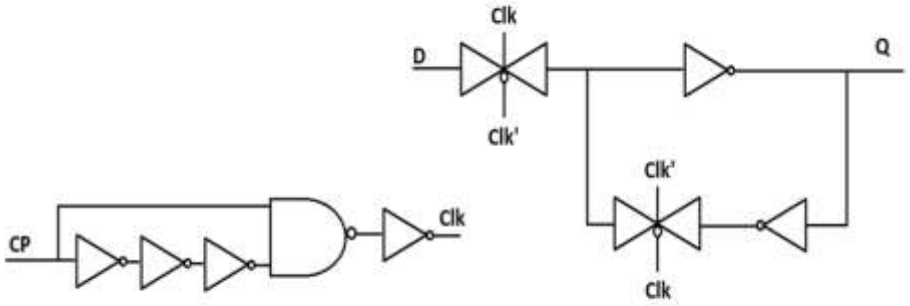

Fig. 3: Clock pulse-based FF architecture

The Figure 4 shows the timing diagram for the clock pulse-based flip flop with the Clock input signal, Data input signal, clock pulse generated and the output signal. Due to the generation of clock pulse and subsequent removal of one of the latches, the flip flop can be operated with zero setup time and sometimes with negative setup time. This proves as a major advantage in comparison to the master slave topology which has a significant amount of setup time. [6] talks about the design and implementation of Clock pulse-based Scan flip flop which can be operated in both the normal mode of operation and scan mode for testing purposes.

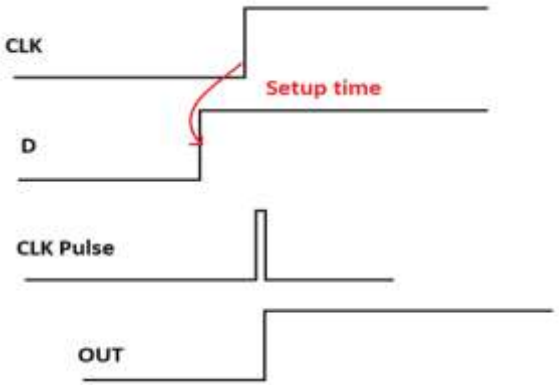

Fig. 4: Timing diagram for Clock pulse FF operation

4. SENSE AMPLIFIER BASED FLIP FLOP

The Sense amplifier-based Flip Flop proves as an alternate topology used to realise the edge triggered flip flop operation. Sense amplifier inputs are fed with the differential Data input signal D and D' which is amplified by the sense amplifier to provide the outputs S' and R'. During the pre-charge phase (Clk = 0), both the outputs of the flip flop S' and R' are charged to VDD and during the evaluation phase (Clk = 1), the S' and R' are evaluated based on the D and D' inputs. This evaluation of the outputs happens only once during the entire evaluation phase right at the clock edge and hence mimics the edge triggered operation. The shorting transistor is used to maintain the values at the output after the clock edge. These outputs are then fed to the latch which stores the data for the entire clock cycle.

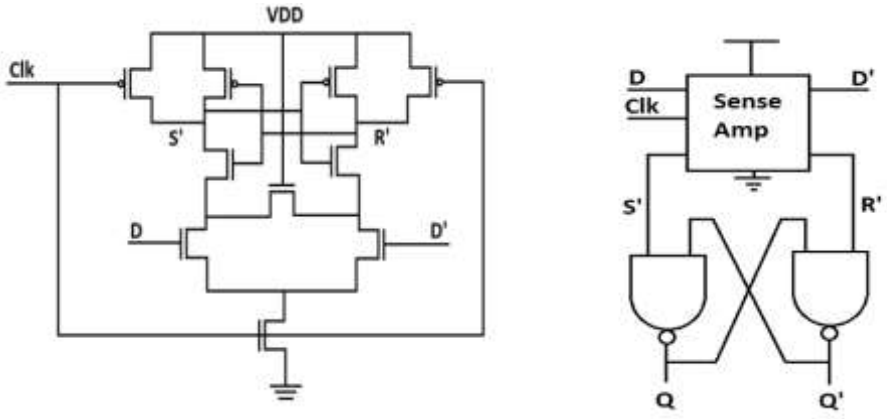

Fig. 5: Sense Amplifier based FF design

Figure 6 shows the timing diagram for the sense amplifier-based flip flop and includes the signals such as the clock input, data input, the S' signal generated and the output Q. During the precharge phase both the intermediate signals S' and R' are pulled to VDD through the PMOS pull up and when switching to the evaluation phase, depending on the D and D' signals, they are pulled down to VSS. The generated signal is then fed to the latch stage to obtain the Q output. This topology is also known for the low setup time requirements and also can be operated with negative setup time. Various modifications have been accomplished to improve the performance of the Sense amplifier-based flip flop. The original NAND gate-based latch topology has been modified and is given in [7], [8], [9] and [10]. The modifications not only provide improvement in the delay, but also offers glitch free operation.

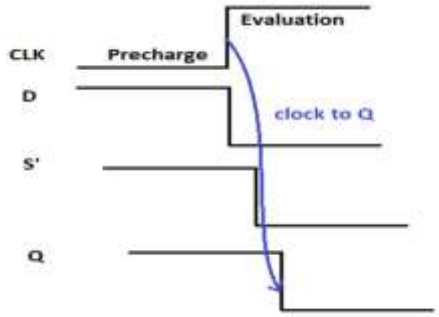

Fig. 6: Timing diagram for Sense Amplifier FF operation

5. DYNAMIC FLIP FLOP

The dynamic class of flip flops are an alternative circuit topology to the static flip flops. The basic difference between the static and dynamic logic is that in dynamic logic, clock signal is used to evaluate the combinational logic. Dynamic logic requires a minimum clock rate that the output state of each dynamic gate is used or refreshed before the charge in the output capacitance leaks out enough to cause the digital state of the output to change, during the part of the clock cycle that the output is not being actively driven. In Figure 7 a basic dynamic version of the flip flop is given. The latch stages used in the previously mentioned topologies or the sense amplifier is not used in this implementation. The gates of the transistors are predominantly controlled by clock input signal and offers for very high-speed operation in certain applications.

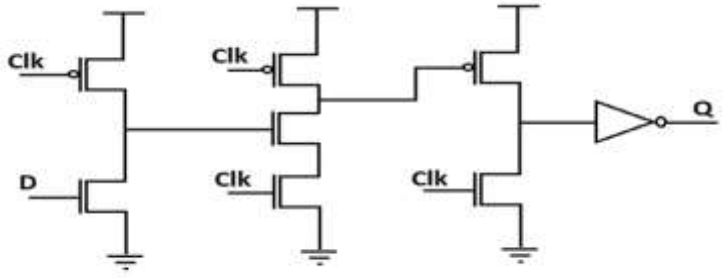

Fig. 7: Dynamic Flip Flop architecture

Figure 8 shows the timing diagram for a single clock transition and the signals included are clock input, data input and the flip flop output. During the precharge phase with Clk = 0, the output of first stage and second stage are pulled to VDD and hence Q shall be floating. When clock input turns to a logic high, the intermediate signals and the corresponding flip flop output is evaluated. Due to the floating nature of the output, a minimum clock frequency is required to not lose the data at the output and hence applies a minimum clock frequency constraint. [11] and [12] explore the dynamic flip flop implementations for high-speed applications.

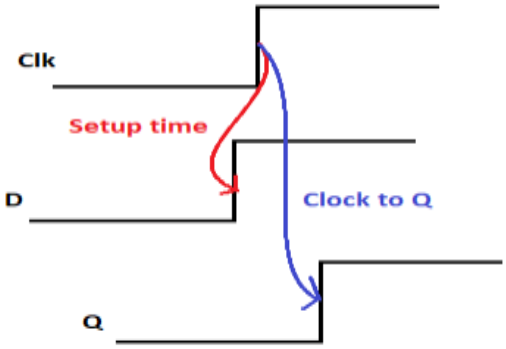

Fig. 8: Timing diagram for Dynamic FF operation

6. CONCLUSION

The study of various Flip Flop architectures is presented along with their basic implementations and principles. The architectures studied were the conventional transmission gate flip flop topology (TGFF), Sense amplifier-based flip flop architecture (SAFF), Clock pulse-based Flip Flop design and the Dynamic Flip Flop architecture. The timing diagram and the associated operating principles were discussed in brief. A set of work from the literature were referred for the important leaps in the implementation and are provided in the references section.

7. REFERENCES

[1] G. Shin, E. Lee, J. Lee, Y. Lee and Y. Lee, "A Static Contention-Free Differential Flip-Flop in 28nm for Low-Voltage, Low-Power Applications," 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA.

[2] Y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell and T. J. Kazmierski, "Ultra-Low Power 18-Transistor Fully Static Contention-Free Single-Phase Clocked Flip-Flop in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 54, no. 2.

[3] V. L. Le, J. Li, A. Chang and T. T. Kim, "A 0.4-V, 0.138-fJ/Cycle Single-Phase-Clocking Redundant-Transition-Free 24T Flip-Flop With Change-Sensing Scheme in 40-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 10.

[4] C. K. Teh, T. Fujita, H. Hara and M. Hamada, "A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40nm CMOS," 2011 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA.

[5] Uming Ko and P. T. Balsara, "High-performance energy-efficient D-flip-flop circuits," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 8, no. 1.

[6] M. -s. Kim et al., "Scan-controlled pulse flip-flops for mobile application processors," 2013 IEEE International Symposium on Circuits and Systems (ISCAS), 2013, pp. 769-772, doi: 10.1109/ISCAS.2013.6571960.

[7] B. Nikolic, V. Stojanovic, V. G. Oklobdzija, Wenyan Jia, J. Chiu and M. Leung, "Sense amplifier-based flip-flop," 1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition (Cat. No.99CH36278), 1999, pp. 282-283, doi: 10.1109/ISSCC.1999.759251.

[8] B. Nikolic and V. G. Oklobdzija, "Design and optimization of sense-amplifier-based flip-flops," Proceedings of the 25th European Solid-State Circuits Conference, 1999, pp. 410-413.

[9] B. Nikolic, V. G. Oklobdzija, V. Stojanovic, Wenyan Jia, James Kar-Shing Chiu and M. Ming-Tak Leung, "Improved sense-amplifier-based flip-flop: design and measurements," in IEEE Journal of Solid-State Circuits, vol. 35, no. 6, pp. 876-884, June 2000, doi: 10.1109/4.845191.

[10] A. G. M. Strollo, D. De Caro, E. Napoli and N. Petra, "A novel high-speed sense-amplifier-based flip-flop," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 11, pp. 1266-1274, Nov. 2005, doi: 10.1109/TVLSI.2005.859586.

[11] Ching-Yuan Yang, Guang-Kaai Dehng, June-Ming Hsu and Shen-Iuan Liu, "New dynamic flip-flops for high-speed dual-modulus prescaler," in IEEE Journal of Solid-State Circuits, vol. 33, no. 10, pp. 1568-1571, Oct. 1998, doi: 10.1109/4.720406.

[12] Byungsoo Chang, Joonbae Park and Wonchan Kim, "A 1.2 GHz CMOS dual-modulus prescaler using new dynamic D-type flip-flops," in IEEE Journal of Solid-State Circuits, vol. 31, no. 5, pp. 749-752, May 1996, doi: 10.1109/4.509860.

