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A direct digital BPSK modulator using an active balun and buffer technology

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ABSTRACT

Earlier there were many circuits which were made using buffer technologies but no such matter exists which implemented five different buffers in any modulation circuit. The whole work is been divided into 3 basic section which is active balun, buffer circuit and the complementary switches. The active balun can have relatively less loss than a passive balun. We preferred active balun in the circuit due to its gain characteristics. In our circuit active balun consists of two MOSFETs with applied in source and drain. The output obtained in the common source FET will have a phase shift of 180° with the input and the output obtained in the common gate will have a phase shift of 0° or multiple of 360° . The input signal was passed to each of the tested buffers and the switching conditions were tested on each of them. CMOS, BiCMOS, FET, common collector and opamp circuits were used for the switching condition and were later added with the active balun for the final result. The main reason for implementing these many signals was to get more accurate and correct results in a shorter period. Based on all the simulations and parameters. In this paper we have further worked on different buffer technologies which were not included in previous works and have got various parameters to compare them and finally conclude which one is better. Also we calculated the rise time and fall time of the buffers to compare the spontaneously they give results. Before plotting the graph and comparing different parameters we have taken different cases and at different input value.

Keywords: Active Balun, Buffer, BiCMOS, FET, Common Collector, OPAMP, CMOS

1. INTRODUCTION

Binary Phase Shift Keying (BPSK) can be termed as a dual-phase modulation technique, in which the 1's and 0's in a digital message signal are depicted by two different phases in the carrier. Applications of Digital BPSK in the telecommunications fields are WPAN, LAN, RFID, bluetooth communication, etc. Earlier many topologies were designed for BPSK modulation. One of the proposed methods for the BPSK modulator was using a lookup table. This architecture was implemented using VHDL. Another BPSK technique was done using a squaring loop algorithm of carrier frequency 8KHz and with a 1kbps transmission rate. For broadband applications, this paper proposes an alternative technique of active balun with proper calibration and switching mechanism. The phase shift properties were shown in the active balun and buffer part of the circuit.

In the first section that is the active balun part, the main idea was to convert the unbalanced circuit to a balanced one so that only two terminals (one for input and one common) are present to increase the stability of the circuit. The message signal and the carrier signal were given as the input in this section on which calibration was performed and result was obtained. The output was obtained in the same way which a XOR signal works. For a better understanding, it can be stated that if both the source are kept on high or both are kept at low, then the output will generate high signal. If either of them is low then the output will be low. The balun circuit is somewhat compared to a converter or inverter functionality. Quite often these technologies are used in the Bluetooth communication field. The buffer circuit was used as an intermediate between balun and switch. It was used for reducing the noise upto a certain limit. The buffer however was the main part which was focused in this paper by changing different techniques and applying different conditions.

2. DESIGN SPECIFICATIONS

2.1 Active balun

Balun comes from 2 words 'Bal' and 'Un'. It acts as an intermediate between the balanced and unbalanced circuits. Here we have connected it to change from unbalanced to balance for improving the noise characteristics. Baluns are used for output generating purposes that have balanced amplitude and phase characteristics. [1] We here preferred active balun in the circuit due to its gain

characteristics and minimal losses. In our circuit active balun consists of two MOSFETs with applied in source and drain. The output we got in the common source MOSFET has a phase shift of 180° with the input and the output obtained in the common gate will have a phase shift of 0° or multiple of 360° . [2] In radio frequency applications, a differential approach is favored, because of its property of strengthening the common-mode disturbances, rejection of unwanted couplings and increased dynamic ranges.

[3] Improved performance can be observed in a dual MOSFET balun which works better in our designed schematic. For carrier signal in the phase, we use a MOSFET with common source configuration, for the 180° phase shift we use a common gate configuration. On the proper calibration of internal resistors, we can obtain equal amplitude measurements at these ends. Simulations were performed to show the above cases which confirms the behavior on different parameters which are shown in this literature. [5] Thus, the active balun circuit gives us sufficient gain parameters and ample bandwidth in a semiconductor circuit. To confirm the parameters, simulations were performed to show the above cases. [4] The output terminal is disposed to couple the output electrodes of the respective ones of the base of transistors. In our circuit, we have given two signals that are message signal and carrier signal, the output will be high if there is no difference between the two signals. If at any instant there are some differences in the signals then the output will be 0.

2.2 Buffer Circuit

A buffer can be termed as an amplifier with nil gain in an IC. We have used buffer as an intermediate between the switch and the balun. Few losses were obtained when the switch is connected with the balun, hence, there is a reduction in the gain parameters. So a buffer was introduced for reduction of losses. Hence a buffer circuit was used to find the input signal supplied is digitally high or digitally low. Apart from this, we can also state that when the buffer output voltage is low then it draws excess of current from VDD which is above the rated. This results in very high impedance which reduces the loss and the effect on the balun part is very less. [2] It provides gain accuracy, low offset value, and low output resistance. But it will hence increase the response time and delay at higher frequencies. The loss obtained is not too small and hence cannot be neglected, which results in the difference in the parameters.

The buffers were fed with the input signal and the switching conditions were tested on them. CMOS, BiCMOS, FET, common collector circuits were used for the switching condition and with the active balun for the final result. [7] The main reason for implementing these many signals was to get more accurate and correct results in a shorter period. Though there are many buffer circuits used earlier as an amplifier, in our case this was not necessary as we have performed impedance matching and gain characteristics by using the buffer as an intermediate between the balun and the output terminal. The losses which occurred during simulation under worst-case conditions and for various impedance matching condition.

2.2.1 CMOS as a Buffer: We all know that a CMOS consists of a PMOS of which the source is connected to VDD and an NMOS whose Drain terminal is connected with the drain of the PMOS and source is connected to VSS or ground. The gate terminal is shorted and the input is taken from that terminal. The buffer circuit which we performed is shown in this literature and simulations are also performed keeping the source voltage as 5V. The output hence obtained is further supplied to the switching circuit which is used as the output in our main circuit.

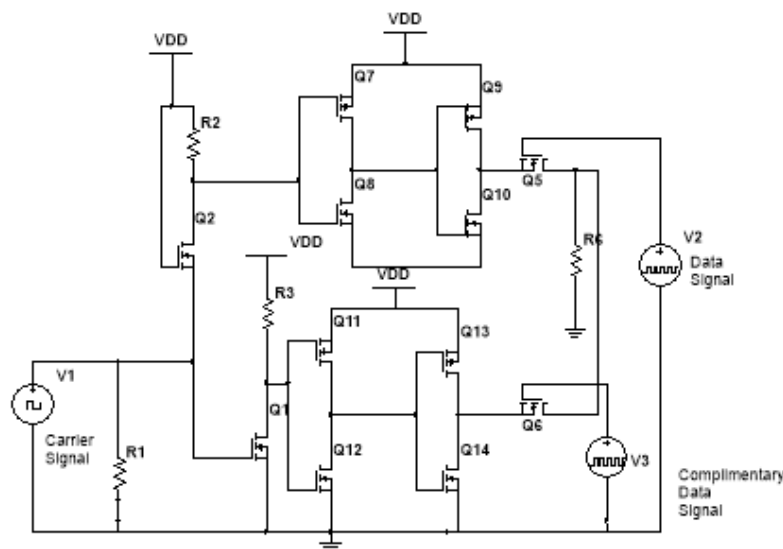


Fig. 1: Design of Buffer using CMOS

Two CMOS are cascaded back to back in the circuit to make a buffer. It inverts the logic level 0 to logic 1 and vice versa. So here for both the switches buffers were implemented so that we can get accurate results in our circuit. The output obtained has a minimal loss compared to other buffers.

2.2.2 Common Collector Buffer: The common collector or emitter follower is used as a voltage buffer in our circuit. In this configuration, the output voltage V_{OUT} is placed contrary and in series with the input voltage V_{IN} . [6] The extraordinary difference is applied to the base-emitter junction. The transistor monitors the voltage and adjusts its emitter voltage continuously almost equal

to the input voltage as it passes the collector current through the given emitter resistor R_E . As a result, the output voltage follows the input voltage variations. hence the name, emitter follower.

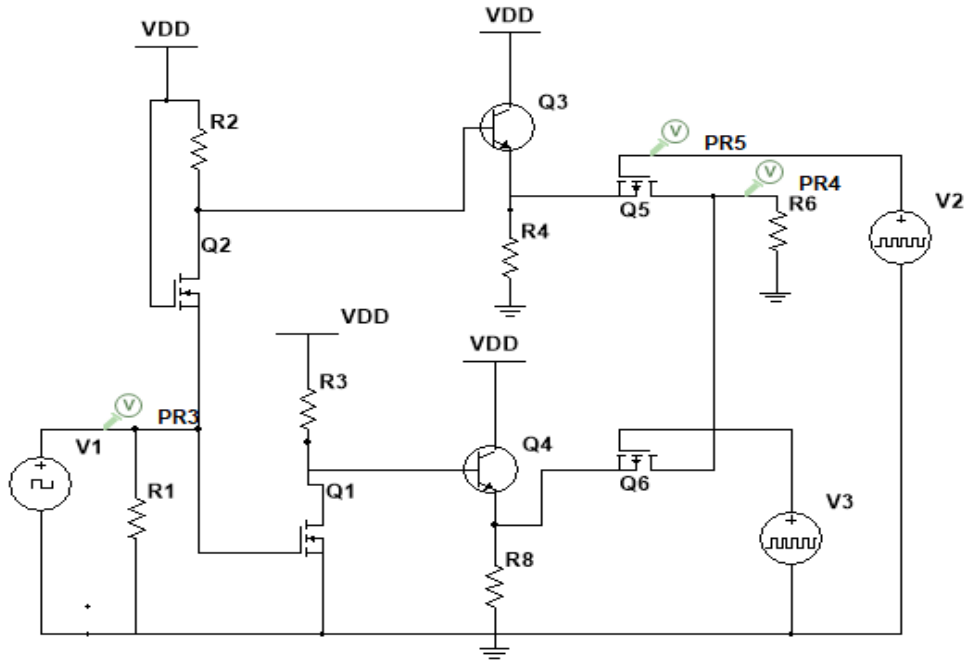


Fig. 2: Design of Buffer in Common Collector Mode

In the emitter follower circuit, we placed two BJT on each switch and the simulation was performed. We observed quite more loss in the circuit. The input impedance was anyhow kept high and output impedance was comparatively low to make it a regular buffer circuit.

2.2.3 OpAmp as a buffer: Negative feedback configuration was used for obtaining our output using the OpAmp circuit. Despite having unity voltage gain, it has high input impedance and low output impedance. [6]The chances of avoiding the loading of source signal can also be performed using this configuration. The issue of impedance matching was reduced to a greater extent in this configuration and the output signal looks like a mirror image of the input signal. The entire simulation draws very less amount of current but there is minimal loss in the output voltage. This result verifies our circuit.

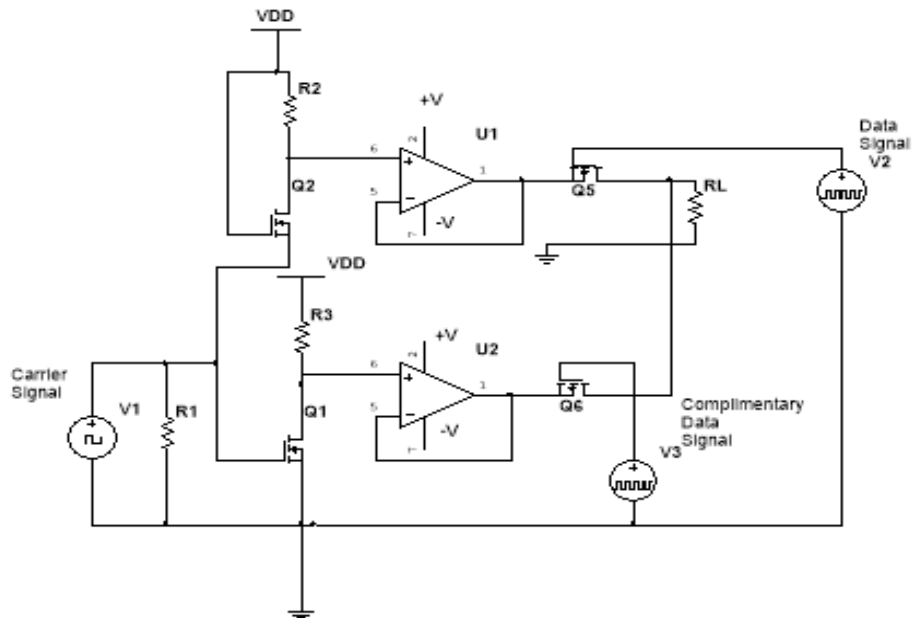


Fig. 3: Design of Buffer using Operational Amplifier

This is one such circuit which is quite commonly used for a buffer as the output gives a mirror image of the input if the impedance and supply voltage are given proper but while taking two signals from input it had few losses.

2.2.4 FET as a buffer circuit: The configuration which is used in our design to obtain the buffer output is a common source and common drain configuration. The buffer amplifying condition is met and the input impedance is kept high whereas the output impedance is kept relatively low. A better level of buffering output is obtained when designed in common source configuration

compared to common drain. The result is verified when the impedance matching state is obtained and hence the entire bpsk modulation is completed.

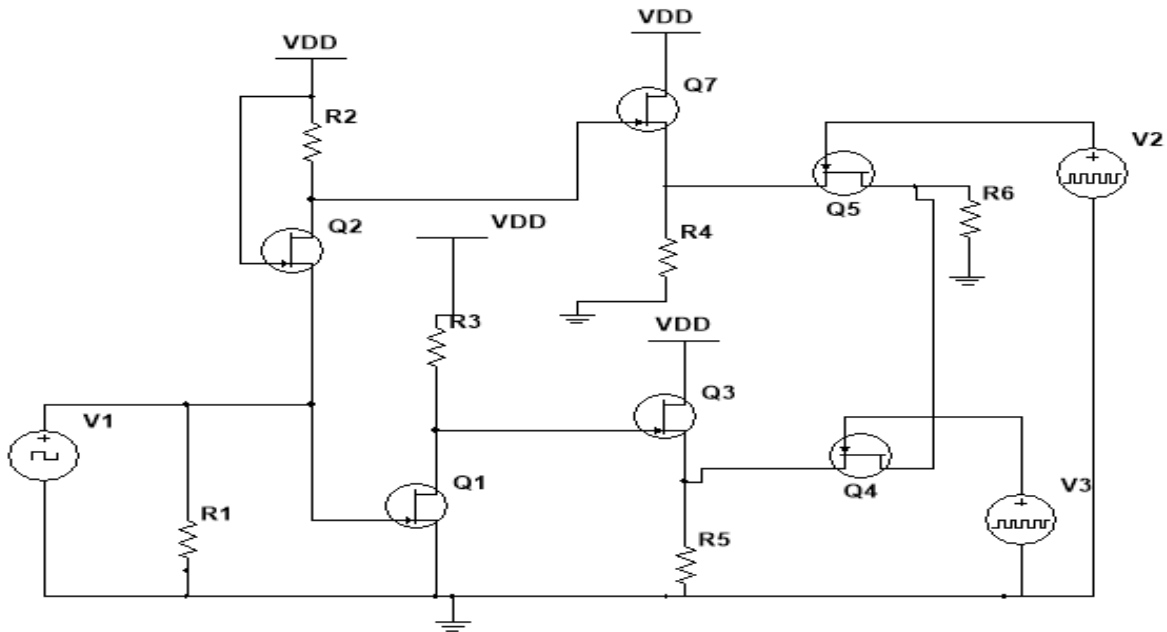


Fig. 4: Design of Buffer using FET

Quite similar to common collector circuit here we used common drain circuit for making the circuit. But the results were better than other circuits as there was less loss and the rise time was also lower than other circuits.

2.2.5 Buffer using BiCMOS: Bipolar CMOS (BiCMOS) is a semiconductor technology that combines two formerly separate semiconductor technologies, those of the bipolar junction transistor and the CMOS gate, in a single circuit device. In our circuit, we used BiCMOS as a buffer and several results were obtained.

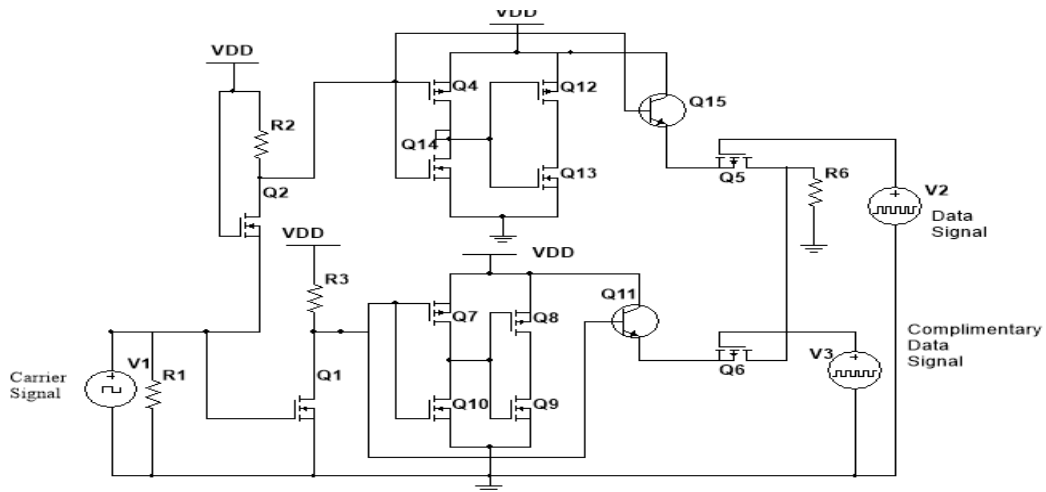


Fig. 5: Design of Buffer using BiCMOS

The BiCMOS buffer was made by cascading 2 nmos and pmos. [7] They have high drive capability also low delay sensitivity to load which makes them a step better than CMOS circuits. But due to the output transistor here in BiCMOS the output obtained has comparatively more losses than CMOS which does not have any transistor.

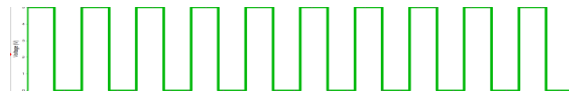
3. RESULT AND DISCUSSION

The following graphs were obtained from all the buffer circuits. The different outputs are shown via different buffers which are given in our literature.

carrier



dat



output via FET buffer



output via CMOS buffer



output via BiCMOS buffer



output via common collector buffer



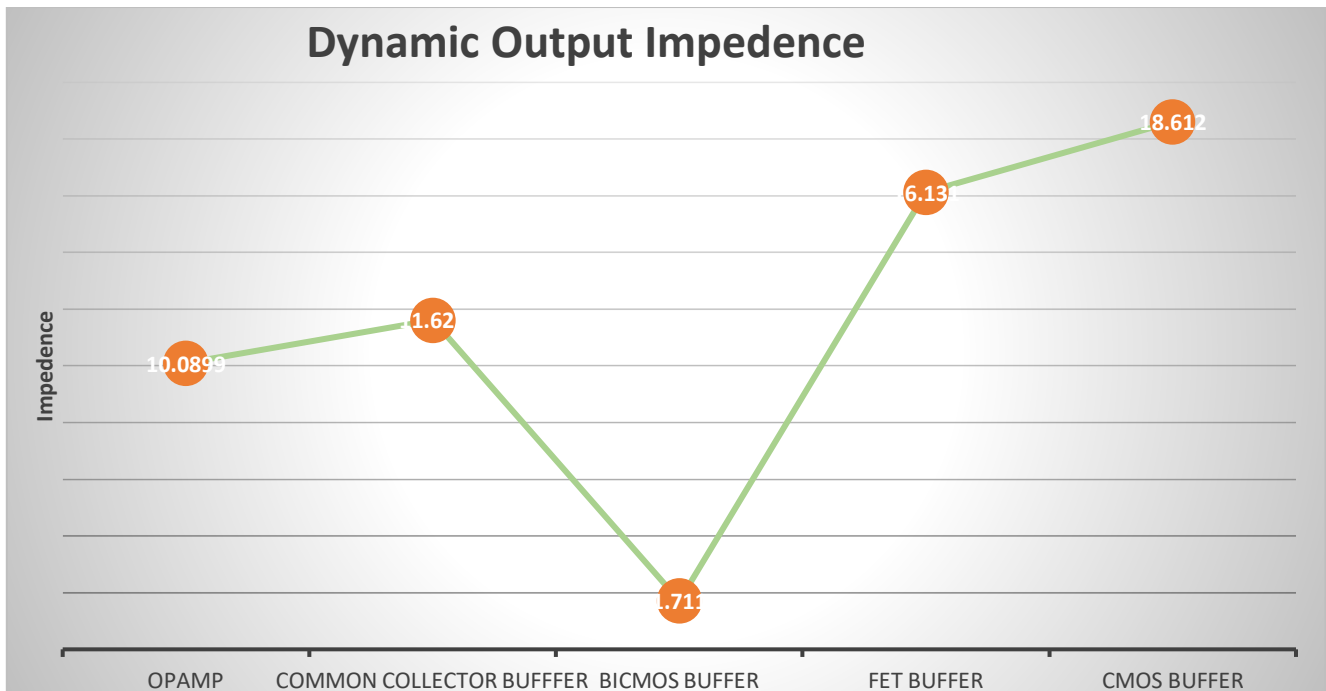
output via opamp buffer



Table 1

Buffers type	Rise Time	Fall Time
FET Buffer	$397 * 10^{-12} \text{s}$	$100 * 10^{-9} \text{s}$
OpAmp	$1 * 10^{-9} \text{s}$	$4 * 10^{-3} \text{s}$
Common Collector Buffer	$1.6 * 10^{-6} \text{s}$	$2.55 * 10^{-6} \text{s}$
BiCMOS Buffer	$3.24 * 10^{-6} \text{s}$	$9.54 * 10^{-6} \text{s}$
CMOS Buffer	$1 * 10^{-9} \text{s}$	$1 * 10^{-9} \text{s}$

Graph 1



The table here gives a description about rise time and fall time of the buffers used here. The time from digital logic 0 to 1 and back to 0 was calculated and the values were compared. It was observed that though the time taken to respond in each of the case is very less but there is a huge difference when we compare them together. On the other hand the graph was plotted which compared the output impedance of all the circuits. The graph here clearly shows the difference in the impedance and how much loss occurred when the signal passes from input signal to the switches through the buffer intermediate.

4. CONCLUSION

After making 5 different technologies of implementing buffer circuit, we get to know that FET was one such circuit which gave us better results than other circuit despite there are minor difference in the results and parameters. Anyhow there are many such parameters which were same for all but our focus was more on noise reduction, response time and impedance matching which gave us a brief idea about the different types and how they are different from each other.

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