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Design of low power and high-performance Carry Save Adder and Ripple Carry Adder using pass transistor logic

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ABSTRACT

Adders are the central structure square of any processor or data way application. For the arrangement of prevalent getting ready units quick adders with low power use is required. To structure viable joined circuits the extent that zone, power additionally, speed has become a troublesome endeavor in present day VLSI design field. In this paper the power and delay modified pass on save snake is differentiated and the standard Carry Save Adder (CSA) and the Domino method of reasoning-based CSA. And moreover the proposed justification CSA is thought about and the Ripple Carry Adder and Carry Bypass Adder. The proposed arrangement is endorsed by execution of 4-piece Carry Save Adder in a standard 90nm CMOS advancement. This circuits is executed using DSCH Tool, Micro wind Tool.

Keywords— *Carry Save Adder, Ripple Carry Adder, Carry Bypass Adder, Dynamic Logic, Delay and power consumption*

1. INTRODUCTION

High performance, energy- efficient logic style has always been a popular research topic in the field of very large scale integrated (VLSI) circuits because of the continuous demand of ever-increasing circuit operating frequency. Among other things, addressing the necessities of future processing will require rationale style that fulfils superior, low-power, high power as commotion or fluctuation, simplicity of usage and confirmation.

- The main objective is to reduce the delay, area and power consumption.
- The performance of the system is high, hence the speed increases.

2. HIGH PERFORMANCE ADDERS

2.1 Carry save Adder

Carry save Adder is truncated as the CSA appeared in figure 1. As we as a whole realize that adders are utilized for number juggling capacities in information processors. A convey spare snake is a sort of advanced viper, utilized in PC micro architecture to process the aggregate of at least three n-bit numbers in double. It contrasts from other advanced adders in that it yields two quantities of the equivalent dimensions as the information sources, one which is a grouping of halfway whole bits and another which is a sequence of carry bits.

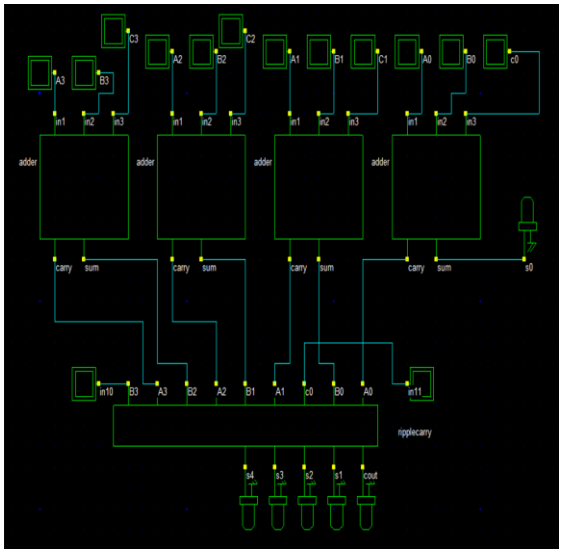

Fig. 1: Carry save adder block diagram

Carry save adder is consists of three or more n-bit binary numbers. Carry save adder is similar as full adder. Here we are computing sum of 3-bit binary numbers, so we take 3 full adders at first stage. Carry save unit consists of 6 full adders, each of which computes single sum and carry bit based only on the corresponding bits of the two input numbers. Let X and Y are two 4-bit numbers and produces partial sum and carry as S and C.

Table 1: Truth table for full Adder

Cin	A	B	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2.2 Ripple carry adder

different full Adders circuits can be fell in relating to incorporate a N-bit number. For a N-bit equivalent Adder, there must be N number of full Adder circuits. A wave convey Adder is a reason circuit in which the total of each full Adder is the pass on in of the predominant next most critical full Adder. It is known as a Ripple convey Adder. Thus, the convey engendering delay is the time slipped by between the use of the convey in signal and the occurrence of the do (Cout) signal. Figure 2 shows Ripple Carry Adder.

Binary Addition:

A 110011

B 1101

A+B :1000000

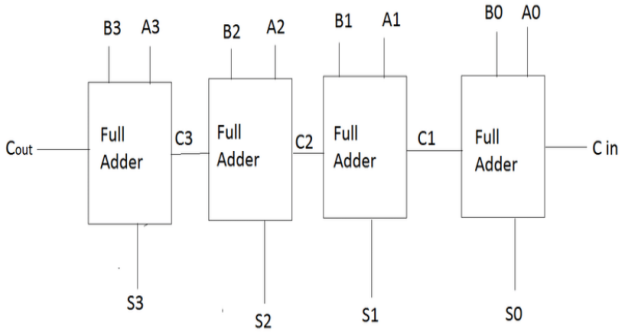

Fig. 2: Ripple carry Adder block diagram

2.3 Carry Bypass Adder

Carry Bypass is am Adder usage that enhances the delay of a Ripple Carry Adder with little exertion contrasted with others. It has low force dispersal and superior activity. On the off chance that a full snake n creates a convey it will be the information carryin (Cin). Carry Bypass is more productive than carry select Adder, appeared in figure 3.

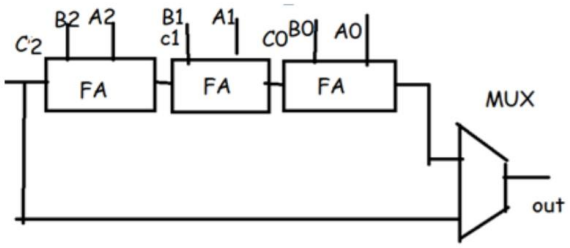

Fig. 3: Carry Bypass Adder block diagram

3. PROPOSED LOGIC

3.1 Dynamic logic

Dynamic CMOS circuits would be astute to execution and require less silicon area than standard static CMOS circuits.The dynamic period of all domino CMOS is investigated of N method of reasoning additionally, discards the inside race conditions by using a support at the yield of each stage that produces simply checking signal. Dynamic rationale is perceived from assumed static rationale in that components basis uses a check signal in its execution of combinational rationale circuits. The common usage of a clock signal is to synchronize changes in progressive method of reasoning circuits. For most executions of combinational rationale, a clock signal isn't required.

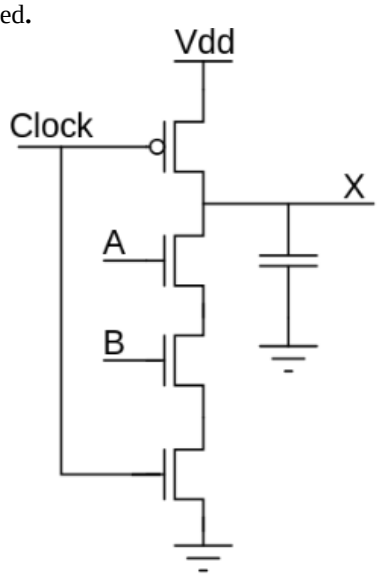

Fig. 4: Dynamic logic

In integrated circuit structure, dynamic logic (or sometimes timed rationale) is an arrangement framework in combinatory rationale circuits, particularly those completed in MOS advancement. It is perceived from the supposed static rationale by abusing brief storage of information in stray and passage capacitances. It was standard during the 1970s and has seen a progressing resurgence in the arrangement of quick propelled devices, particularly computer CPUs. Dynamic rationale circuits are generally speedier than static accomplices, and require less surface locale, anyway are continuously difficult to design.

3.2 Pass Transistor Logic

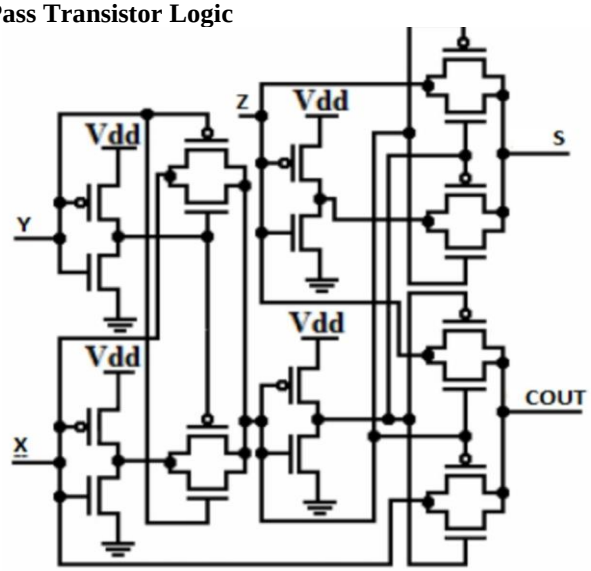

Fig. 5: Pass Transistor Logic

In hardware, Pass Transistor Logic (PTL) depicts a few rationale families utilized in the structure of incorporated circuits. It lessens the tally of transistors used to make distinctive rationale entryways, by taking out repetitive transistors. Transistors are utilized as changes to pass rationale levels between hubs of a circuit, rather than as switches associated straightforwardly to flexibly voltages. This lessens the quantity of dynamic gadgets,

yet has the impediment that the distinction of the voltage among high and low rationale levels diminishes at each stage. Each transistor in arrangement is less immersed at its yield than at its input [5].By differentiate, traditional CMOS logic switches transistors so the yield interfaces with one of the force gracefully rails, so rationale voltage levels in a consecutive chain don't diminish. Since there is less disengagement between input signals and yields, planners must take care to evaluate the impacts of unexpected ways inside the circuit. For legitimate activity, structure rules confine the course of action of circuits, so sneak ways, charge sharing, and moderate exchanging can be maintained a strategic distance from. Recreation of circuits might be required to guarantee sufficient execution.

3.3 Block Diagram

Full Adder diagram is show in figure 6 Full Adder using pass transistor logic.

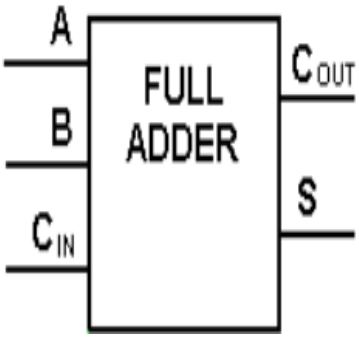

Fig. 6: Full Adder block diagram

3.4 Carry Save Adder Block Diagram

Carry Save Adder block diagram is shown in figure 7. Pass transistor logic implemented full adder has used in the design of carry save adder in order to reduce power dissipation as well as delay. Carry save adder is a combination of half adder and full adder.

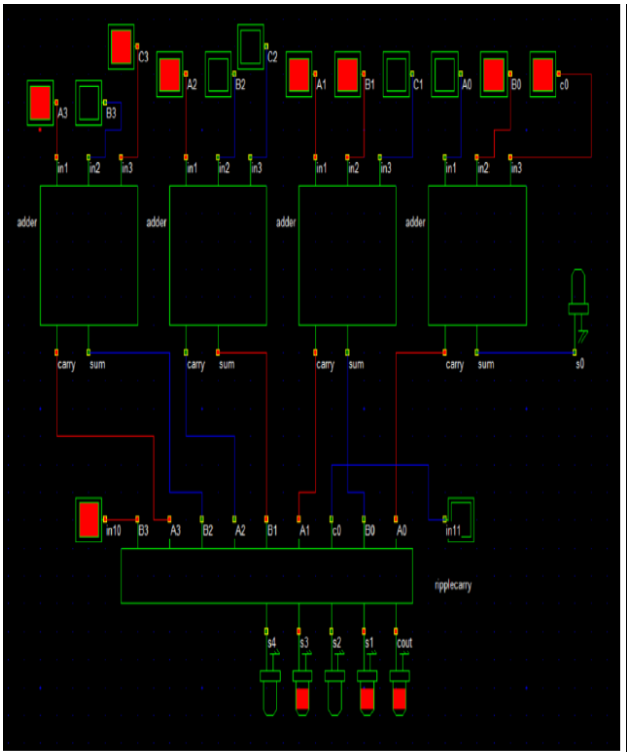

Fig. 7: Carry save adder circuit design in dsch tool

Sum and carry of each full adder is input to the Ripple carry adder s1,s2,s3,s4,cout are the outputs

3.5 Output graph for CSA

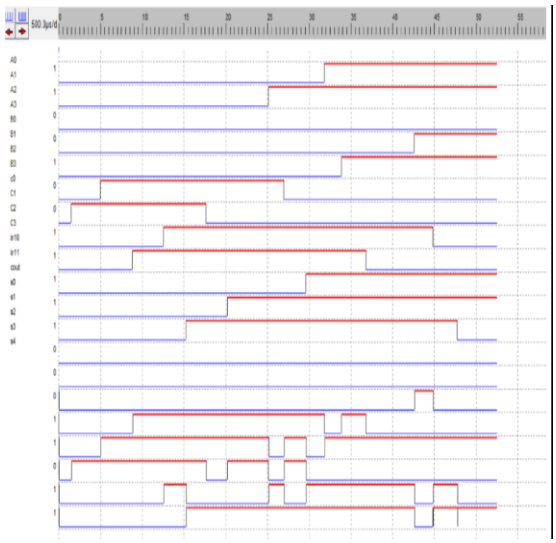

Figure.8. Timing diagram for CSA

3.6 Out for CSA in micro wind

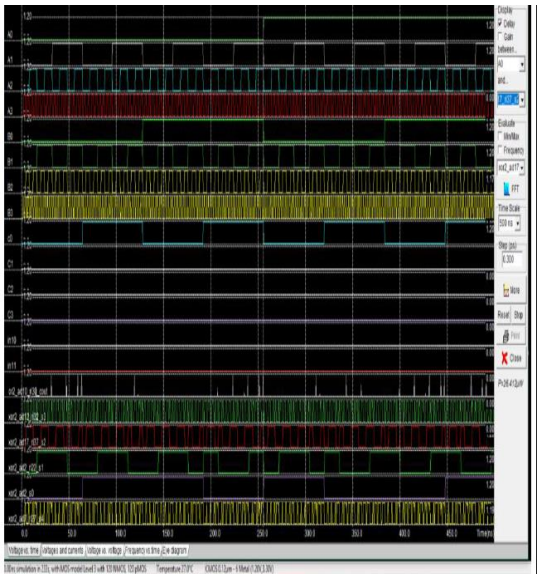

Fig. 9: Output graph for CSA

3.7 Ripple Carry Adder Block Diagram

Ripple Carry Adder (RCA) is a basic adder which works on basic addition principle. The architecture of RCA is shown in figure 10. RCA contains arrangement structure of Full Adders (FA); every FA is used to include two bits along with carry bit. The carry produced from each full adder is given to next full adder etc.

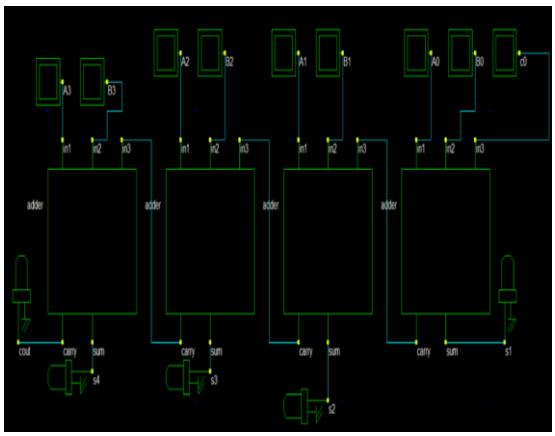

Fig. 10: Ripple carry adder in DSCH tool

In this four full adders are used. s0,s1,s2,s3 is out bit to the sum of each full adder. Carry of first full adder is input to the next full adder. In ripple carry adder applicable for addition of two variables like A, B.

3.8 Output graph for Ripple carry Adder

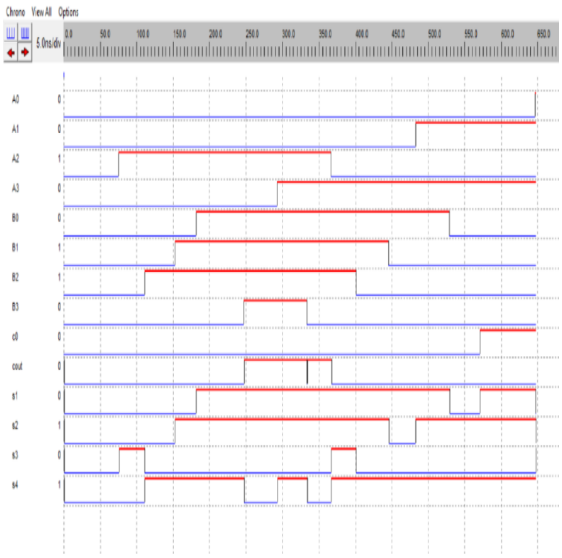

Fig. 11: Timing diagram for ripple carry adder

Out put of Ripple carry Adder in micro wind:

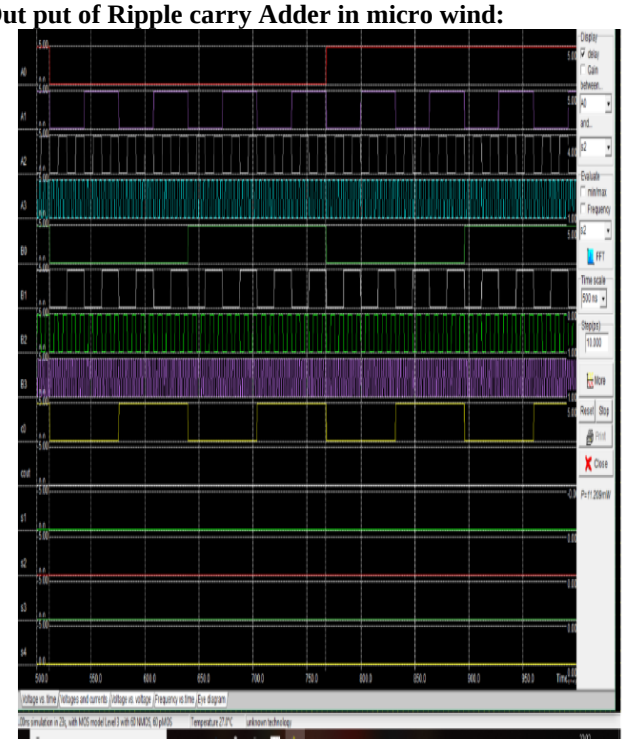

Fig. 12: Ripple carry Adder output in micro wind

Comparison Table 2:

2a.4-bit CSA

Parameters	Dynamic	Pass transistor
Power(uw)	38	26
Delay(ps)	10	7

2b.4-bit RCA

Parameters	Dynamic	Pass transistor
Power(uw)	45	32
Delay(ps)	60	48

4. CONCLUSION

An elite proposed rationale style fundamental objective was to make the pass transistor circuits progressively vigorous and with low force dispersal and low postponement. Execution examination of 4-piece Carry Save Adder uncovers that proposed rationale quicker than domino and customary Carry Save Adder separately. By the examination of pass transistor CSA is quicker than RCA. A CSA utilizing dynamic rationale and pass transistor rationale is planned utilizing Microwind Tool and DSCH Tool.

5. REFERENCES

[1] Design of Low Power and High-Performance Carry Save Adder Using Dynamic Logic, IJETSR, volume 4, May 2018.
[2] Jayasimha.T, Daka Lakshimi, Gokula Lakshmi, Kiruthiga, Kaviya,"Implementation of High Performance Carry Save Adder Using Domino Logic", AJAST ,2017
[3] Khushbu Nagori and Suman Nehra, "Design of a high speed and low power 4 Bit Carry Skip Adder", March 2017.
[4] Pooja Singh and Rajesh Mehra, "Design Analysis of XOR Gates Using CMOS & Pass Transistor Logic", July 2014.
[5] D. Markovic, B. Nikolic and V.G. Oklobdzija, "A general method in synthesis of pass-transistor circuits", 2000.
[6] Min Cha and Earl E. Swartzlander, "Modified Carry Skip Adder for reducing first block delay", 2000.
[7] J. Princy Joice, M. Anitha and Mrs. I. Rexlin Sheeba, "Design of carry save adder using transmission gate logic", Jan 2015.
[8] Pournima Pankaj Patil and Archana Arvind Hatkar "A Comparative analysis of 8-bit carry skip adder using CMOS and PTL techniques with conventional MOSFET at 32nm regime", 2016.

