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Performance analysis of low power 1-Bit CMOS full adder

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ABSTRACT

One-bit full-adder efficiency and interpretation are anatomized into smaller parts. Such modules are thoroughly tested. Multiple designs are created, simulated and evaluated for each full adder. Twenty separate 1-bit full-adder modules are designed by integrating the various designs of these modules. Each of these full adder exhibits different power consumption, speed, area, and driving capabilities. Two realistic circuit structures that include full adders are used for simulation. The main aim of our project is to use CMOS technology to construct an optically reconfigurable low power full adder circuit. Analysis of time parameters in all existing full adders and comparison with the time study of our proposed circuit.

Keywords— *Cadence, CMOS, CPL, Full adder, Power consumption, Transistor, Transmission Gates.*

1. INTRODUCTION

The addition is one of the fundamental arithmetic operations. It is extensively used in many VLSI systems applications such as DSP architectures and microprocessors. In addition to its task, which is adding two binary numbers, it also includes many other useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems, the adder is part that determines the overall performance of the system. That is why enhancing the performance of the 1-bit full-adder is a significant goal. It contains 20 transistors and uses transmission gates and inverters to implement XOR . A binary full adder, including provision for carrying digits, is implemented using for each transmission gate, which functions like an AND-gate [1], The transmission function full adder, which uses 16 transistors, for this circuit, there are two possible short circuits paths. This circuit uses pull-up and pull-down logic as well as complimentary pass Logic [2].

2. PROBLEM DESCRIPTION

Given the three 1-bit inputs and it is desired to calculate the two 1-bit outputs sum and where there are standard implementations for the full-adder cell that will be used as the basis for comparison in this paper. Among these adders, there are the following

(a) The transmission-gates CMOS adder (TG-CMOS) it is based on transmission gates and has 20 transistors.
(b) The low power implementation of the full-adder cell that has only 14 transistors (14T) is based on the low power XOR design and transmission gates.
(c) The complementary pass-transistor logic (CPL) full adder has 32 transistors and uses the CPL logic family.
(d) The CMOS full adder (CMOS) has 28 transistors and is based on the regular CMOS.

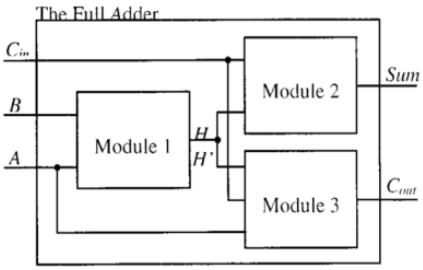

Fig. 1: Full adder

3. PROPOSED CIRCUIT

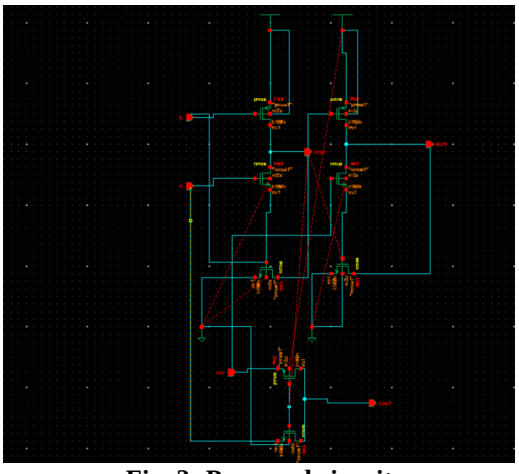

Fig. 2: Proposed circuit

By considering other full adders it has a very less number of transistors and the power consumption and time delay in this circuit are low.

4. ADVANTAGES

This project deals with the tools which we used is Cadence software to analyze the following parameters such as:

(a) For low power consumption
(b) High speed

5. POWER LIMITATIONS

There are three major components of power dissipation in CMOS:

5.1 Switching Power

Power consumed by the circuit capacitance during transistor switching.

5.2 Short Circuit Power

Power consumed by current flowing from supply to ground during transistor switching.

5.3 Static Power

Due to leakage and static currents.

5.4 Dynamic power in CMOS

The first two components are referred to as dynamic power. Dynamic power constitutes the majority of the power dissipated in CMOS circuits. It is the power dissipated during charging or discharging the load capacitances of a circuit.

6. SOFTWARE COMPONENTS

Cadence products primarily target SoC design engineers and are used to move a design into packaged silicon, with products for custom and analog design, digital design, mixed-signal design, verification, and package/PCB design, as well as a broad selection of IP, and also hardware for emulation and FPGA prototyping. Virtuoso ADE product suite enables designers to fully explore, analyze, and verify a design against design goals so that they can maintain design intent throughout the design cycle.

7. RESULTS

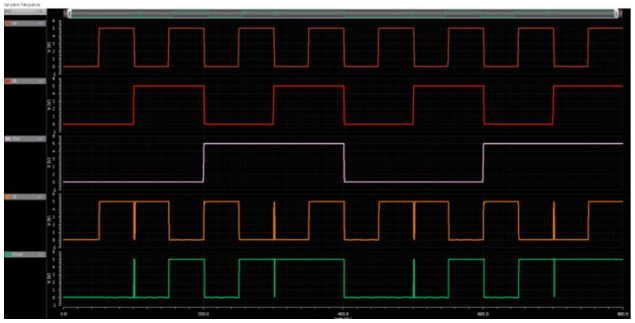

Fig. 3: Results

By observing the above results, it shows the waveform of full adder there are 3 inputs and two outputs, the input is named as A, B, C, and the output is named as Sum and Carry, if the inputs A, B, C is 0 then the outputs Sum and Carry also 0, if the input A=0, B=0, C=1, then the sum=1, carry=0, if input=A=1, B=0, C=0, then the sum=1,carry=0, likewise the waveform moves on up to 7 states. A full adder is a circuit that performs addition. Full adders are implemented with logic gates in software. A full adder adds three one-bit binary numbers with two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit this term is contrasted with a half adder, which adds two binary digits.

8. OBSERVATION OF DELAY

Cell	Number of transistors	Delay (sec)
TG CMOS	20	9.96Å
TFA	16	8.21Å
CPL	32	9.97Å
CMOS	28	7.81Å
Proposed circuit	8	4.861Å

9. CONCLUSION

Thus, the full adder is a circuit that performs addition. Full adders are implemented with logic gates in software. A full adder adds three one-bit binary numbers with two operands and a carry bit. The adder outputs with two numbers, a sum and a carry bit this term is contrasted with a half adder that adds two binary digits. Thus, the project report is concluded with some existing full adder circuits the time was analyzed. Therefore, by comparing other circuits, our proposed circuit performs with a better delay.

10. REFERENCES

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