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Modelling and control of DStatcom using modified DSOGI - SRF Control algorithm

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ABSTRACT

This paper proposes to design and control of three-phase Distribution Static Compensator (DSTATCOM) for mitigating power quality problems at the distribution level. The current related power quality issues such as excess reactive power, harmonics and unbalancing of load are taken into consideration. Control based on Double Second Order Generalized Integrator Synchronous Reference Frame (DSOGI-SRF) theory is developed for generating reference supply currents. Three phases Voltage Source Converter (VSC) with self-support DC bus is used as DSTATCOM. Switching pulses for VSC are generated using hysteresis current control. This system is developed with MATLAB environment using SIMULINK and Sim Power System (SPS) tools.

Keywords— *DSOGI -SRF, DSTATCOM, VSC*

1. INTRODUCTION

Power quality is a combination of voltage and current quality. Power quality is concerned with deviations of voltage and current from the ideal one. The Power quality problem in the AC transmission systems is generally due to the Non-linear loads such as power electronic based loads (use of diodes, thyristor rectifiers and cycloconverters) and Arc furnaces. These Non-linear loads draw non-sinusoidal currents from the utility grid. These currents contain reactive power and harmonics which run down the power quality of the system. So the compensation of reactive power and harmonics has become a major concern for Electrical specialists because reactive power and harmonics increase the losses, cause more heating in the rotating machinery, interferences with communication lines and generation of noise in the system. Besides these, in three-phase four wire system, there is a problem of excessive neutral current.

These Non-linear loads cause the voltage distortion at the Point of Common Coupling (PCC). The distorted supply current at (PCC) is the source of poor voltage for the other loads at (PCC). Poor power quality causes a huge loss to the sensitive loads due to malfunctioning and reduces the lifetime of the equipment. According to International standards such as IEEE-519, the harmonics should be less than 5% [1] which can be done by limiting the harmonic current drawn by the consumers using the active shunt compensator at the (PCC). Here in this paper, we use the Distribution Static Compensator (DSTATCOM), [2] to mitigate the current related problems like low power factor, unbalancing and harmonics control etc. The performance of DSTATCOM depends upon the control algorithms used for firing pulse generation for Voltage Source Converter (VSC) used in these devices. Various control algorithms are available for DSTATCOM such as Instantaneous Reactive Power theory (IRP), Synchronous Reference Frame Theory (SRF) [3], Cross-correlation theory, Neural network and fuzzy logic theory[4] etc. For DSTATCOM a multilevel approach is also presented in [5].

In this paper, we use the control algorithm based on the Synchronous Reference Frame (SRF) theory and Double Second Order Generalized Integrator (DSOGI) based PLL for the three phase distribution system to compensate for harmonic current, reactive current and load balancing in Power Factor Correction (PFC) mode.

2. CHARACHERTISTIC AND DESIGN OF DSTATCOM

Figure1 and figure 2 shows the basic circuit diagram of a three leg VSC based DSTATCOM connected to the three phase AC load with signal sensing. Three phase load may be an unbalanced load or low power factor load (lagging) or Non-linear loads or mixed of these loads. For smoothening the compensating current by reducing the ripples, Interfacing Inductors (L_C) is used at AC side of the Voltage Source Converter (VSC).

A passive ripple filter which consists of small series connected resistor (R_r) and a capacitor (C_r) are installed in parallel with loads at PCC for compensating the high frequency switching noise of the voltage at PCC. Six IGBTs (insulated gate bipolar transistors) switches with anti-parallel diodes are used for realized the three phase voltage source converter (VSC). The harmonics reactive power demanded by the load current is

supplied by the DSTATCOM so that the current from the source side is harmonic free and the load reactive power burden is also compensated. The DSTATCOM is operated for reactive power compensation for power factor correction in which there is no phase difference between the source current and the voltage at PCC [6]. The data considered for the analysis of the system is shown in the appendix. The voltage source converter (VSC) is designed for compensating the reactive power of 33 KVAR as decided by the details of the load. The selection of the component of the system is given below [7].

2.1 DC Bus Voltage

The DC bus voltage is calculated as,

$$V_{dc}=2\sqrt{2}V_{LL}/(\sqrt{3}\ \mathrm{m}) \quad (1)$$

The minimum value of the DC bus voltage should be greater than twice the peak of the phase voltage of the system. Where m is the modulation index and considered as 1. The AC line to the line output voltage V_{dc} of DSTATCOM for V_{LL} of 415 V is obtained as 677.7 and considered as 700V.

2.2 DC Bus capacitor

According to the principle of energy conservation the value of DC capacitor $C_{dc}$is given as

$$\frac{1}{2}C_{dc}\{(V_{dc}^2)-(V_{dc1}^2)\}=3\mathrm{V}\ (\mathrm{aI})\ \mathrm{t} \quad (2)$$

The C_{dc} depend on the instantaneous energy available during the transients. Where V_{dc} is the reference DC voltage and V_{dc1} is the minimum voltage level of DC bus is the overloading factor, V is the phase voltage, I is the phase current, and t is the time by which the DC bus voltage is to be recovered. Considering the minimum voltage level of the DC bus, Vdc1= 690 V, V_{dc}= 700 V, V = 240 V, I = 28 A, t = 350 µs, a = 1, the calculated value of C_{dc} is 2600 µF and is selected as 3000 µF.

2.3 AC inductor

The AC inductor is calculated as

$$L_f = \mathrm{m}V_{dc}\ /(12\cdot \mathrm{a}\cdot f_s.i_{cr-pp}) \quad (3)$$

Which depends on the supply frequencyf_s, current ripple i_{cr-pp} and DC supply voltage V_{dc}, where a is overload factor and m is the modulation index. Considering, i_{cr-pp} = 5%,f_s = 10 kHz, m = 1,V_{dc} = 700 V, a = 1.2, the $L_f$value is calculated to be 2.44 mH. A round-off value of$L_f$of 2.5 mH is selected in this investigation.

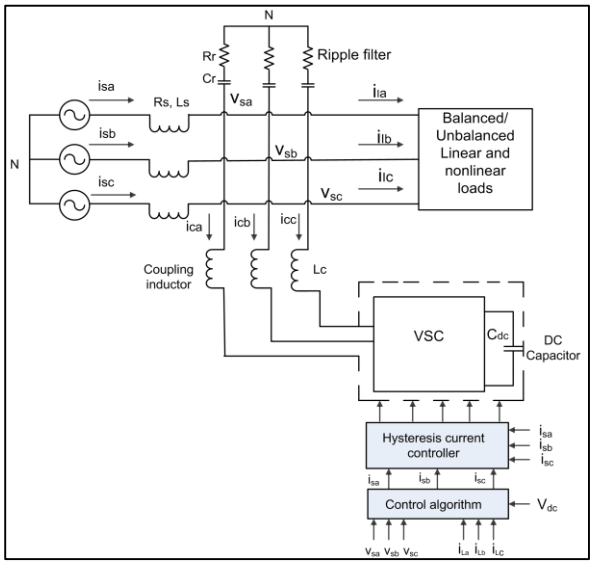

Fig.1: Schematics of proposed three-leg VSC based DSTATCOM

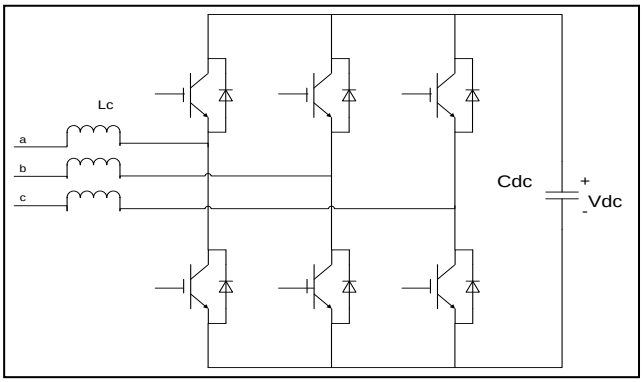

Fig. 2: Schematic of three-phase VSC

2.4 Ripple filter

A low pass first order passive filter is used to filter the high frequency noise from the voltage at PCC which is tuned at half the switching frequency. Considering a low impedance of 8Ω for the harmonic voltage at a frequency of 5 KHz, the ripple filter capacitor is designed as C_r=5 f. A series of resistance R_r of 5Ω is connected in series with a filter capacitor C_r.The ripple filter is connected at the PCC in parallel with the load. The impedance is found to be 637 Ω at the fundamental frequency, which is sufficiently large, and hence, the ripple filter draws negligible fundamental current. The time constant of the filter should be very small compared to the fundamental time period (T)

$$R_fC_f \ll T/10 \quad (4)$$

3. CONTROL ALGORITHM

The control algorithm for the proposed system consists of three stages. For an approximation of the reference AC mains current for the control of VSC used in this proposed system, the control algorithm is used. In this paper SRF and DSOGI –PLL are used as control algorithm for extraction of reference supply currents.

3.1 Synchronous reference frame theory

The synchronous reference frame theory is used for control of three phases three wire DSTATCOM in this literature [8]-[9], although there are many control algorithms are available for the generation of reference source currents. The block diagram of the control algorithm for DSTATCOM is shown in Fig.3. Quantities (i_{La}, i_{Lb}, i_{Lc}) be the load currents, (v_{sa}, v_{sb}, v_{sc}) be the PCC voltages and $V_{dc}$is the DC bus voltage of DSTATCOM is sensed as feedback signals. A park's transformation is used to convert the three phase load current (i_{La}, i_{La}, i_{Lc}) into the d-q-0 frame as in below equation.

$$\begin{bmatrix} I_0 \\ I_d \\ I_q \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \cos(\theta) & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta+\frac{2\pi}{3}\right) \end{bmatrix}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (5)$$

The three phase (PLL) phase locked loop is used to synchronize these signals with the PCC voltage. The low pass filter is used to pass the d-q components to extract the DC value of $I_d$andI_q. The error between the reference DC capacitor voltage (V_{dcr}) and the sensed DC bus voltage (V_{dc}) of DSTATCOM is given to a PI (proportional-integral) controller which output is considered as the loss component (P_{loss}) and is added to the DC component of I_{ddc}.The controller strategy is used to regulate

the PCC voltage, load balancing and to eliminate the harmonics of load current. Using the inverse park's transformation the I_d and I_q current again converted into the reference source current. Here hysteresis current controller is used to control the three phase source current to generate the gating pulse for voltage source converter (VSC). PI controller is required in the control algorithm for the power factor correction.

3.2 DSOGI-PLL

Double second order generalized integrator PLL (DSOGI-PLL) shown in Fig. 4 is same as Sinusoidal Signal Integrator PLL (SSI-PLL), which extracts the fundamental positive sequence to the synchronous frame – PLL [10]-[13]. To contraption the quadrature –signals generator it utilizes a double second order generalized integrator.

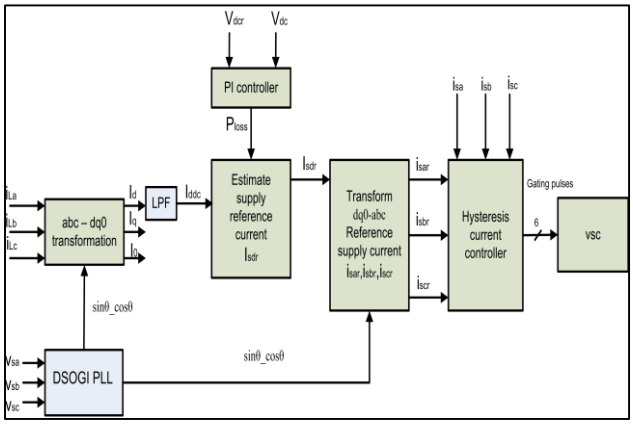

Fig. 3: Control algorithm for the three-leg VSC based DSTATCOM in a three phase 3-wire system

$v_{abc} = [v_a v_b v_c]^T$ is the three-phase voltage vector and its positive sequence component can be expressed as:

$$v^+_{abc} = [v^+_a v^+_b v^+_c]^T = [T]v_{abc} \quad (6)$$

Where

$$[T] = \frac{1}{3}\begin{bmatrix} 1 & a^2 a \\ a & 1 \; a^2 \\ a^2 a & 1 \end{bmatrix}, a = e^{-j\frac{2\pi}{3}} \quad (7)$$

The positive-sequence component of the voltage vectors $v^+_{\alpha\beta}$, the negative-sequence component of the voltage vectors $v^-_{\alpha\beta}$ can be also obtained as follows:

$$v^+_{\alpha\beta} = C_{32}v^+_{abc} = C_{32}[T]v_{abc} = C_{32}[T]C_{23}v_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix} v_{\alpha\beta} \quad (8)$$

Where,

$$C_{32} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, C_{23} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}^T \quad (9)$$

$$v^-_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix} v_{\alpha\beta}, \quad q = e^{-j\frac{\pi}{2}} \quad (10)$$

For extraction of accurate sequence component, it requires 90-degree phase shift for v_α and v_β . For obtaining a 90 degree phase shift for v_α and v_β two solutions are as follows:

(a) Transport delay buffer method

(b) All pass filter method.

However, these two methods are not frequency-adaptive, which could give rise to errors in the positive sequence estimation and they can't block harmonics from the input signals [12]. A smart combination of a Low Pass Filter (LPF) and a Band-Pass Filter (BPF) is utilized to solve the above problems. Harmonics are filtered by using both BPF and LPF but 90 degree phase shift provided by LPF only.

$$LPF(s) = \frac{qv'}{v} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \quad (11)$$

$$BPF(s) = \frac{v'}{v} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \quad (12)$$

Therefore, DSOGI –PLL method can provide accurate positive sequence information for grid synchronization even under grid faulty conditions.

3.3 Design of hysteresis current controller

Figure 5 shows the hysteresis current controller for tracking of reference source currents. The actual source currents and the error signal of the reference are determined and compared within a small hysteresis band of 1 to 5% because a wide hysteresis band may not provide effective tracking and the system may become unstable [8]. A narrow hysteresis band results in the very good and fast tracking of currents but switching frequency may become too high. If (i_{sa}<i_{sar}- h_b), then the upper switch of VSC is OFF and lower switch is ON[9]. The upper and the lower switching device (IGBT in the VSC) are switched in a complementary fashion.

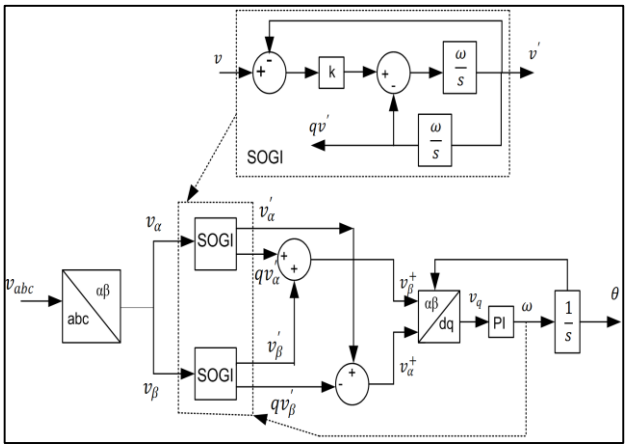

Fig. 4: Block Diagram of DSOGI-PLL

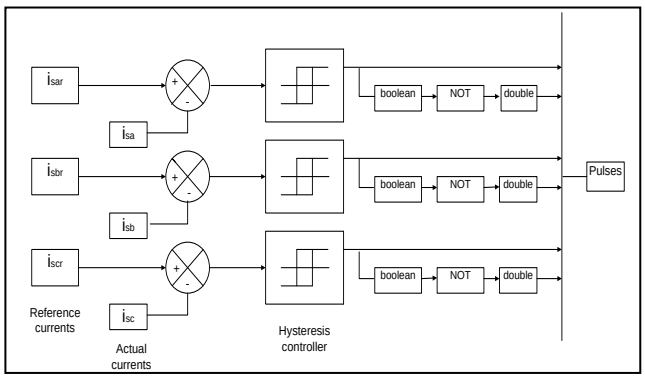

Fig. 5: Hysteresis current controller for tracing of reference source current

4. SIMULATION RESULT AND DISCUSSION

Simulink model of the test system is given in figure 6. In the simulation, the test system model with DSTATCOM employing SRF algorithm is simulated for 0.5 seconds.

In the Simulink model system, the breaker is used. The breaker is used to control the connection of a variable load to the system. This system is analyzed for two different load conditions. One load is a linear load that is fixed resistive load and another load is Non-linear load that is three phase diode

rectifier with R-L load. The result of the simulation is to analyze the performance of voltage source inverter based DSTATCOM in PFC mode under linear load and harmonic suppression and load unbalancing under non-linear load.

4.1 Performance of VSC based DSTATCOM under linear load

The source voltage (V_s), source current (i_s),compensator current (i_{cabc}),load current(i_{labc}),DC bus voltage(V_{dc}) for linear load are shown in figure 7. The DC bus voltage in the system is constant which is equal to 700VDC. It is analyzed that these source currents are balanced and power factor is unity at source side for given loads as the loads are compensated by the DSTATCOM

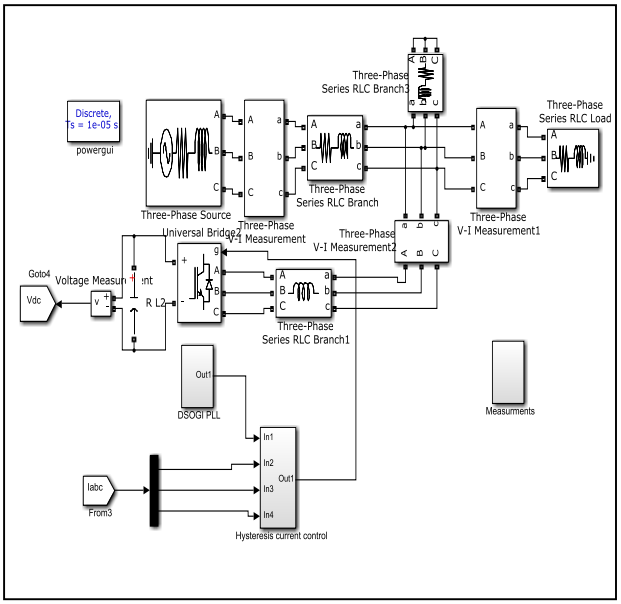

Fig. 6: Simulink model of the test system

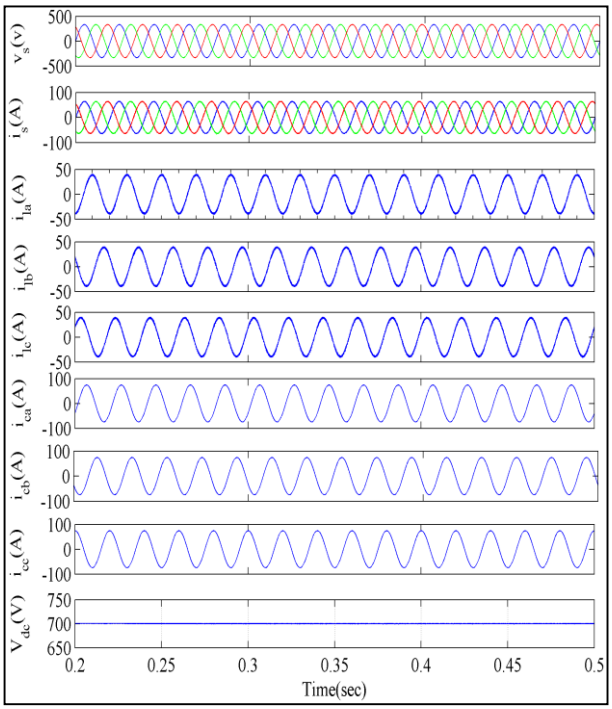

Fig. 7: Performance of DSTATCOM under linear load

Figure 8 shows the active power supply by source, active power demanded by load and reactive power delivered by the compensator. It is analyzed that the active power required by the load side that is 33 kw. 33 kw is completely given by the supply side and the compensating power is zero.

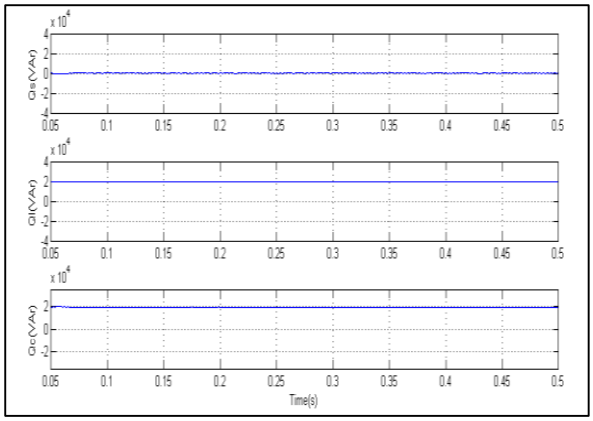

Fig. 8: Reactive power compensation under linear load

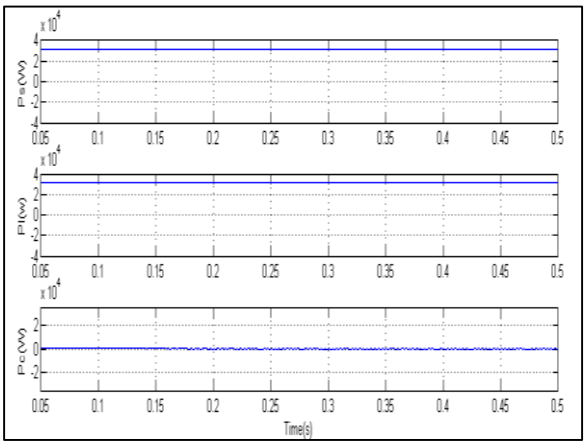

Fig. 9: Active power at the source side, load side and at compensator side

Figure 9 shows the active power supply by source, reactive power demanded by load and the reactive power delivered by the compensator. It is analyzed that the reactive power which was demanded by the load side that is 20 KVAR. The reactive power supplied by the source side is zero and 20 KVAR reactive power is completely supplied by the compensator. Hence the system is working at unity power factor.

4.2 Performance of VSC based DSTATCOM under non-linear load

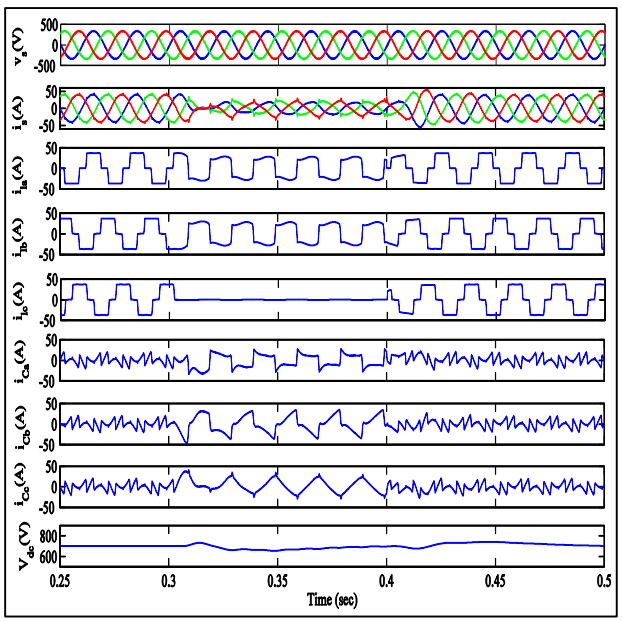

Fig. 10: Performances of DSTATCOM under non-linear load

The source voltage (V_s), source current (i_s), compensator current (i_{cabc}), load current (i_{labc}), DC bus voltage (V_{dc}) for Non-linear load are shown in Fig.10.The DC bus voltage in the system is constant which is equal to 700V DC. With the help of breaker 2, the linear load is converted into Non-linear load. Either the load is balanced/unbalanced nonlinear loads, the source currents are balanced, harmonic free and power factor is unity at the source side. Harmonic spectra and THD of source current and load current are shown in Fig. 11. FFT analysis analyzed the THD of source current and load current are 2.77% and 26.61% respectively.

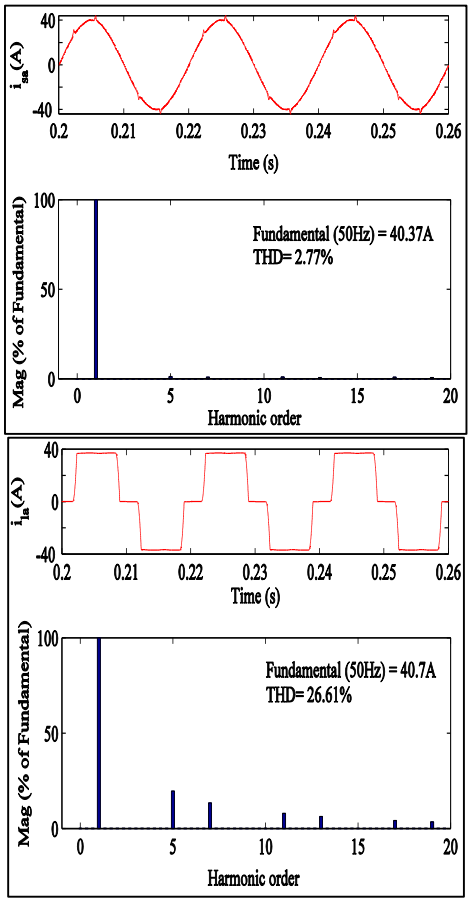

Fig. 11: Harmonic spectra of source current and load current

5. CONCLUSION

This paper presents the performance of DSTATCOM in three phases three wire distribution systems under linear and nonlinear loads. The SRF control algorithm with DSOGI-PLL has shown improved performance in generating reference currents and fast synchronization of VSC with the grid. The test system has been analyzed and results have been present for power factor correction under linear load and harmonic suppression under nonlinear load. The PI controller has been used to regulate DC bus voltage and shows improved the performances of DSTATCOM. The proposed DSTATCOM with DSOGI-SRF algorithm provides quick and independent control for various power quality features like – power factor correction, voltage regulation along with load balancing.

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APPENDIX

Data for simulation

AC line voltage 415V (line to line), 50Hz; source impedance: R_s =0.01Ω,L_s=0.05 mH; voltage source converter: DC link voltage 700V, DC capacitor 2500μF,interfacing inductor 2mH,switching frequency 10 KHz. For ripple filter:R_r =3Ω,C_r =20μF; linear load: three phase load 33 kilowatt, 0.8 power factor each, non-linear load: three phase bridge rectifier with R=12Ω, L=100mH; PI controller gain K_p=1,K_i=20.

