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Design and simulation of Carry Save Adder using VHDL

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ABSTRACT

This paper presents a low power and high-speed multi-operand adder which shows a higher degree of modularity than other existing adders. In Digital Signal Processing (DSP) applications, Addition is one of the fundamental operations. In advance technology, researches are still going on to design an adder that carries out addition in a twinkle of time. Carry Save Adder (CSA) is one of such high speed and low power adder. This paper focuses on the designing and simulation of Carrying Save Adder (CSA) using Carry Look ahead adder instead of using usual ripple carry adder so that speed increases by 10%.

Keywords— *Carry Save Adder (CSA), VHDL design*

1. INTRODUCTION

1.1 Carry look ahead adder

One of the probable techniques for decreasing carry propagation delay time is to use quicker logic gates. But there exists a boundary below that it is not possible to reduce the gate delay. There is another method relating to hardware which is mostly adopted called look-ahead carry. The concept is used to look ahead and generate the value of carry for a fixed implicit addition operation. It would result otherwise from some last operation. Two new binary variables are defined to discuss the concept, one is Pi called CARRY PROPAGATE and another is G_i called CARRY GENERATE. The binary variable G_i is as called as it generates a carry whenever A_i and B_i are '1'. The binary variable P_i is called CARRY PROPAGATE because it is instrumental in the propagation of C_i to C_{i+1}. CARRY, SUM, CARRY GENERATE and CARRY PROPAGATE parameters are presented using the following equations

$$Pi = Ai \oplus Bi$$
$$Gi = Ai\_Bi$$
$$Si = Pi \oplus Ci$$
$$Ci+1 = Pi\_Ci + Gi$$

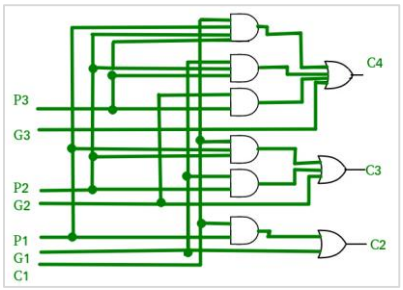

Fig. 1: Carry look generator with AND-OR

The C4 does not wait for C3 and C2 to propagate; it is clear from the expressions for C2 and C3. In similar, it is not required for C3 that it will wait for C2 to propagate. The actual reality will be known in the hardware design and the implementation of all equations describes the concept of look-ahead carry generator. The look-ahead carry generator following AND-OR logic based on the implementation of the above logics is shown in figure 1. Figure 1 presents the logic diagram of a 4-bit adder with the suggested concept of look-ahead carry. The block considered look-ahead carry generator is analogous to figure 2. The input half-adder slice of different full adders instituting 4-bit adder is presented by the logic gate shown to the left side of the presented block. EX-OR are taking outputs with the portion of the output half-adders and different full adders on the right side. The output of the logic is accessible as sum output at the output end after the combinational delay of two logic levels of the gates. The digital logic IC no.

74182 is for typical operation of look-ahead carry generator following TTL logic family. The IC is applicable to produce relevant carry inputs corresponding to 4 four-bit binary adders, which are linked in cascaded form can perform the operations on two 16-bit numbers in a similar way. The reality is that the 4-bit adders are capable to produce outputs as CARRY GENERATE and CARRY PROPAGATE.

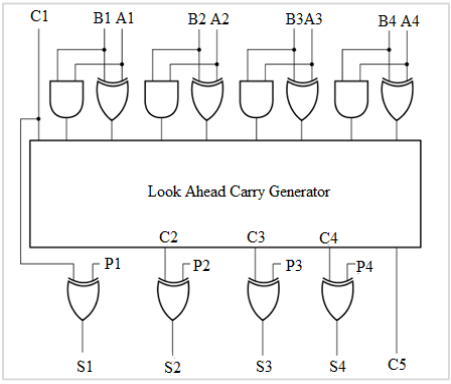

Fig. 2: Carry look ahead generator

1.2 Carry Select Adder (CSA)

The carry-select adder is an actual method to implement addition operation, in which logic element is used to work out the (n+1) bit sum of n bit numbers. The CSA adder is faster and simple as it has the gate level depth of O√(n). It contains two ripples carry adders and multiplexers to add two n-bit numbers. Fig. 3 presents the carry select adder of 4 bit. Two ripples carry adders, perform the calculations two times. In one time, it is assumed that the carry is being zero and another time carry is one. The actual sum output is obtained after the calculations of two results, as well as the correct output of carry-out is tailed by the selection of multiplexer with the correct information of known carry. In each select block, the number of bits can be variable or uniform. The optimal delay will be there for a block size of √(n). The block size must have a delay in case of the variable with additional inputs A and B to the carry output and it is equal to the chain of multiplexer following it. The uniform size provides the delay O√(n.The carry calculation is done just in time and will yield an equal delay with respect to the multiplexers.

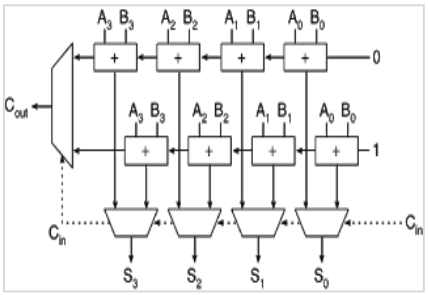

Fig. 3: Carry Select Adder

2. RESULT AND DISCUSSIONS

The Xilinx software provides the RTL of the developed chip of adder which is depicted in the figure 4 and internals schematic is also presented in the figure 5. The waveform simulation of the same is given in figure 6

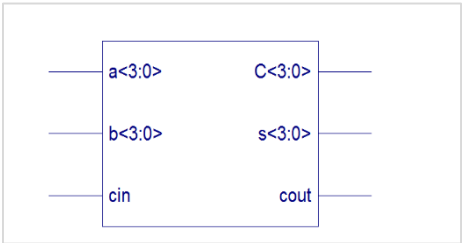

Fig. 4: RTL view of Carry Select Adder

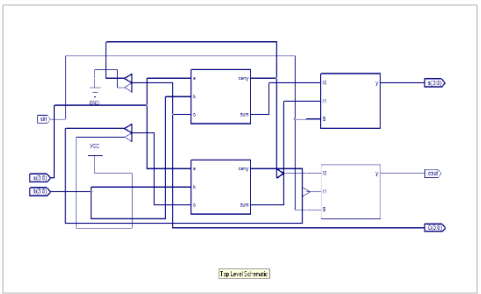

Fig. 5: Internal schematic of 4 bit Carry Select Adder

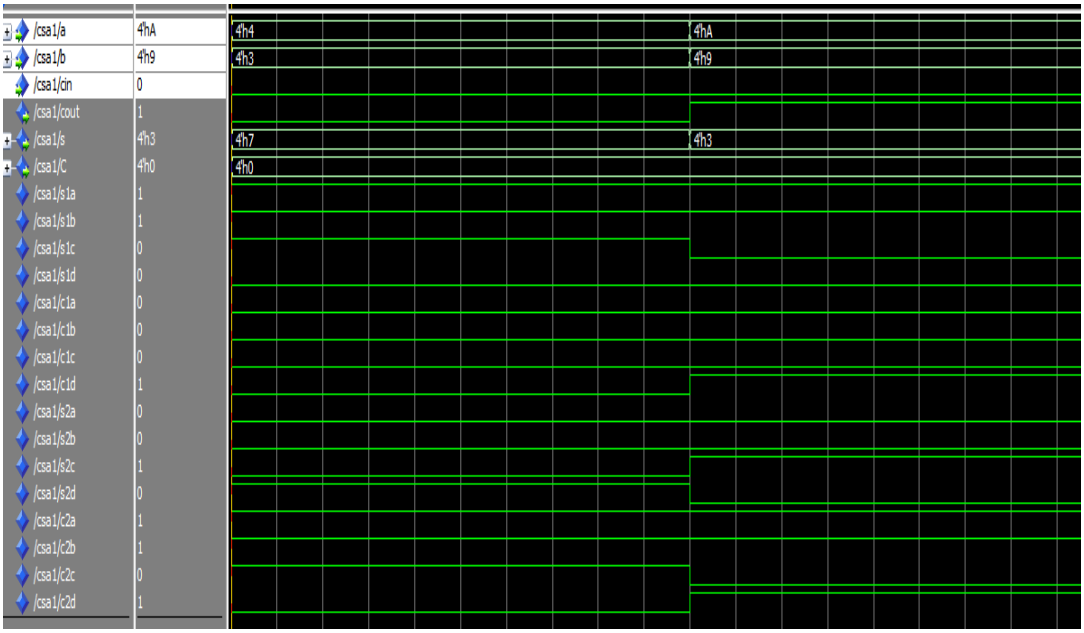

Fig. 6: Modelsim waveform simulation of Carry Save Adder in integer

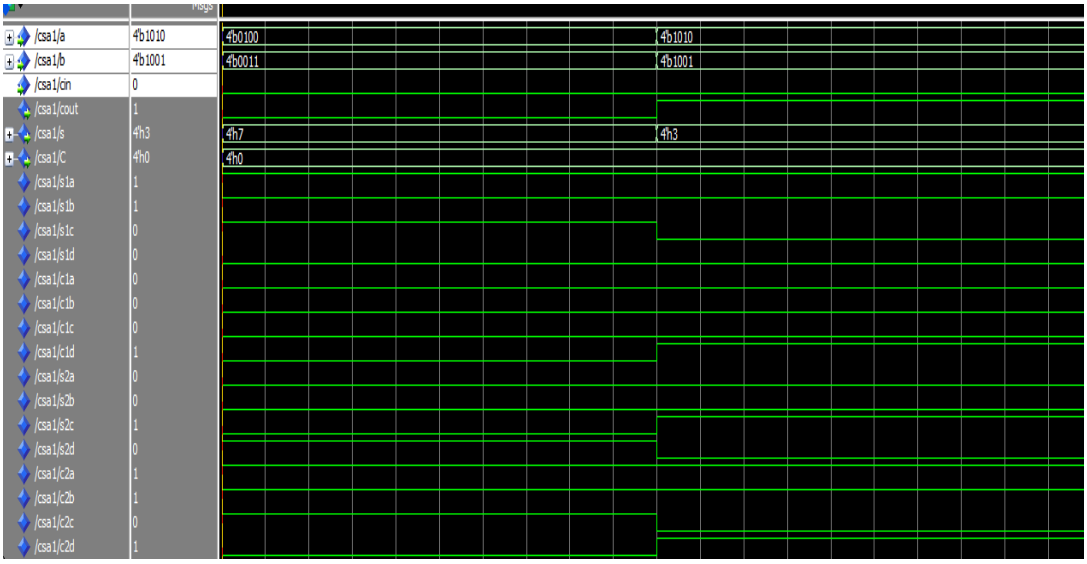

Fig. 7: Modelsim waveform simulation of carrying Save Adder in binary

Table 1: Comparison of Adder design parameters

Parameter	Ripple Carry Adder	Carry Select Adder
Slices Usage	6	9
LUTs Usage	10	16
IoBs	17	18
Memory Usage	90336 kb	91360 kb
Combinational time	12.160ns	12.135ns

The comparative analysis of the Adder design is also carried. Table 1 shows the comparison between 4 bit carry ripple adder and 4 bit Carry Select Adder in terms of slices, IoBs and LUTs and delay. It is estimated that CSA adder has less delay than ripple carries adder.

3. CONCLUSION

The design of carrying save adder is done in Xilinx ISE 14.2 successfully. The output of the carry Save Adder is simulated for many cases in modelsim10.1 software. The CSA requires 4 input sequence. The CSA design consists of two carries look ahead adder. The adder utilizes fewer hardware parameters and its performance is very good in comparison to Ripple carry adder application for DSP Applications. The FPGA hardware parameters such as slices, LUTs an, DSP elements and IoBs are also analysed. The combinational time for Ripple Carry Adder and Carry Save Adder is 9.160 ns and 9.135 ns. The Carry Select Adder design is an approach which is optimal in terms of area and speed for several DSP applications.

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