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Design and analysis of low power 1-bit hybrid full adder using 130nm technology

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ABSTRACT

Basically, a conventional CMOS logic circuit design approach depends upon charging the output capacitive nodes to the supply voltage Vdd or discharging it to the ground. This is one of the most used methods in VLSI circuit designs. There are various techniques to design low power circuits to reduce power consumption. The major source of power dissipation is the charging and discharging of the capacitor. Whenever a capacitor is discharged to ground, an amount of energy stored in the capacitor is mislaid. We can reduce this power dissipation by restoring this energy to the source instead of discharging to the ground. It has been observed that by charging the capacitor gradually, the energy requirement is slighter than the faster charging method. The modern VLSI techniques focus significantly on High-Speed Propagation and Low Power Consumption. In this study, I present a low power 1-bit hybrid full adder design which utilizes both static CMOS logic and Swing Restoring Pass Transistor Logic. Moreover, a comparison is made on the power consumptions of various other designs with this work. The full adders are designed in Mentor Graphics 130nm technology. Starting at 0.4V supply, the average power consumed by this Hybrid design is 2.33µW.

Keywords— *Low power full adder, Multiplexer, CMOS logic, Swing restoring pass-transistor logic*

1. INTRODUCTION

The main need for Low Power Circuit Design is to increase the eminence of portable systems and the need to limit power consumption. During recent years the development of low power VLSI circuits is increasing rapidly. The driving forces behind these developments are portable applications requiring low power consumption and high-speed propagation, such as notebook computers, portable communication devices, and mobile phones. Hence, the low-power design of VLSI circuits has emerged as a very active and rapidly developing field of CMOS design. The inadequate battery lifetime typically imposes very strict demands on the overall power consumption of the portable system. This paper mainly focuses on full adder design, as the full adder is very important in every digital system. Full adders are used in carrying out multiplications, ALU (Arithmetic Logic Unit), calculate addresses, table indices, increment and decrement operators, generating memory addresses inside a computer and to make the Program Counterpoint to next instruction, for graphics related applications, where there is a very much need of complex computations, the GPU uses optimized ALU which is made up of full adders, full adder is the fundamental unit of DSP -VLSI architecture and also MAC units have a Full-adder in their core blocks. Thus, development in the performance of the 1-bit adder block shall cause improvement in the performance of the intact system. This implies us the need and necessity of developments and deep study of adders. This 1-bit Full adder is able of adding 3 (1-bit) inputs and gives a 1-bit Sum and 1-bit Carry.

2. FULL ADDER DESIGN

A full adder circuit is an arithmetic circuit block that can be used to add three bits to produce a sum and a carry output. Such a building block becomes a necessity when it comes to adding binary numbers with a large number of bits. The full adder circuit overcomes the limitation of the half adders, which can be used to add two bits only.

Fig. 1: Block diagram of full adder

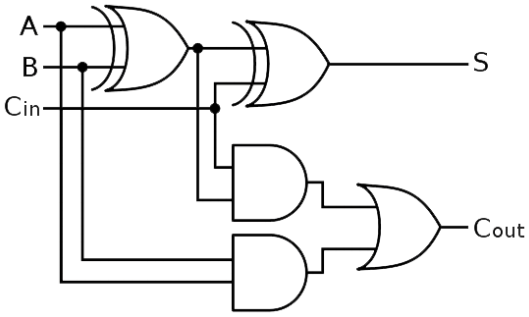

Fig. 2: Logic Implementation of Full Adder

A one-bit full-adder adds three one-bit numbers, often written as *A*, *B*, and C_{in}. A and B are the operands, and C_{in} is a bit carried in from the previous less-significant stage. The circuit produces a two-bit output.

A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates. One example implementation is with

$$\boldsymbol{S = A \oplus B \oplus Cin \; and \; Cout = (A \cdot B) + (Cin \cdot (A \oplus B))}.$$

Various full adder designs are used to compare with the proposed adder design in this work. Some basic full adder designs such as static CMOS, SERF (Static Energy Recovery Full-*adder*), Transmission gate adder, 12T adder are used.

Table 1: Truth table of full adder

Inputs			Outputs	
A	**B**	**C_{in}**	**C_{out}**	**S**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The various designs of the full adders consist of a different number of transistors as listed below.

Table 2: List of designs with a number of transistors

Logic style	No. of Transistors
Static CMOS	28
SERF	10
Transmission Gate	20
12T	12
Proposed design	20

3. ARCHITECTURE OF 1-BIT LOW POWER HYBRID ADDER

The proposed 1-bit full adder consists of 3 Multiplexers and 4 inverters. This Full adder architecture is designed using two logic styles, a combination of Static CMOS and Swing Restoring Pass Transistor Logic.

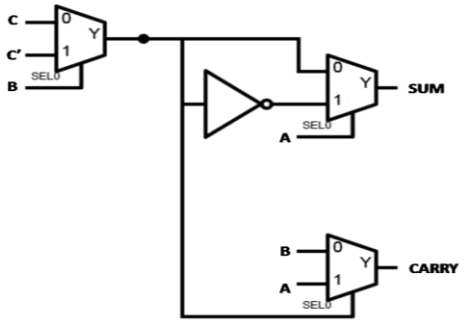

Fig. 3: Block diagram of 1-Bit Hybrid full adder

Here the inputs are considered in the same order for proper comprehension of the truth table of a 1-bit full adder. Multiplexers used here are realized by Switch Restoring Pass Transistor Logic. The 2X1 MUX logic entails 4 transistors and each NOT gate requires 2 transistors. As a result, the total number of transistors required is 20 transistors

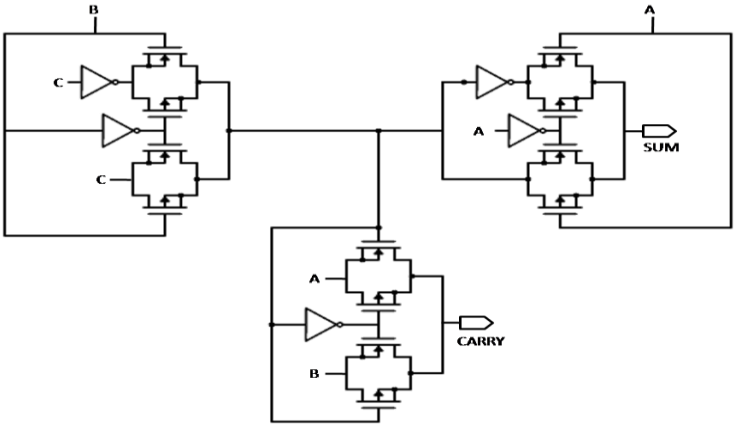

Fig 4: Schematic of 1-Bit Hybrid adder logic

4. ANALYSIS, SIMULATION AND RESULTS

Here results are obtained for power consumption at various input levels. The simulation is done in Mentor Graphics using 130nm Technology. A comparison is carried out with the Static CMOS Adder design, SERF, Transmission gate Full Adder, 12T adder, and Hybrid full adder. All the mentioned designs are simulated in the same condition and same technology.

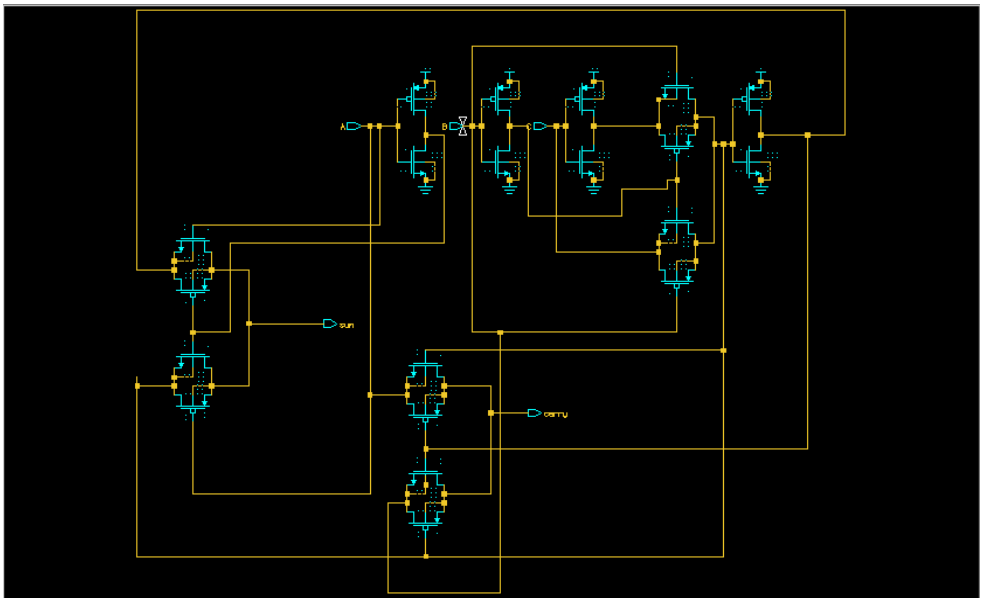

Fig. 5: Schematic of 1-Bit Hybrid full adder

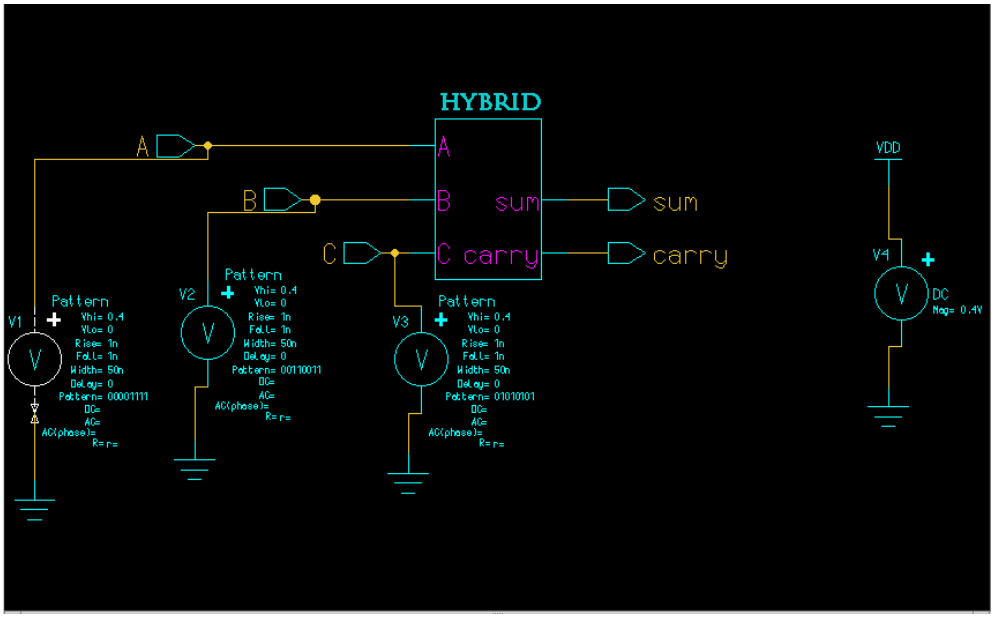

Fig. 6: Simulation circuit of 1-Bit Hybrid full adder

The proposed design is simulated for different voltages ranging from 0.4V to 0.8V. At every voltage level, the power consumed is noted and compared to other designs.

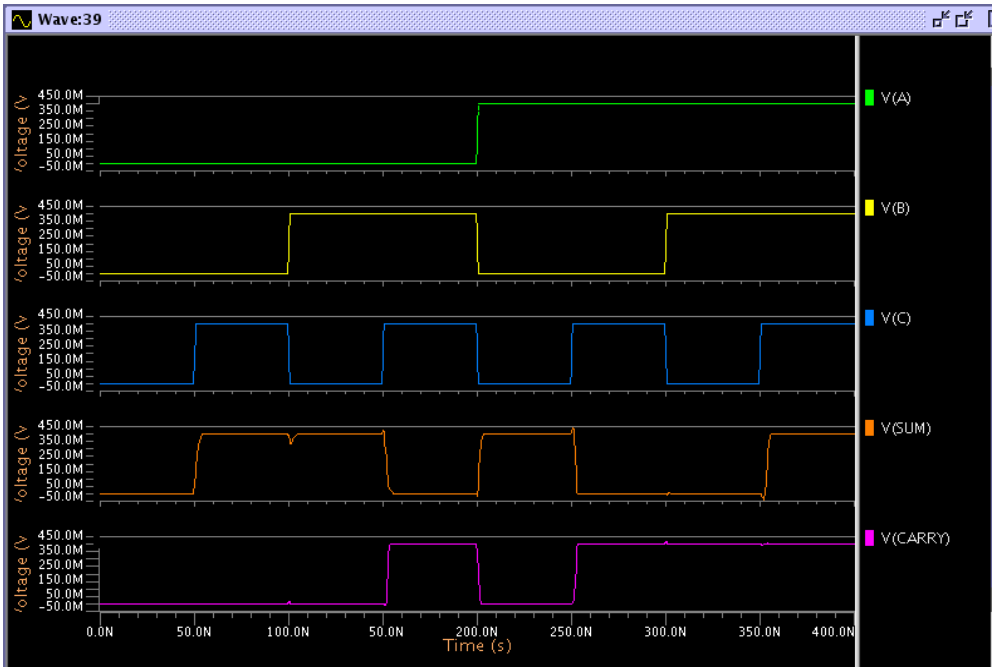

Fig. 7: Transient response of Hybrid adder at a 0.4V input voltage

The power consumed is calculated by using measurement tools in the simulation results window. Here peek-to-peek power is measured at every level of input voltages applied.

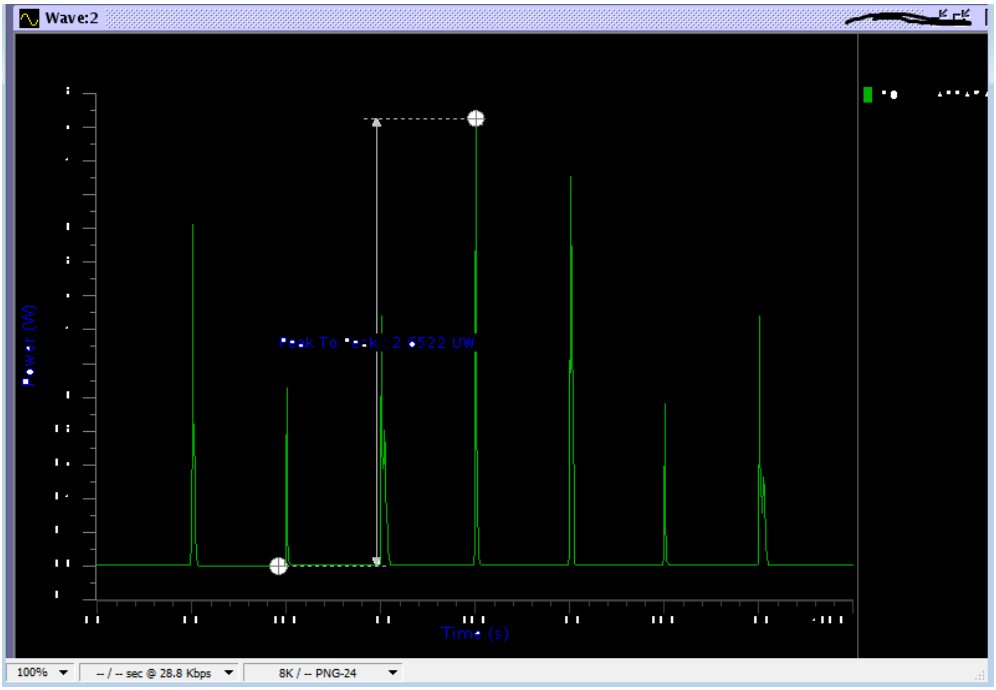

Fig. 8: Power response of Hybrid adder at a 0.4V input voltage

For 0.4V input voltage, the observed power consumption is approximately 2uW peak to peak.

4.1 Power comparison of various logic styles

The power consumptions for different voltages are noted and a comparison is made for all the mentioned logic styles.

Table 3: Power Consumptions at different voltages

VOLTAGE(V)	POWER IN UW				
	Static CMOS	12T	TGL	SERF	Hybrid
0.4	19.25	6.241	9.3	4.77	2.35
0.5	31.5	16.29	19.46	14.38	8.4
0.6	66.48	35.43	36.58	34.8	19.07
0.7	209.45	102.8	109.12	91.4	27.45
0.8	368.78	270.32	232.58	325.5	67.5

The graph is obtained by plotting the input voltages and power.

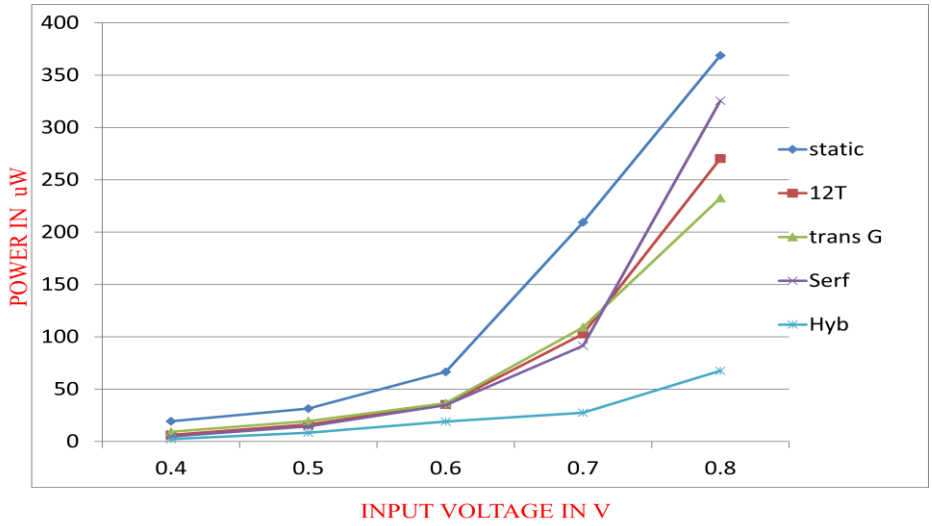

Fig 9: Power comparisons of various logic styles

5. CONCLUSION

Full Adder is the heart of any digital and data processing applications. In conclusion, the basic operation found in most arithmetic components is the binary addition. The addition is the most basic arithmetic operation. In this study, an analysis of all the adders has been individually carried out. The design and analysis of 1-bit hybrid Full adder are made in Mentor Graphics. The simulations have been achieved for 130nm technology at different supply voltage levels. Thus, the results acquired shows that as the input voltage is lowered the power consumption decreases gradually. The proposed hybrid full adder shows exceptional performance even at low voltages and has excellent output levels. Moreover, the different adders were compared on the basis of power consumption.

Hence it's concluded that the proposed 1-bit hybrid Full Adder is a good preference in the future at scaled technology.

6. ACKNOWLEDGEMENT

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