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Carry look ahead adder using adiabatic logic

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ABSTRACT

Nowadays in digital circuits, some important issues like high speed, high throughput, small silicon area, and low power consumption are being considered by designers. Full adders are important components in applications such as subtraction, counting multiplication, filtering, Digital Signal Processors (DSP) architectures, and microprocessors. So it at interest to design carry look ahead adder because of its high-speed operation and to study the functional behavior and power consumption. In this project, the CLA is implemented using 180nm CMOS technology in cadence virtuoso tool software. Two logics that is static CMOS and adiabatic logic have been analyzed and implemented. Finally, the power consumption is estimated and compared. From the results, power consumption will be found that adiabatic logic consumes low power whereas static CMOS logic offers low delay.

Keywords— *Adiabatic logic, Static CMOS logic, Power consumption, Full adder, Carry look ahead adder, Cadence virtuoso tool software*

1. INTRODUCTION

The increased demand for portable and small size devices in the last few decades, to implement integrated circuits with low power consumption, integrated circuits require electronic circuit design methods. The computer systems have been improved in several order of magnitude with great performances with an ever growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades. The increased power and energy dissipation of the systems have been accompanied by such a phenomenal performance improvement. To understand better the sources of power dissipation, the factors that affect them and methodologies and techniques to achieve optimal results, the design of low power consumption should be successful. Therefore, this thesis is on the sources of power dissipation in an integrated circuit. For various different Levels, such as the architecture level, the gate level and the technology level, the low power design can be applied. Apart from that, to report the characteristic.

Regarding power consumption, a number of alternative logic design styles is present. One of the best circuit design methods to reduce energy consumption in different operations is adiabatic logic design. Only a few topologies of adiabatic logic satisfy our requirements, those are compatible to a static CMOS design flow and robust with respect to P-V-T variation and to generate energy efficient manner, a manageable number of clock pulses can be applied.

2. LITERATURE SURVEY

Low power circuits and their designs find applications in electronic components which have power efficient processing capabilities. The high-speed processor consumes more power and multipliers contribute maximum extent of this power consumption. Adiabatic logic is one of technology where we can achieve low power designs different types of the designs area implemented using adiabatic logic and this paper provides a survey of various multipliers and adders that are modified into a logic power multiplier using adiabatic logic. [1]

Important issues in digital circuits like high speed, high throughput, and small silicon area low power consumption are considered by designers. An important component such as full adders in the applications such as subtraction, counting, multiplication,

filtering, DSP architectures and microprocessors. Carry look ahead adder as a high-speed operation where designer as great interest. Power consumption of static and adiabatic logic is been implemented and compared in this paper. [2]

In present-day power consumption major role in VLSI design technology. There is a rapid increase for the demand for low power consuming devices and adiabatic logic style is a better solution. In this paper different method for designing adiabatic logics such as ECRL, PFAL, CAL, DFAL, 2N-2P and 2N-2N-2P had been investigated. The simulation results show the comparison of power consumption of conventional CMOS and adiabatic logic circuits. [3]

There exist only a few partial comparisons and no methodological investigation of the robustness amongst the adiabatic logic families. We compare different adiabatic logic families with respect to energy consumption area occupation and frequency range keeping 4-bit adder as a reference circuit. Significant differences are found among various adiabatic implementations and reduction of energy dissipation compared to standard CMOS. The effect of supply voltage scaling, as well as the sensitivity to technological parameters, have been investigated in this paper. [4]

The speed is improved by reducing the amount of time required for carrying bits in CLA. In the ripple carry adder carry bit is calculated along the sum bit and each bit must wait until the previous carry has been calculated, which is slower. The carry looks ahead adder calculates one or more carry bits before the sum where larger value bits can be calculated. Since the wait time is reduced. [5]

3. CARRY LOOKAHEAD ADDER

The popular methodology among computational logic elements is binary addition. The ripple carry order is an n-nit adder which has n one-bit full adders. Carry is computed in this method until (n-1) th adder has computed the (n-1) th output, the adder is not complete. The total delay of the logic element is done by the carry chain. Therefore speeding up in carrying chain leads to the speeding up an adder. As the speed of addition with reminds amount of power is the main criteria, carry look ahead adder is chosen, the one way to speed up the carry computation is carry look ahead adder. The carry computation is broken into 2 steps by CLA, starting with the computation of two intermediate values. The adder has 2 inputs ai and bi, then propagate (pi) and generate (gi) is given by

$$Pi = Ai\ XOR\ Bi \tag{1}$$

$$Gi = Ai\ Bi \tag{2}$$

P_i and G_i depend only on the input bits and thus valid after one gate delay.
The sum and carry outputs can be written as

$$Ci + 1 = Gi + Pi\ Ci \tag{3}$$

$$Si = Ci\ (XOR)\ Ai\ (XOR)\ Bi \tag{4}$$

So, C_{i+1} is a function of inputs and C_i

These equations tell that carry signal will be generated into 2 cases:
(a) If both bits A_i and B_i and are 1.
(b) If either A_i or Bi is 1 and carry-in (C_i) is 1.

Schematic diagram of 4-bit CLA is shown in the below figure:

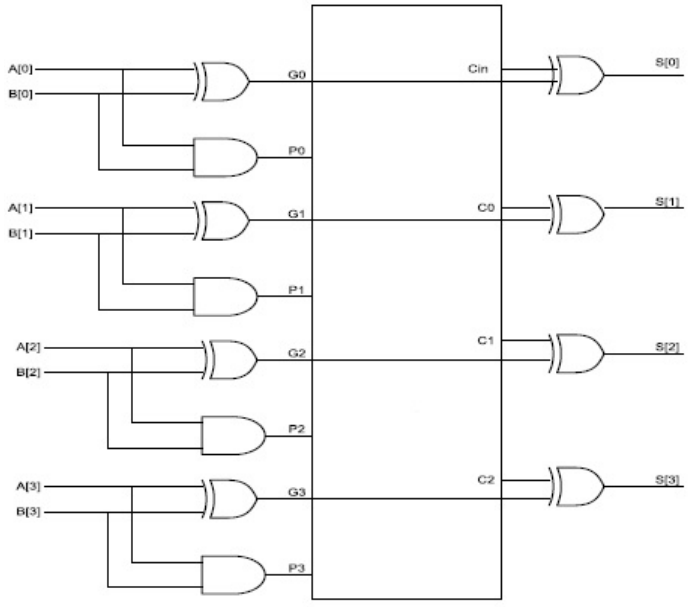

Fig. 1: Schematic diagram of 4-bit carry look ahead adder sum

4. CMOS IMPLEMENTATION

Behind the rapid improvements in integrated circuit products with excellent performance, the scaling of MOS transistors plays the main driving force. The reduced transistor dimensions increased transistor counts and increased operating frequencies improve the performance. The reduction in the amount of energy used during switching event is the important feature of scale MOS transistor. The combination of lower parasitic capacitance from the overall feature side and from low operating voltage is the cause for the reduction in switching energy. It is important to note transistor switching energy due to overall circuit power constraint. These are two function determining blocks such as n-block and p-block in CMOS logic gates. These are normally n input gates for a 2n number of the transistor. The fundamental logic circuits in cadence virtuoso schematic are shown in the fig2. AND, OR, Inverter. The simulation results show that the task is basically charging and discharging of parasitic capacitances with propagating signal through various logic functions. Low input capacitance and high input conductance are required for the logic transistor. Therefore we use 1.8V supply voltage. In this work, 180nm technology have been used for the simulation process. It is important to understand the power consumption behaviour of the digital CMOS circuit. The current that leaks through the transistor even when they are turned off is static power. Dynamic power which arises from the repeated capacitance charge and discharge outputs of the gate in the chip. Only dynamic power has been a significant source of power consumption. Dynamic power is proportional to the square of the supply voltage. So reducing power consumption. The overall power consumption as the sum of dynamic and static power.

$$P = ACV2f + VIleak$$

Where f $(V\text{-}V_{th})/V$
V- Transistor supply voltage
V_{th}- threshold voltage

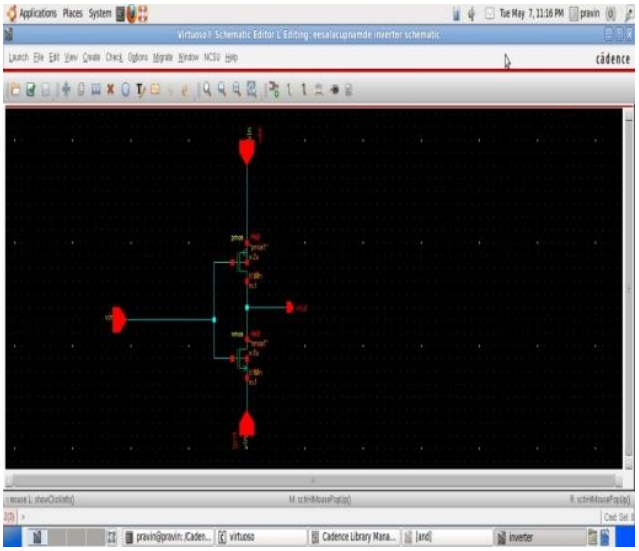

Fig. 2: Inverter logic gate

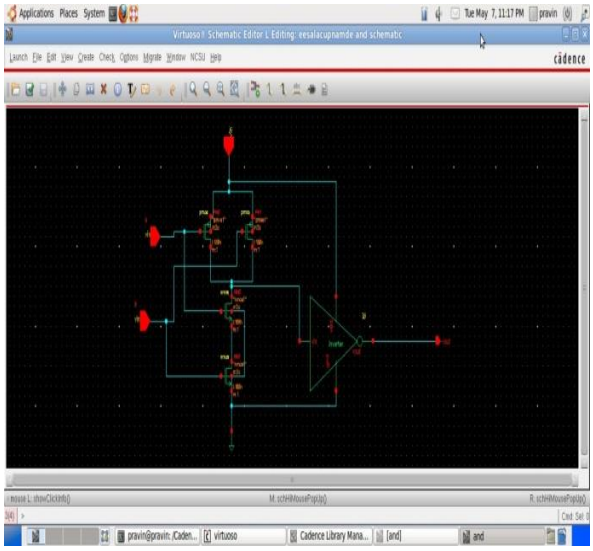

Fig. 3: And the logic gate

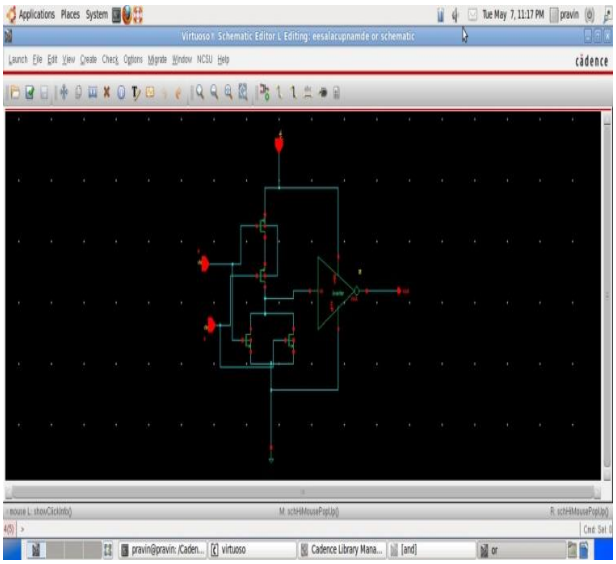

Fig. 4: OR logic gate

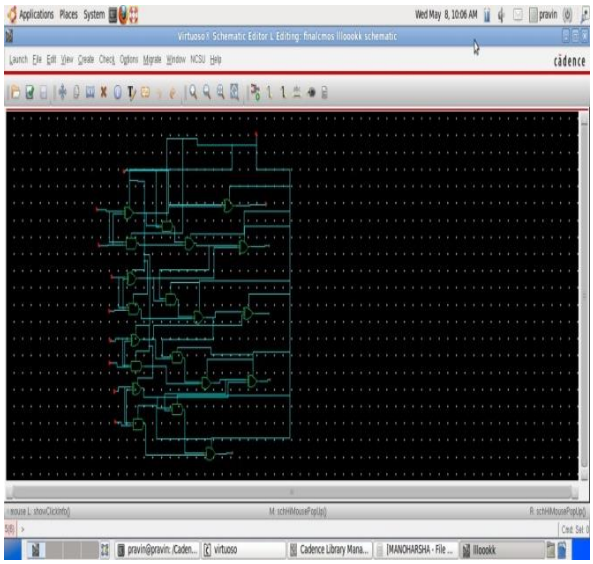

Fig. 5: Carry look ahead adder

5. CMOS IMPLEMENTATION RESULTS

Power and Waveforms of carrying look ahead adder is as shown in the below figure:

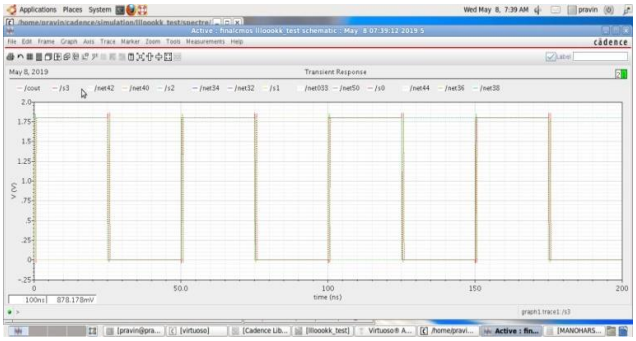

Fig. 6: CLA waveform

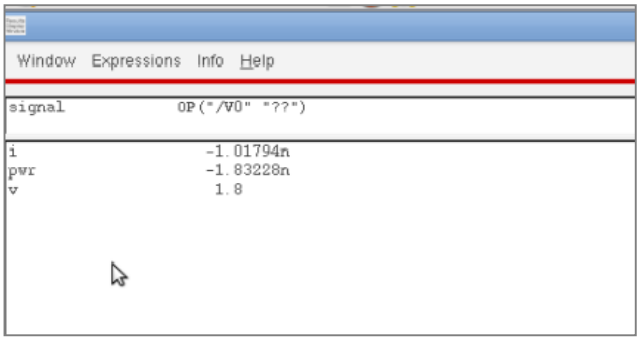

Fig. 7: Power calculations

6. ADIABATIC LOGIC IMPLEMENTATION

In conventional static CMOS, the power supply delivers the charge to the internal nodes of the circuit and later it returns to the ground. While through the resistive elements in the current path all the energy is dissipated. The more efficient way in the adiabatic charge recovery circuits is that charge and discharge capacitances are by restricting the current to flow across devices using clock signals and it is possible to recycle the energy stored in the node capacitors using AC supply. Hence adiabatic circuits are more significant power saving compared to static CMOS. To fabricate the adiabatic logic circuit, it doesn't require different technology than the static one. The phase clocked controlled evaluation of each adiabatic logic stage is the important difference between adiabatic logic and static logic. The deep submicron phase is installed in the semiconductor process, hence the transistor increases continuously which is integrated into a single chip. Significant reduction of on-chip power density has received considerable favor. To achieve low energy dissipation, adiabatic circuits are a promising approach whereby restricting the current flow across the devices with low voltage drop and recycling the energy stored on their load capacitances by using a time-varying ac power supply. Transferring charge between circuit capacitances and time-varying supply voltage enables the charge transfer to occur in a controlled manner is the main idea behind adiabatic logic. In conventional COMS circuits, by reducing the supply voltage, node capacitances and switching activity to a certain extent power dissipation can be minimized. But adiabatic appears naturally acceptable and practical solution in low power VLSI system. To look a deeper on energy recovery principle in adiabatic logic family the following mathematical analysis is based on the time period (T), stored charge (C), load capacitance (C_L), channel resistance (R) is sufficient.

$$EDSS = (RCL/T)\, CL\, V2DD$$

Theoretically, by extending the switching time it is possible to reduce the power dissipation.
Adiabatic logic are classified into (1) fully adiabatic (2) quasi /partial adiabatic circuits.

(A) Fully adiabatic: All charges are stored in the load capacitor is recovered and fed back to the power supply in fully.

- Pass Transistor Adiabatic Logic (PAL) and
- Split-rail Charge Recovery Logic (SCRL) is popular fully adiabatic techniques.

(B) Partial adiabatic: some of the charges are allowed to transfer to the ground. Therefore part energy is recovered.

- Efficient Charge Recovery Logic (ECRL)
- Positive Feedback Adiabatic Logic (PFAL)
- 2N-2N-2P adiabatic logic
- NMOS Energy Recovery Logic (NERL)
- Clocked Adiabatic Logic (CAL)
- Two-phase adiabatic static clocked logic

In this paper ECRL, 2N-2N-2P is implemented and compared.

7. EFFICIENT CHARGE RECOVERY LOGIC IMPLEMENTATION

In adiabatic ECRL is one of the simplest logic. In this design charge recovery part of the circuit is composed of 2 cross-connected PMOS transistor and a logic portion is made of NMOS transistor. Actual and inversion of it can be obtained from the adiabatic logic circuit. The AND, OR, NOT of ECRL schematic in cadence virtuoso is shown in the below figure.

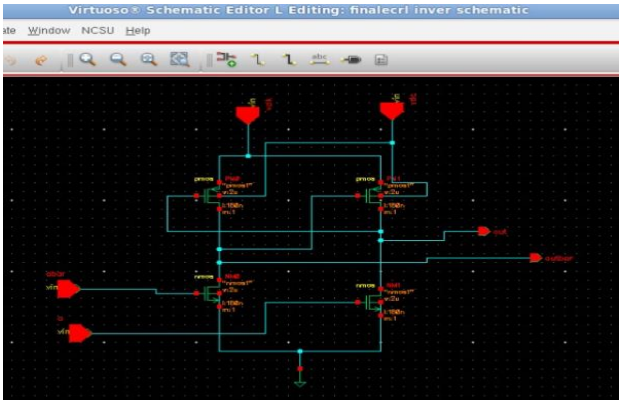

Fig. 8: NOT logic gate

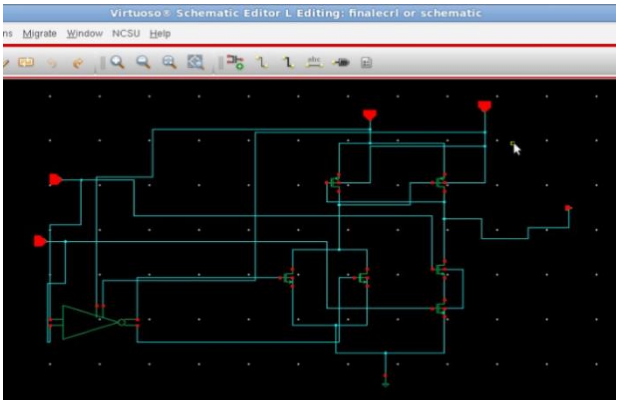

Fig. 9: OR logic gate

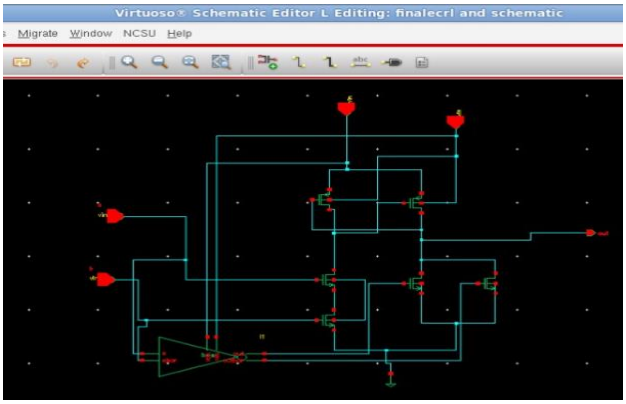

Fig. 10: AND logic gate

Fig. 11: Carry look ahead adder

8. ECRL IMPLEMENT RESULTS

Power and Waveforms of ECRL carry look ahead adder is as shown in the below figure:

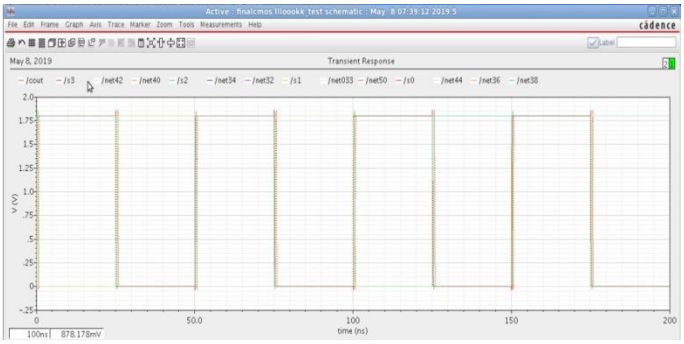

Fig. 12: CLA Waveform

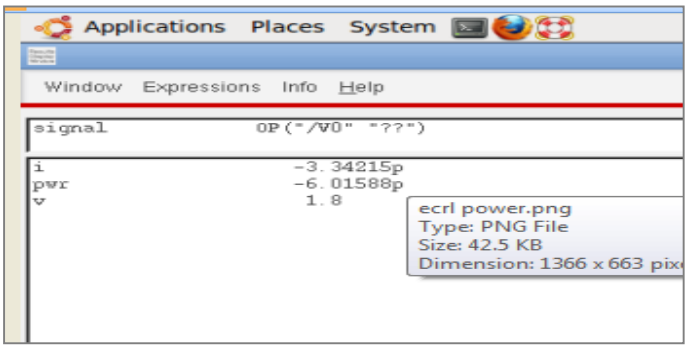

Fig. 13: CLA Power Calculations

8.1 2N-2N-2P implementation

The 2N-2N-2P is based on the convention of using a number of the transistor because each of input cost in term of the transistor is 2N FETS. Here each gate computes both logic and complement function. And each gate requires the input of both polarities to represent. The only difference between 2N-2P and 2N-2N-2P is that a pair of cross-coupled N-FET is added to cross-coupled P-FETs common to both families. The 2N-2N-2P and, or, not gate schematic in cadence virtuoso is shown below:

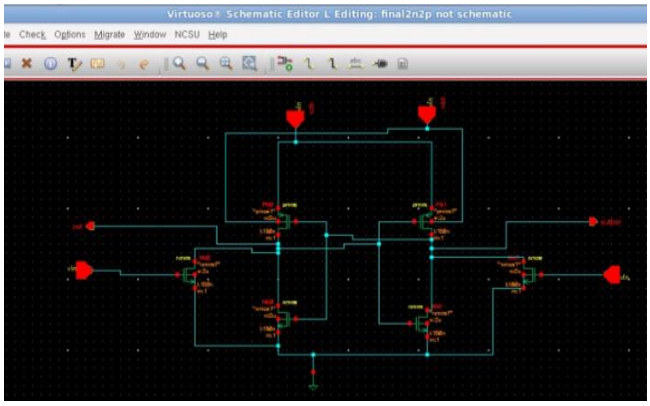

Fig. 14: NOT logic gate

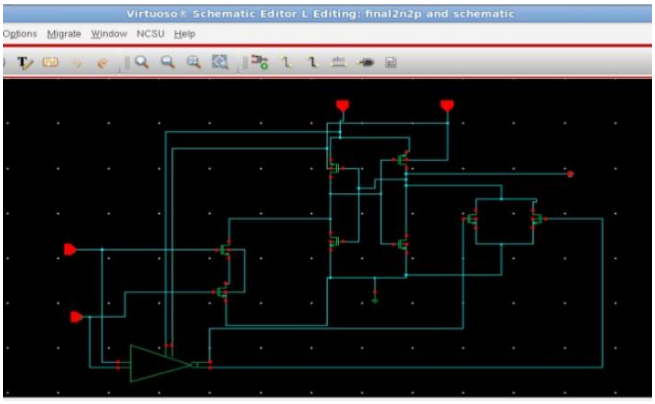

Fig. 15: OR logic gate

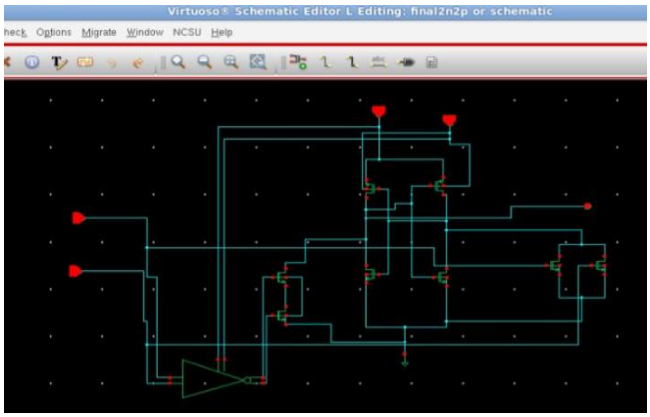

Fig. 16: AND logic gate

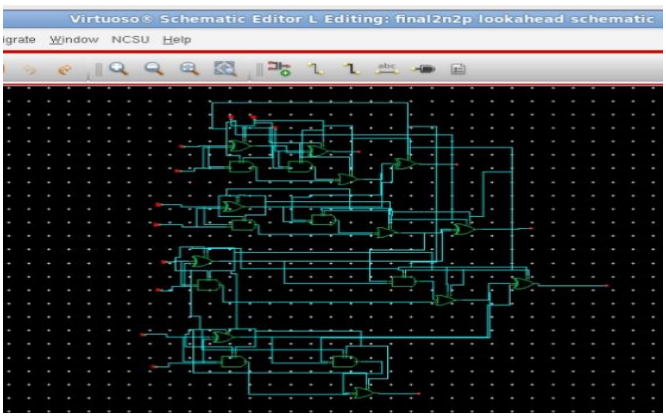

Fig. 17: Carry look ahead adder

8.2 2N-2N-2P implementation results

Power and Waveforms of 2N-2N-2P carry look ahead adder is as shown in the below figure:

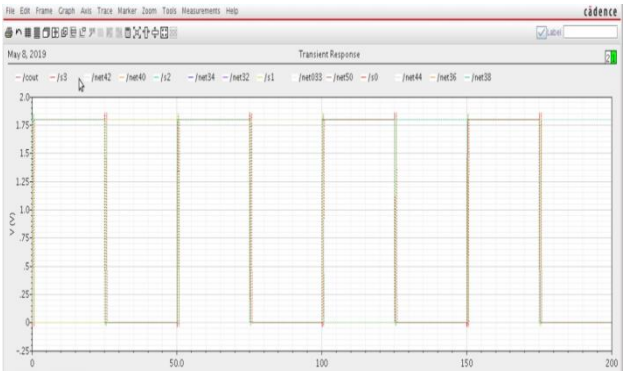

Fig. 18: CLA waveforms

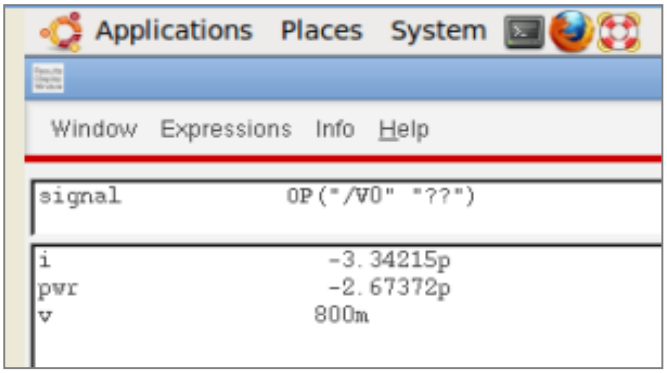

Fig. 19: CLA Power Calculation

9. COMPARISION OF STATIC CMOS AND ADIABATIC LOGIC

Table 1: Power and Gates comparison of CMOS and adiabatic logic

Logic / Characteristic	Average Power Dissipation	No. Of transistors
CMOS	-1.83228E-9	128
ECRL	-6.01588E-12	152
2N-2N2P	-3.34E-12	336

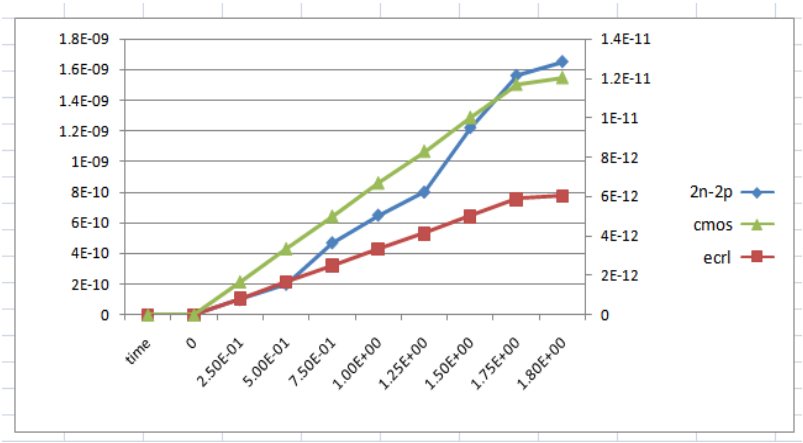

Fig. 20: Comparison of CMOS, ECRL, 2N-2N-2P Power

10. CONCLUSION

This work concludes from the above simulation results and comparisons, efficient charge recovery adiabatic logic dissipates power almost 50% less than the conventional static CMOS logic and 2N-2N-2P adiabatic logic dissipates slightly greater than ECRL and less than CMOS logic.

11. REFERENCES

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