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Comparison research on FIR filter with RRC filter using a reconfigurable constant multiplier

Arya P. Kumar
aryapkumar111@gmail.com
Believers Church Caarmel Engineering College, Ranny Perunad, Kerala

Mercy Mathew
mercy13@gmail.com
Believers Church Caarmel Engineering College, Ranny Perunad, Kerala

ABSTRACT

This paper proposes a capable constant multiplier architecture with the help of an architecture called Binary Common Sub-Expression (BCSE) algorithm. As multiplication using coefficients or constants plays a necessary role in Digital Signal Processing (DSP). Firstly, a single constant multiplier switching between some constants are converted to an n-bit constant multiplier in which any of the bit can be generated at the output according to the input bit x using the BCSE algorithm. Then an RRC filter is designed using then-bit multiplier and finally, the performance of the RRC filter is compared with that of FIR filter.

Keywords— *BCSE, RRC, FIR*

1. INTRODUCTION

As the selection of constants plays an important role in multiplication processes. In any filter, the major factor that determines the performance of the desired filter is the multiplier. So the design of such multiplier constant is considered as a major research focus area over the past decades. FIR filter has a wide range of applications including DSP systems, image processing, video processing, and wireless communication. Systems like multi-standard video code [2] and Software Defined Radio (SDR) requires an FIR filter having dynamically programmable coefficients, interpolation factor and lengths which may change according to various standards in a portable computing system. In filters, if the multiplication process is carried out between a single input x and between many constants namely coefficients are known as Multiple Constant Multiplication (MCM).

There are different algorithms to implement such SCM including graph-based algorithm and CSE algorithms. These algorithms are used to obtain an efficient filter hardware architecture by executing the algorithms on a fixed set of coefficients on a highly computing platform. Such MCM designs are not applicable for SDR systems because of the requirement of the highly computationally efficient platform and coefficients are dynamically programmable based on different standards. Some techniques are introduced for designing efficient reconfigurable constant multiplier whose coefficients are changing in real time such as up or down counter [1].BCSE algorithm introduces the concept of eliminating the common sub-expressions in the binary form for designing efficient constant multiplier and can be applicable for reconfigurable filters with low complexity [4].

2. EXISTING SYSTEM

The existing architecture consists of FIR filter and that of RRC filter and RRC filter is designed with n bit multiplier so that any of the constants can be generated.

2.1 FIR filter

Some Finite Impulse Response (FIR) filters play an important role in digital signal processing as their characteristics in linear phase and forward fees implementations make such filters suitable as a building block for the formation of filters yielding high performance. There are different forms for FIR filters such as direct form and transposed form. In hardware, both forms have similar complexity but the transposed form is usually preferred because of high performance and power efficiency. In transposed form since the multiplication of coefficient with the input has a considerable crash on performance as well as complexity because a large number of multiplication stages are needed. Multiplication of filter coefficient with input data is executed by using a shift/add operation where each constant involved in the multiplication is realized using add/subtract and shift operations in MCM operations.

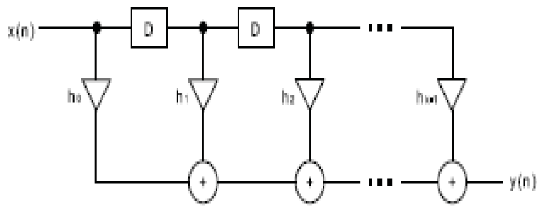

Fig. 1: FIR filter implementation

Add/shift method of constant multiplication is generally known as digit based recoding. This method defines constants as binary values where each “1” in the binary representation of the corresponding constants, it shifts the input variable and adds to the shifted value to obtain the final result. Such techniques do not exploit the sharing of commonly occurring artificial products. It also allows the reduction in a number of operations. The algorithm for MCM falls under two categories. They are Common Sub-Expression Elimination (CSE) and Graph-Based (GB) technique. In such techniques, the input data is processed in parallel and the shift operation requires the use of flip-flops.

2.2 BCSE algorithm

For 3-bit BCS, the partial product generated from each BCS can be summarised as:

$$X * H = \frac{X}{2} + \frac{X}{4} + \frac{X}{8} + \frac{X}{16} + \frac{X}{32} + \frac{X}{64} + \ldots\ldots\ldots\ldots\ldots + \frac{X}{65536}$$

$$X1 = X + \frac{X}{2} + \frac{X}{4}.$$

On substituting the value of X_1, we can reduce the number of partial terms.

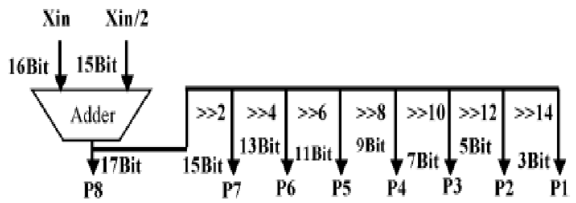

Fig. 2: Block diagram of partial product generator

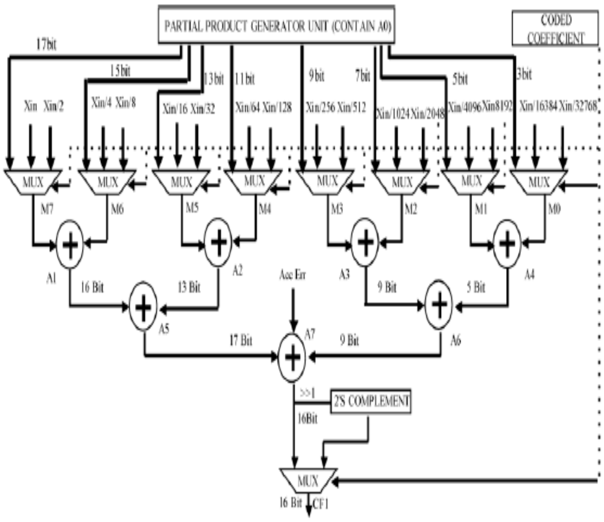

Fig. 3: Reconfigurable constant multiplier using the BCSE algorithm

3. PROPOSED ARCHITECTURE

In this, reconfigurable modified Root Raised Cosine (RRC) filter is designed using reconfigurable constant multiplier designed with BCSE algorithm since it eliminates common partial products thereby makes the multiplication process much faster as compared as to previous works. The proposed architecture is better as compared to existing architecture in terms of delay and power. In such an RRC filter, the coefficients can be dynamically changed in real time. The 2-bit BCSE algorithm is more efficient as compared to the 3-bit BCSE algorithm in terms of area and delay. This architecture has two clocks namely master and slave clock. Master clock is used to sample the output and it operates at a higher rate than other clocks in the architecture. The other clock sources are divided into CLK divided by 4(CLK4), CLK divided by 6 namely CLK6 and CLK divided by 8 namely CLK8 and is used for performing different multiplication processes for data generation. This architecture mainly consists of a block which helps in the generation of data called Data Generation(DG)block, then next block is the coefficient generator(CG) followed by a block called coefficient selector(CS)and accumulation block.DG is used to sample the input data and it is observed that 25,37 and 49 tap filters are obtained with interpolation factors of four, six and eight constituting [25/4]=[37/6]=[49/8]=7 which indicates that seven sub filters are required for multiplication process.CS block is used to provide proper data to final accumulation block and takes input from the CG block. Accumulation block is a block consisting of six adders and six registers. And finally by using this multiplier, RRC filter is designed and performance is compared.

4. RESULTS

A comparison is performed between the proposed RRC filter and that of the FIR filter. Since the RRC filter has much more functional blocks as compared to FIR filter and hence RRC filter is more complex as compared to simple FIR filter.

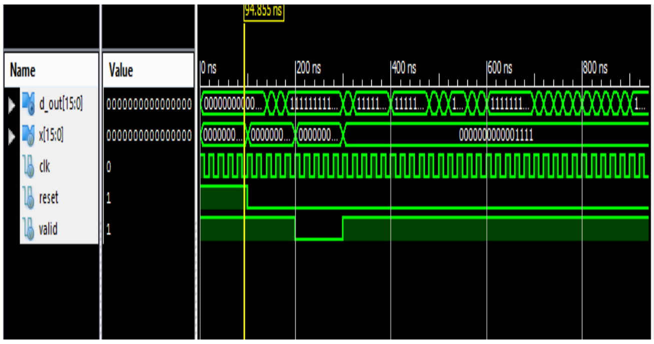

Fig. 4: Output of FIR filter

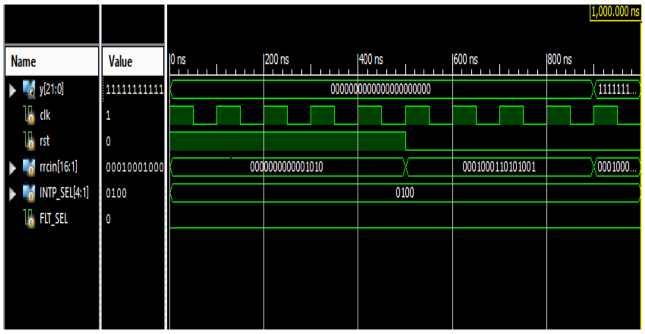

Fig. 5: Output of RRC filter

5. CONCLUSION

An n-bit multiplier can be implemented by using 2 bit or 3-bit BCSE algorithm and an RRC filter is designed by using above-mentioned multiplier. Finally, a comparison is made with RRC filter and that of the simple FIR filter. The power obtained on simple FIR filter is about .128 and that of RRC is .132. As a result, it is obtained that complex RRC design shows better performance as compared to that of FIR filter.

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