INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume 5, Issue 3)
Available online at: www.ijariit.com

Design of Vedic multiplier using Urdhva Tiryagbhyam Sutra

Harsha R.
harsharam147@gmail.com
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

Anilkumar S. R.
sranilkumar94@gmail.com
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

Chandan R.
chandansens36@gmail.com
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

Jeevan Kumar S.
kjeevan984@gmail.com
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

Manjula N.
manjulan6@gmail.com
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

ABSTRACT

The multiplier is a key building block of all processors, which improves the speed of Digital Signal Processor (DSP), a special application in which we need to reduce the time delay. In the proposed method, we design a Vedic multiplier by using a Vedic Mathematics Sutra called Urdhva Tiryagbhyam, which means "vertically and crosswise". Vedic Mathematics is mainly based on 16 Sutras and was rediscovered in the early 20th century. In ancient times in India, people used this Sutra for decimal number multiplications effectively. The same basic concept of the above-mentioned Sutra is extended to the multiplication of binary numbers to make use in the digital hardware system. The computation of partial products in parallel in the Urdhva Tiryagbhyam Sutra increases the speed of the computation process and the processing time is reduced in comparison with the use of inbuilt MATLAB functions. In our proposed multiplier design, the delay for the 4X4 Vedic multiplier is reduced and also the number of transistors is reduced by a large amount compared to the previously proposed design [1].

Keywords— *Vedic mathematics, Urdhva Tiryagbhyam Sutra, Vedic multiplier, Adder, Transistors*

1. INTRODUCTION

Multiplication is an important fundamental function in arithmetic and logic operations. Digital Signal Processing involves operations like frequency domain filtering using Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters and frequency transformations like Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT). Multiplication is essential in all the above operations and performance of the multiplier is important in determining the performance of the entire system. Multiplication dominates the execution time of most DSP algorithms as it is the slowest and most time-consuming element in the system. Thus optimization of multiplier speed and area is a major design challenge and the same can be achieved using Vedic mathematics. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

It is believed that Veda is the storehouse of all knowledge. Vedic mathematics was reconstructed from Vedas by Sri Bharathi Krishna Tirthaji in the early twentieth century. According to his view, Vedic Mathematics is mainly focused on 16 very important principles or word-formulae which are otherwise known as Sutras. The beauty of Vedic mathematics lies in the fact that it reduces cumbersome calculations into very simple means. This is true because Vedic formulae were developed in a natural way in which the human mind works.

2. LITERATURE SURVEY

The traditional multiplication operation is achieved by using the array multiplier. It uses shift and adds an algorithm to compute the product [2]. Here, each partial product is generated by multiplying one bit of multiplier with the entire multiplicand. Such partial products are shifted according to their position, placed one below another and then added to arrive at the final product. Array multiplier uses an array of adders to arrive at the final product [4]. Due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. Also, the implementation of array multiplier needs more area due to more number of gates used. Thus the delay involved in obtaining the final product is large. Ancient Indian Vedic Mathematics gives efficient algorithms or formulae for multiplication which increase the speed of devices [5]. The problem of high carry propagation delay will have been solved by Urdhva Tiryagbhyam which reduces the multiplication of two large numbers to the multiplication of two small numbers [6]. The framework of the proposed work is to be taken from the Urdhva Tiryagbhyam and is further optimized by the use of some general arithmetic operations.

This Sutra was traditionally used for the multiplication of decimal numbers [7]. In our proposed work, we are going to

extend this to the multiplication of binary numbers. Vedic mathematics is the wise choice according to the results shown in [9] and [10] where the delay time and power consumption are considered short and low respectively. Vedic algorithm claims to be the most interesting algorithms of the available ones.

By using the uniqueness of Vedic mathematics, a less number of steps are required for multiplication [3]. Thus the Vedic multiplier will be more power efficient, faster and small in size. It is one of the feasible techniques to be implemented in VLSI design to overcome the power dissipation issue as the number of transistors increased as stated in Moore's law [8].

3. PROPOSED WORK

3.1 Methodology

In this section implementation of Vedic multiplication technique namely "Urdhva Tiryagbhyam – Vertically and crosswise" is demonstrated. This technique is more popular for its high speed working as it generates partial products in a parallel manner and then adding partial products simultaneously. There is reinforcing need for high-speed data processing systems. Vedic multiplier conciliates this need without increasing power consumption. It has less complexity compared to Booth multiplier. Vedic multiplier requires less hardware. Thus Vedic multiplier gives numerous advantages in terms of area, power, delay and complexity.

Reasons for using Urdhva Tiryagbhyam Sutra for the implementation of the proposed Vedic multiplier are as follows: It is found that the processing time when a DSP is implemented using Urdhva Tiryagbhyam Sutra is less in comparison with the processing time obtained when the same DSP is implemented using MATLAB functions. The Urdhva Tiryagbhyam follows a regular and parallel structure making the implementation of the multiplier designed using such Sutra easy on the silicon chip. Parallel structure improves the speed of the multiplier. Another important advantage of using this Sutra is that higher order multipliers (say, a 4×4 Vedic multiplier) can be easily designed if the lower order multipliers (like a 2X2 Vedic multiplier) are already designed and available.

Using this algorithm, the multiplication of two large bit numbers (say, of two 8-bit numbers) is reduced to that of two small bit numbers that are, of two 1-bit numbers.

The above Sutra was traditionally used for multiplication of two decimal numbers. Here, this has been extended to the multiplication of two binary numbers. Since the partial products are generated parallel, the speed with which the final product is obtained increases.

Since the multiplication of two bits is equivalent to a simple AND operation between them, the multiplication can be implemented using simple logic AND gates as shown in figure 1.

3.2 Comparison with the previous work

The block diagrams of Vedic Multiplier proposed previously and that proposed in this paper are shown in figure 2 and figure 3. In previously proposed multiplier of figure 2, to implement the three 4-bit adders, ripple carries adders were used. But the limitation associated with ripple carry adder is that, the sum and carry outputs of a stage will depend on the carry output from the previous stage. This delay adds up for three stages greatly increasing the propagation delay. Thus, in the proposed multiplier of figure 3, ripple carry adders are replaced by carrying look-ahead adders. In the latter adder, the output from a stage depends only on the input carry, Cin and not on the carry outputs from the previous stages. Thus, the propagation delay is reduced in comparison with the ripple carry adders.

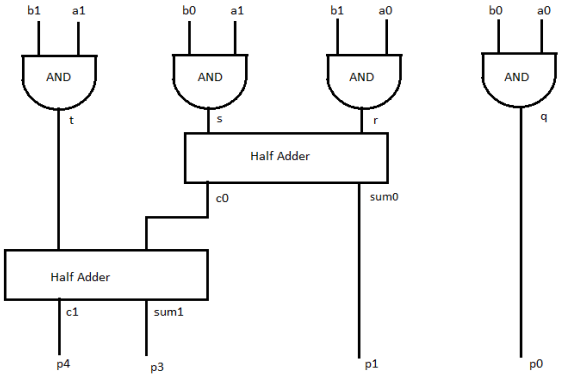

Fig. 1: Block diagram of 2x2 Vedic multiplier

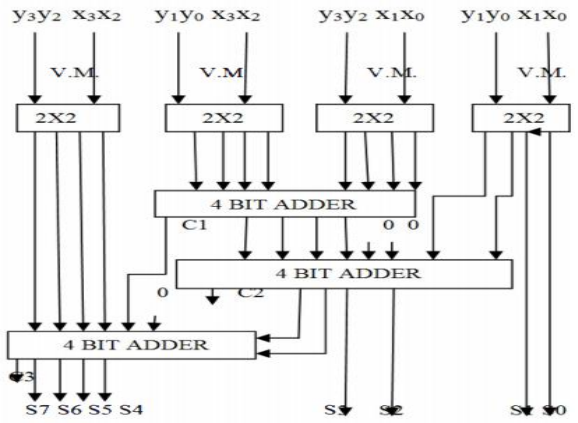

Fig. 2: Block diagram of previously proposed 4x4 Vedic multiplier

The equations for sums and carries of a 4-bit CLA are as shown below:

$$P_i = A_i \oplus B_i$$
$$G_i = A_i B_i$$
$$S_i = P_i \oplus C_i$$
$$C_{i+1} = G_i + P_i C_i$$
$$C_1 = G_0 + P_0 C_{in}$$
$$C_2 = G_1 + P_1 C_1$$
$$= G_1 + P_1 G_0 + P_1 P_0 C_{in}$$
$$C_3 = G_2 + P_2 C_2$$
$$= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{in}$$
$$C_4 = G_3 + P_3 C_3$$
$$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{in}$$

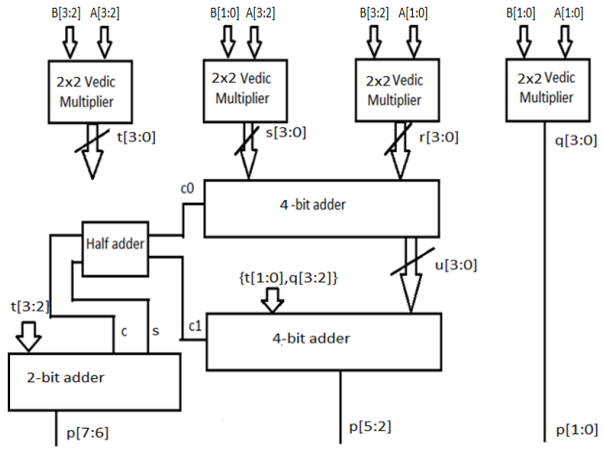

Fig. 3: Block diagram of proposed 4x4 Vedic Multiplier

As an improvement, in our multiplier design, we have made C_{in} as 0, which, in no way, affects the computation of the final product. As C_{in}=0, the last terms in the equations for C_1, C_2, C_3 and C_4 for a normal 4-bit CLA, gets eliminated. This reduces a significant number of logic gates required to implement those last terms. Another optimization introduced in the proposed multiplier is that the use of four 2-bit OR gates needed in implementing the Vedic multiplier, has been replaced by a single 5-bit OR. This reduced the number of transistors needed, from 24 to 12 (50% reduction).

4. ADVANTAGES AND LIMITATIONS OF PROPOSED WORK

To summarize, the advantages of the proposed Vedic multiplier are detailed as: The multiplier proposed in [1] makes use of three 4-bit adders while that proposed in this paper makes use of two 4-bit adders and a 2-bit adder, thus, proving to be efficient in a number of transistors USED and hence the area. The use of CLAs in the proposed multiplier in comparison with the use of ripple-carry adders in the previous counterpart greatly reduces the propagation delay associated with the multiplier. The Urdhva Tiryagbhyam Sutra used computes the partial products in parallel. This increases the speed with which the final product is obtained. The possibility of the algorithm to reduce the multiplication of two large bit numbers to that of two single numbers makes the algorithm simple.

Two limitations of the proposed design are as : The power consumption of the proposed design is somewhat high in comparison with the array multiplier design. Also, design becomes more complex as the size of the numbers to be multiplied increases.

5. APPLICATIONS

The DSP designed by employing the proposed Vedic Multilpier can enhance the speed of its operations like frequency domain filtering, frequency transformations and data compression. Image processing and Multiply and Accumulate (MAC) unit are the other two application areas. Urdhva Tiryagbhyam Sutra can be employed in medical image compression.

6. RESULTS

As an example, consider multiplication of two 2-bit binary numbers b1b0=11 and a1a0=11. The result that we got is p3p2p1p0=1001 which is the expected output.

Table 1: Comparison of results

S. no.	Parameters	4x4 Vedic Multiplier of [1]	Proposed 4x4 Vedic Multiplier
1.	Delay	$208.7x10^{-9}$s	$198.1x10^{-9}$s
2.	Transistors count	904	780
3.	Type of adder used	Slow ripple carry adder	Fast carry look-ahead adder

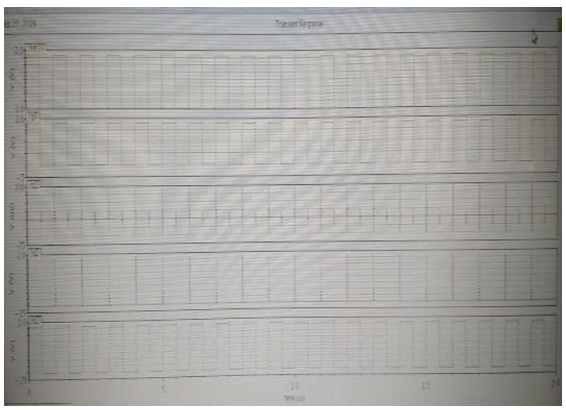

Fig. 4: Simulation Waveforms

7. CONCLUSION

In the traditional array multiplier, which uses a shift-and-add algorithm, the partial products are generated by multiplying entire multiplicand with one bit of multiplier. Its implementation requires a large area due to more number of gates. Also delay in obtaining the final product is large. A multiplier of [1] makes use of ripple carry adders which offer high propagation delay. Thus, a Vedic multiplier is proposed using Urdhva Tiryagbhyam Sutra which is simple and increases the speed by computing partial products in parallel. The use of CLAs reduces the propagation delay involved in the design of [1]. The number of gates is also significantly reduced by making Cin=0 and by using a 5-bit OR gate. Such a multiplier, when implemented in DSPs, is expected to speed up the operations of DSPs involving multiplication.

8. REFERENCES

[1] Raj Kumari, Rajesh Mehra, "Power and Delay Analysis of CMOS Multipliers Using Vedic Algorithm", 1st IEEE ICPEICES-2016.

[2] C. Selvakumari, M. Jeyaprakash, A. Kavitha, "Transistor Level Implementation of an 8-bit Multiplier Using Vedic Mathematics in 180nm Technology", 2016 IEEE.

[3] Dravik Kishor Bhai Kahar, Harsha Mehta, "High-Speed Vedic Multiplier using Vedic Mathematics", ICICCS, 2017.

[4] Devika Jaina, Kabiraj Sethi & Rutuparna Panda, "Vedic Mathematics Based Multiply Accumulate Unit", IEEE 2011.

[5] Ms G. R. Gokhale, Mr S. R. Gokhale, "Design of Area and Delay Efficient Vedic Multiplier Using Carry Select Adder", IEEE 2015.

[6] Sumit R. Vaidya, D. R. Dandekar, "Performance Comparison of Multipliers for Power-Speed Trade-off in VLSI Design", IEEE 2017.

[7] Lee Shing Jie, Siti Hawa Ruslan, "A 2x2 bit Vedic multiplier with different adders in 90nm CMOS technology", AIP Conference Proceedings, 2017.

[8] Sreelekshmi M. S., Farsana F. J., Jithin Krishnan, Rajaram S, Aneesh R, "Implementation of MAC by using Modified Vedic Multiplier" ISSN-2013.

[9] P. Jagadeesh, Mr S.Ravi and Dr Kittur Harish. "Design of High-Performance 64-bit MAC Unit" IEEE-2013.

[10] Shamim Akhter "VHDL Implementation of Fast NxN Multiplier Based on Vedic Mathematics", IEEE-2007.

[11] Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni, "32-bit MAC unit design using Vedic multiplier" ISSN 2013.

[12] B. S. Premananda, S. S. Pai, B. Shashank, S. S. Bhat, "Design and Implementation of 8-bit Vedic Multiplier", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 02, no. 12, pp. 5877-5882, December 2013.

[13] N. H. E. Weste and D. M. Harris, "CMOS VLSI Design", Pearson Publications, 4th Edition, pp. 476- 490, 1998.

