INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume 5, Issue 3)
Available online at: www.ijariit.com

VHDL implementation of acquisition sensor for optical communication terminal

Ashika B. P.
ashikabp9@gmail.com
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

Anuradha Prakash
anuradaprakash@gmail.com
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

Shri. Ravikumar K.
ravikumar.pune@gmail.com
Laboratory for Electro-Optic System (LEOS), ISRO, Bangalore, Karnataka

Girija S.
girija.s@dr-ait.org
Dr. Ambedkar Institute of Technology, Bengaluru, Karnataka

ABSTRACT

This paper presents the development of the Acquisition sensor which is a part of overall Acquisition, Tracking and Pointing (ATP) mechanism for maintaining the Line Of Sight (LOS) between two Optical Communication Terminals (OCT). The ATP mechanism is basically used to align the transmitting and the receiving optical communication terminals which in turn can continuously transmit the data between them. The Acquisition sensor is designed to acquire the LASER image falling on it which is being transmitted by the transmitter terminal and to process this image to calculate the 2-axis angular error. This error is then used to re-position the terminal to maintain the LoS if it is out from the Field of View (FOV) of the transmitter by feeding this data to Tracking and Pointing modules of ATP mechanism.

Keywords— *Optical Communication Terminal (OCT), Acquisition sensor, Line of sight (LoS), Two-axis angular error, Centroid of an image, ATP mechanism*

1. INTRODUCTION

Optical Inter Satellite communication is one of the emerging technologies to meet data transfer requirements at higher rates. This requirement is arising from the space crafts which can handle a large amount of payload data. The main optical carrier of data in the optical inter satellite communication is the LASER beam having high data rate which enhances the communication capacity. The major challenge of Optical Inter Satellite Link is the requirement of precise pointing of optical beam, with high accuracy. To achieve this, Acquisition, Tracking and Pointing (ATP) mechanism is used. This mechanism establishes and maintains the communication link between the two Optical Communication Terminals (OCT). Acquisition sensor module in the ATP mechanism is used for initial pointing, and acquisition of data from the target terminal. During the acquisition phase of OCT, master terminal scans the uncertainty area of the target terminal using a fine laser beam of 20 µrad divergences. The target terminal will wait for the presence of a laser beam on its acquisition sensor. The function of the acquisition sensor is to derive the 2-axis angular error with respect to the Line of Sight (LOS) of OCTs.

2. DESIGNING ACQUISITION SENSOR

Acquisition sensor consists of a SWIR detector, analog processing section and FPGA based digital signal processing section. The function of FPGA is to generate the driving signals for the detector, and process the detector output by generating drive signals to the components in the analog processing block and compute the centroid. Additionally FPGA has to compute the 2-axis angular error for the Tracking sensor module.

The design of the Acquisition sensor using FPGA includes the functionality as shown in fig.1. The basic acquisition component used is the SWIR (Short Wave Infrared) detector. This detector will acquire the data (intensity) from the laser light of wavelength 1550 nm falling on it. The 8-channel analog intensity output produced by the detector is passed on to the analog signal processing circuit.

The analog signal processing circuit includes multiplexers for selecting between the multiple output lines of the detector and the analog to digital converters to convert the analog data into the digital form. The FPGA requires digital data for processing. This

detector acquired intensity value in the digital form along with the address generated by the address generator of the corresponding intensity values are used in the centroid calculation and hence two centroid values of x and y-axes are generated. These two centroid values are further used to compute the 2-axis angular error which is necessary for the Tracking sensor to maintain the LOS.

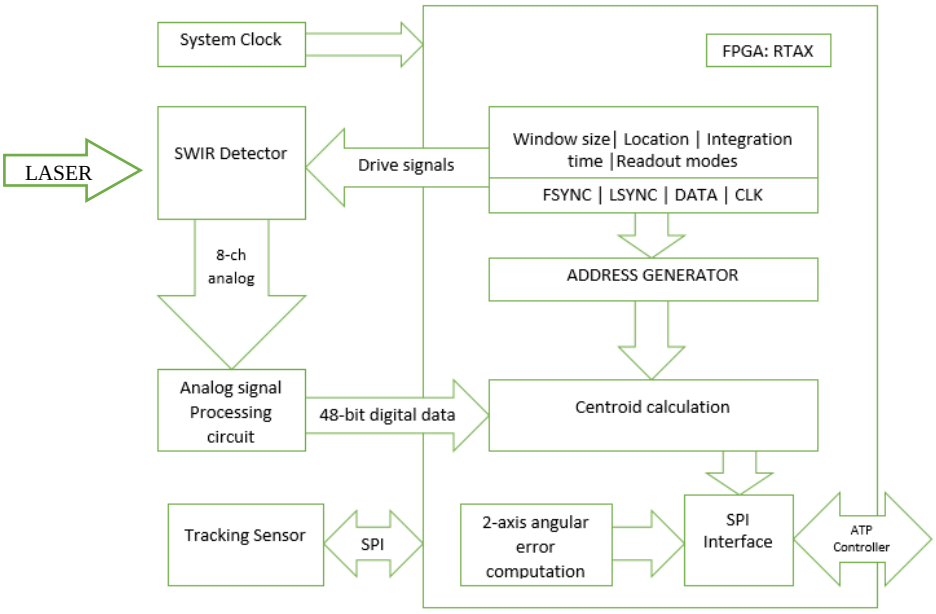

Fig. 1: Functional block diagram

3. FPGA REQUIREMENTS

3.1 FSYNC and LSYNC requirements

- Frame sync signal has to be high for the whole duration of the specified window size, with an additional frame dead time of at least 17 clock cycles. This additional frame dead time is necessary to facilitate the settling of the internal signals of the detector.
- The minimum integration time necessary for gathering enough light intensity is 3 clock cycles.
- The start of line readout is represented using the high of the line sync signal, which is required to be in logical high for a duration of one clock cycle.
- The active pixel output from the detector is only available after two clock cycles of the rising edge of the line sync signal.
- The line sync is held low for as long as all the pixels in that particular line has been read and an additional line dead time of at least 16 clock cycles is to be added before the start of the next line sync.
- During the pixel readout, it is noticed that there is no valid data available after the first line sync. Instead, the data is available at the next line sync and so on up until the N^{th} row readout, whose data will be available at the $(N + 1)^{th}$ line sync.
- For test row readout, another line sync is added at the end of the $(N + 1)^{th}$ line sync, this is used to indicate the start of the next integration.

3.2 MUX select line requirements

- Worst case channel switching time required for this device is 14ns. And the output from this analog switch is available after a delay of 15ns.
- FPGA has to generate the multiplexer selection signal in proper timing synchronization with data output from the SWIR detector, whenever available.

3.3 ADC encode line requirements

- The output from this device is available after a delay of 9 ns.
- FPGA has to generate the ADC encode signal to convert the analog output from the multiplexer to 12-bit digital output.

3.4 Address generation requirements

During the design of this module, one must take into consideration the overall delay caused by the analog signal processing unit, which is up to 118ns. This delay becomes significant throughout computation of the centroid of the system, which is in turn essential while computing the 2 – axis error.

4. FPGA IMPLEMENTATION

This functionality is configured by programming the FPGA using the VHDL hardware description language. FPGA designing for Acquisition sensor module are as follows:

4.1 Clock Divider

The system clock of 24 MHz is being used for designing of the acquisition sensor. This 24 MHz frequency needs to be divided to produce the 12 MHz and 6 MHz frequencies for synchronizing the multiplexers and the SWIR detector respectively. This is done using the clock divider or frequency divider module.

4.2 FSYNC and LSYNC signals for detector

The Short Wave Infrared (SWIR) detector needs four drive signals for its operation. They are FSYNC, LSYNC, DATA and CLK. These signals need to be generated by the FPGA with a pre-defined set of constraints. To generate these signals, the FPGA will get the initial data from the ATP controller via an SPI interface. These signals from the FPGA will trigger the detector to start its reading process in order to acquire the intensity from the laser light falling on it. Once the detector initiates its reading process, it will produce intensity as an analog output which is then fed to the signal processing circuit.

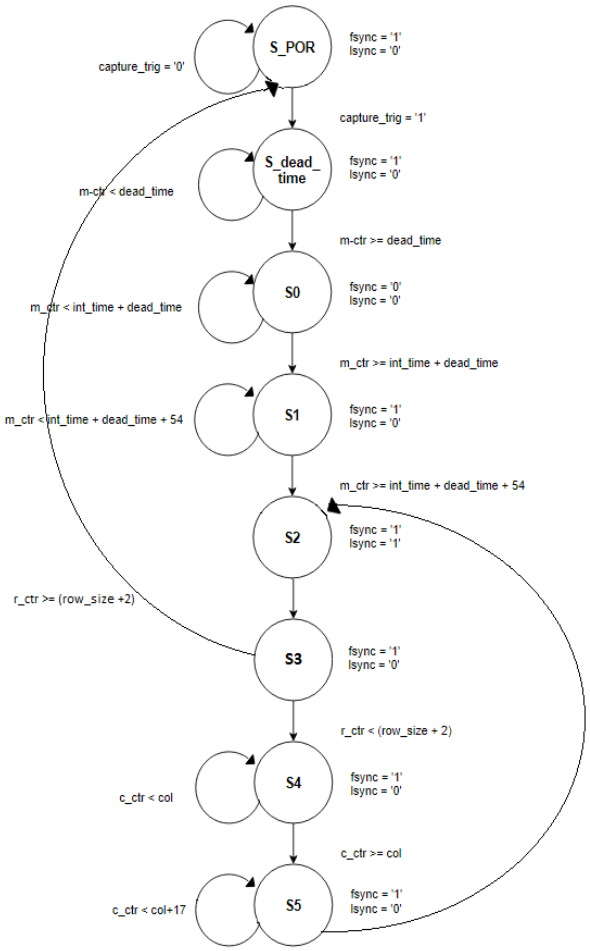

Fig. 2: Generation of FSYNC and LSYNC using FSM

In the designing process, we have chosen Integrate Then Read (ITR) mode of operation where the screen is exposed to laser light for acquiring the data in a defined integration time duration. The generation of FSYNC and LSYNC signals for the detector is done using the FSM as shown in figure 2.

The generations of FSYNC and LSYNC signals are done according to the designing constraints as mentioned in section 4 of this paper. The generation of these signals internally depends on the values of WAX, WAY, WSX, WSY, integration time and OM.

The FSYNC signal will be low during integration time and will be high throughout the frame. The LSYNC signal is for reading row by row data. This signal is defined to start with an initial time delay of 54 clock cycles. Then while reading one row of data, this signal will be high for one clock cycle and remain low till all the pixels in that particular row is being read. The Output Mode (OM) chosen is 8 and hence we get 16 intensity values at any given point of time. The output signals are produced in such a way that, the data readout is synchronized with that of the address generation module.

4.3 Detector control

The detector requires eighty bit control register values to perform the required operation. This signal is defined as per the requirements and the control register bits which are transmitted from the ATP controller to the FPGA via the SPI and these data bits are stored in the registers for other necessary computations taking place within the FPGA. All the eighty bits of control information is transmitted to the detector serially, which is called the DATA signal.

4.4 Drive signals for MUX and ADC

The FPGA will generate the SELECT signal for multiplexer and ENCODE signal for ADC. These signals are generated keeping in mind the switching delays that occur within these components.

4.5 Address generation block

During the design, care has been taken when generating the x and y coordinate addresses of the pixels that are being read by the detector using the LSYNC signal. The addresses need to be generated correspondingly when a pixel is read. During which we

consider the overall delay that is produced before which the digital data (intensity values) are available to the FPGA for the centroid computation. This module is implemented using the FSM as shown in the figure below.

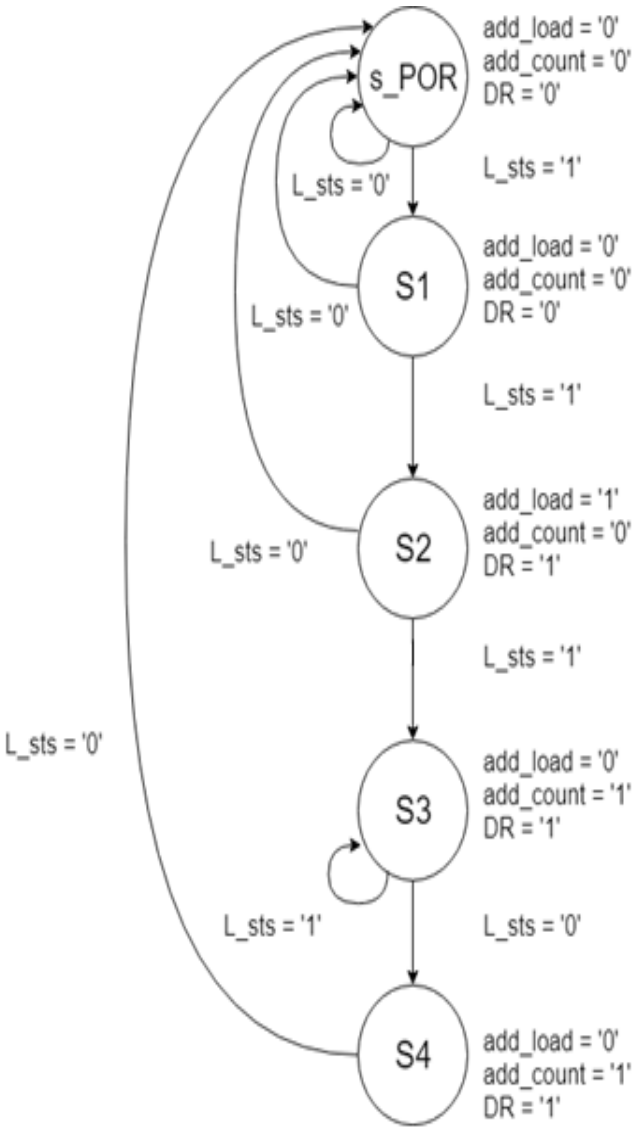

Fig. 3: Implementation of Address Generation using FSM

Where add_load signal represents address load operation, using the formulae,

$$\text{Start address } X = (WAX * 32)$$

$$\text{Start address } Y = (WAY * 4)$$

While add_count signal represents whether are not the computed addresses should be incremented by 1 or 7 based on the value of the MUX select line.

4.6 Centroid Computation Block

The 12-bit digital intensity value from four ADCs along with the address generated by the address generation block is being fed to the centroid computation block. The laser light acquired by the sensor on converting the intensity to its digital format we deal with a grey scale image. Greyscale images are those images containing only shades of grey where each pixel holds only the intensity values of the acquired image. In order to calculate the centroid of a grey scale image, we compute the weighted average of the pixels grey value using the formulae,

$$Cx = \sum xi.pi \,/\, \sum pi$$

$$Cy = \sum yi\,.pi \,/\, \sum pi$$

Where xi represents the x-axis address of the pixel, yi represents the y-axis address of the symbol and pi represents the intensity level acquired from the corresponding pixel.

A computation involving multiplication and division of this module may lead to a larger delay than expected. In order to reduce the delay, the same computation is implemented using the inbuilt booth array multiplier module for multiplication and designed a division module for division operation based on restoring algorithm. The flowchart representing the implementation of the restoring algorithm is as shown below.

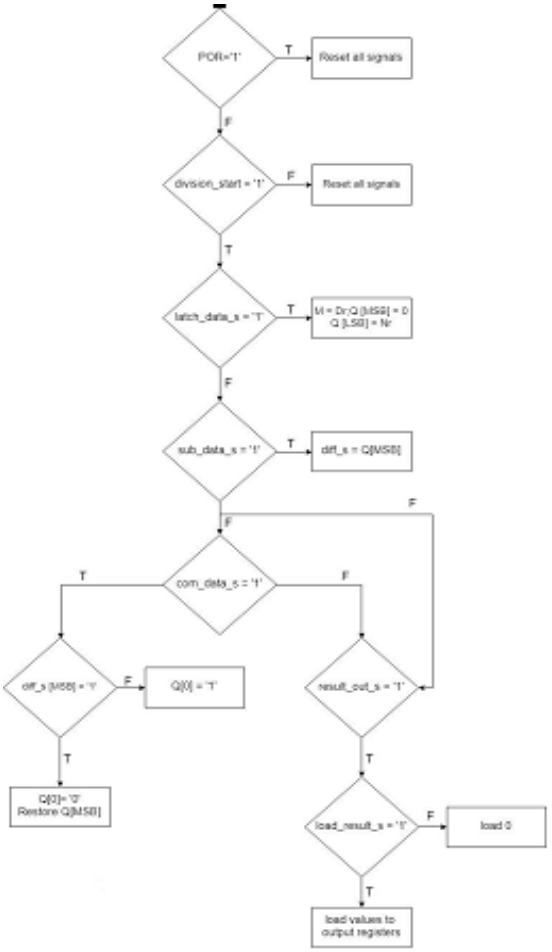

Fig. 4: Logical Implementation of Restoring Algorithm using Flow Chart

4.7 Two-axis error computation block

The final function performed by the Acquisition Sensor is computing the two-axis angular error from the centroid values transmitted to it. The purpose of this error estimation is to position the satellites in the line of sight of the detector to facilitate the better and more accurate acquisition of data. These angular errors are calculated using the following formulae,

$$\theta = tan - 1\,(Cx\,/\,f)$$

$$\varphi = tan - 1\,(Cy\,/\,f)$$

Where Cx and Cy are the x-axis and y-axis centroids respectively and f is the focal length. The block diagram below represents the inputs to this module along with the outputs.

This is implemented using an IP-core called the Cordic Core. Cordic is also called as the Volder's algorithm is a very simple algorithm employed in order to calculate trigonometry and hyperbolic functions. This algorithm is a digit by digit algorithm converging with only one digit every iteration. This algorithm is used typically when the hardware cannot be realized for the above-mentioned functions hence, it is used, as the only operation it requires in order to carry out multiplier functions would be addition subtraction bit shift and table lookup. The CORDIC algorithm is preferred over other approaches as it is relatively faster or when the number of gates used to implement the function needs to be reduced.

5. CONCLUSION

In this paper, we have implemented the VHDL code required for realizing the Acquisition sensor. This includes the calculation of centroid, which is further used to compute the 2-axis angular error. The 2-axis angular error will be used by the Tracking sensor to re-locate or re-position the receiving optical terminal in such a way that the LOS between two OCTs is maintained.

6. REFERENCES

[1] OpticalInter-Satellite Communication Operational (https://ieeexplore.ieee.org/document/5680175/)
[2] A Survey on Acquisition, Tracking, and Pointing 0Mechanisms for Mobile Free-Space Optical Communications (https://ieeexplore.ieee.org/document/8288586/)
[3] Optical Inter - satellite Communication (https://ieeexplore.ieee.org/document/5475229/)

