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Analysis of 5 stage pipelined operations of ARM 32/64 bit

Abinash Ghosh
abhiabinash1997@gmail.com
Chaibasa Engineering College, Kelende, Jharkhand

Sujata Kumari
sujataheena1997@gmail.com
Chaibasa Engineering College, Kelende, Jharkhand

Neha Pan
nehanoa@gmail.com
Chaibasa Engineering College, Kelende, Jharkhand

Sangita Kumari
sangita771997@gmail.com
Chaibasa Engineering College, Kelende, Jharkhand

Aditi Kumari
aditi6101998@gmail.com
Chaibasa Engineering College, Kelende, Jharkhand

Tathagata Roy Chowdhury
tathagatamtech13@gmail.com
Chaibasa Engineering College, Kelende, Jharkhand

ABSTRACT

In this paper, we have introduced an analysis of the architecture of the ARM processor. This processor includes some concepts of memory diagram, relative performance, and pipeline stages. Here we have briefed about the introduction, block diagram, pipeline organization, and various stages of pipelining, features and application of ARM processor. And we have also included a comparison between different ARM processor and architecture.

Keywords— *Pipeline, ARM processor, Pipeline architecture, Stages of pipeline*

1. ARM PROCESSOR INTRODUCTION AND BLOCK DIAGRAM

The Arm processor was originally developed Acorn computer limited of Cambridge, England between 1983 and 1985. It was the first RISC microprocessor developed for commercial use. In 1990 ARM limited was established as a separate company. It is established as a market leader for low power and cost-sensitive embedded application. Later joint venture was co-founded by Acorn and Apple designating it as advance RISC machine.

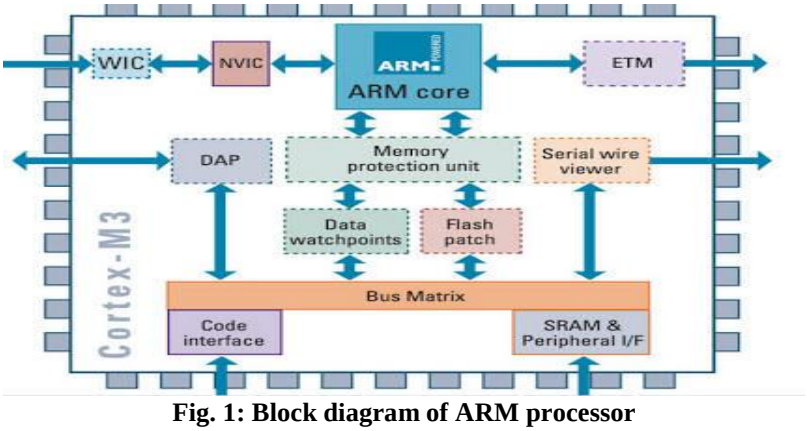

Fig. 1: Block diagram of ARM processor

2. ARM PIPELINING ORGANIZATION

2.1 5-Stage pipeline

- Breaking instruction execution down into five component rather than 3 reduces the maximum work which must be completed in one clock cycle.
- Hence allows a higher clock frequency to be used.
- Instruction memory is also redesigned to operate the higher clock rate.
- This is implemented in the ARM9 CPU.

Various Stages: Fetch, Decode, Execute, Memory Access, Write Back.

2.2 Pipelining stages

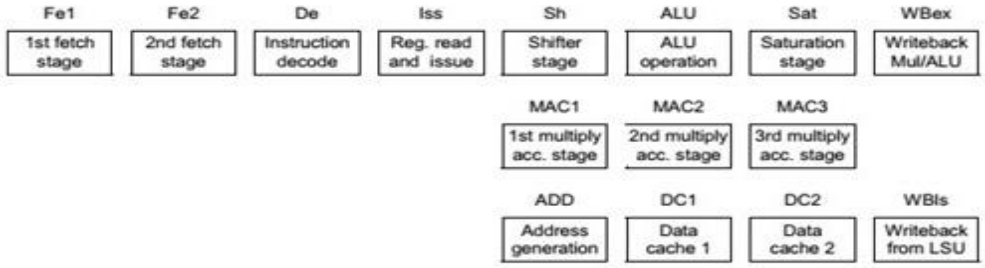

Fig. 2: CPU pipelining stages: Different stages of ARM

The pipeline stages are:

Fe1	First stage of instruction fetch and branch prediction.
Fe2	Second stage of instruction fetch and branch prediction.
De	Instruction decode.
Iss	Register read and instruction issue.
Sh	Shifter stage.
ALU	Main integer operation calculation.
Sat	Pipeline stage to enable saturation of integer results.
WBex	Write back of data from the multiply or main execution pipelines.
MAC1	First stage of the multiply-accumulate pipeline.
MAC2	Second stage of the multiply-accumulate pipeline.
MAC3	Third stage of the multiply-accumulate pipeline.
ADD	Address generation stage.
DC1	First stage of Data Cache access.
DC2	Second stage of Data Cache access.
WBls	Write back of data from the Load Store Unit.

Fig. 3: Description of all instructions

2.3 Typical pipeline operations

This is our pipelining operation where we can perform various operations on each instruction, the operation includes ALU and Multiply operation together where each stage of pipelining relate with the 5 phases of instruction execution.

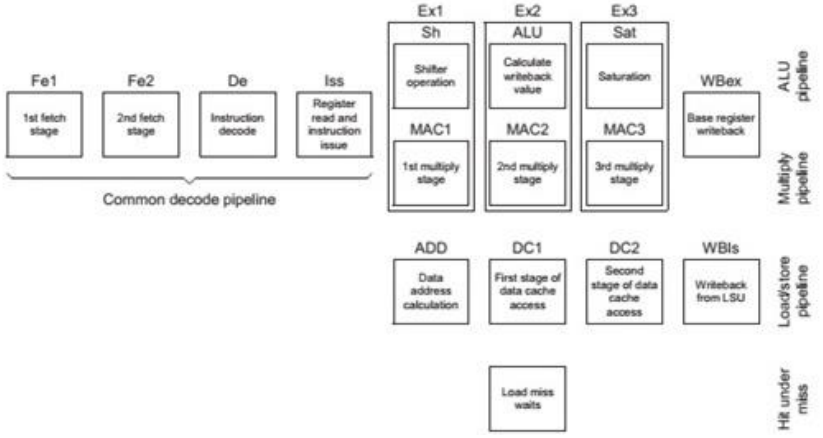

Fig. 4: Typical Pipeline operation in different stages.

Here we include the ALU operation and multiply operation together in our analysis.

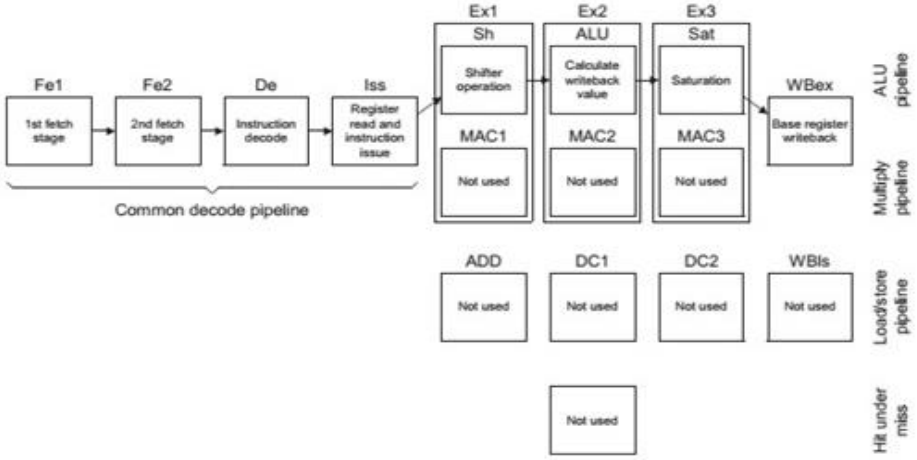

Fig. 5: ALU operation

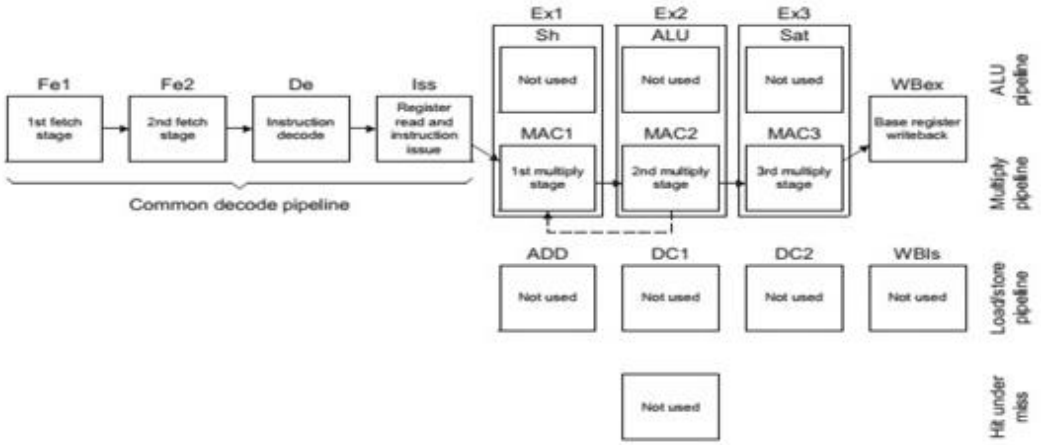

Fig. 6: Multiply operation

3. FEATURES OF ARM PROCESSOR

3.1 Features of ARM Processor

- ARM is a 32-bit instruction set architecture.
- Gadgets such as smartphones, set-top boxes, digital television, and digital cameras use ARM processors.
- It costs low and consumes low power.
- It is found user-friendly with all types of operating system i.e. Symbian, Palm, Windows, and Android.
- ARM processors are high speed as well as smaller in size.

3.2 Features inherited from risc design

- Load-store architecture.
- Fixed length 32-bit instructions.
- 3-address instruction format.
- Simplicity

4. DIFFERENT MODES OF ARM PROCESSOR

4.1 Architecture of ARM processor

- An ARM processor consists of 31 general purpose 32-bit register.
- R0-R15 are the visible registers.
- Special registers such as R14 acts as link register (LR), R15 acts as Program Counter (PC) and R13 acts as a Stack Pointer.

4.2 ARM Processor modes of operation

There are various modes of operation categorized as:

(a) User mode
(b) Prevailed mode
(c) Exception mode

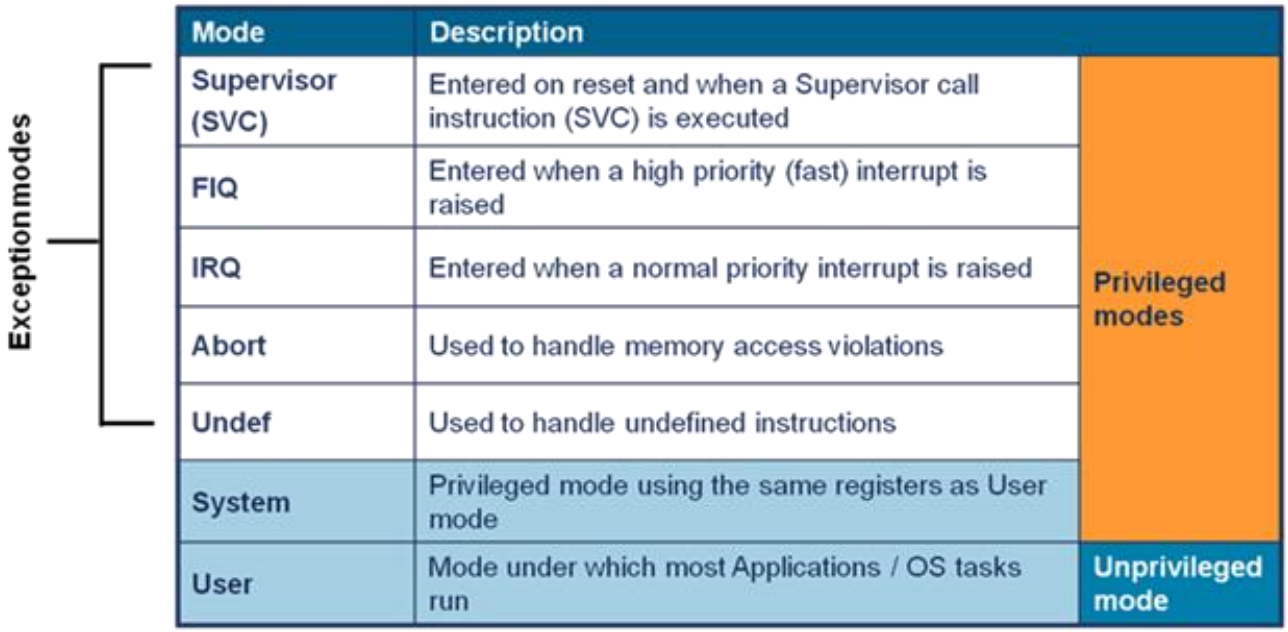

Fig. 7: ARM processor mode of operations

5. COMPARISON OF DIFFERENT ARM PROCESSOR

Table 6: Comparison of Cortex ARM processor

Cortex-A8:	Cortex-R4:	Cortex-M3:
Architecture v7A	Architecture v7R	Architecture v7M
MMU	MPU (optional)	MPU (optional)
AXI	AXI	AHB Lite & APB
VFP & NEON support	Dual Issue	

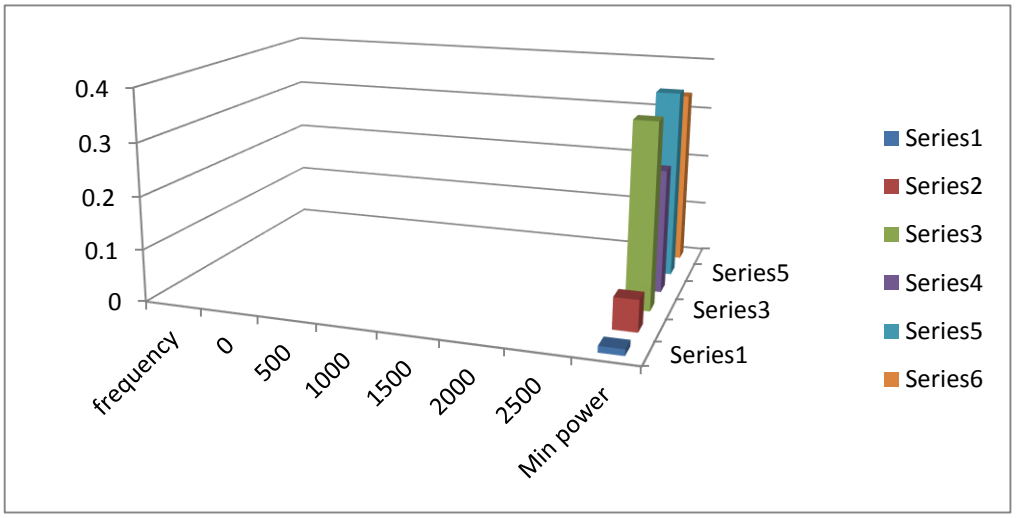

Fig. 8: Relative Performance of different processor family

6. ADVANTAGE AND DISADVANTAGE

6.1 Advantage of using an ARM processor

- They perform one operation at a time and can work faster.
- They are designed with such features that it consumes less power.
- Improved memory protection schema.
- Saving in cost, physical space, and space on the circuit board.
- The availability and applications support has also made the user choose ARM Processor.

6.2 Disadvantage of using an ARM Processor

- Some arm processors have limited clock frequencies which are why speed and memory bandwidths are limited in case.
- It is not binary compatible with x86, which means windows can't be run.
- The scheduling of instruction marks debugging difficult.
- The performance of this processor greatly depends on the execution.

7. CONCLUSION

ARM is the standard processor architecture, that is used in embedded systems from several years till now and it is going to dominate in the future also. Even though we have come across and worked on current processor architecture which claims to solve some of the interlocking problems in the ARM pipeline but not seen much in this front.

According to our study, we can say that the ARM core is really dominating the processor/controller market. ARM is constantly striving hard to produce cores with lowest power consumption, smallest footprint catering to various application segments. The major microcontroller/processor vendors such as **TI, freescale, Microchip, renasis** etc. have a range of ARM core-based controllers and they are dominating the embedded market.

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