Low power design of 4-bits counter at circuit and system level of abstraction

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ABSTRACT

This paper presents a design of Low power 4 bits Counter at circuit and system level of abstraction using Cadence Virtuoso and Xilinx ISE 14.7 respectively. The laboratory work described includes the CMOS based transistor level design and implementation of the counter using back end and front end tools respectively. The functionality of the design has been simulated and tested using Cadence Virtuoso for back end simulation and synthesized using plan ahead and is implemented on ArtixTM-7(family), with device xc7A100TTM. Power calculation has been done at 100 MHz clock frequency for the 1.8V supply voltage.

Keywords—Low power, Sequential circuits, Flip-flop, Counter, FPGA

1. INTRODUCTION

The development of ICs played a significant role in solving the problems of logic circuits. These ICs are fabricated to place a large number of transistors and on a single chip. Thus with the miniaturization of circuitry and with the increase in the demand for portable applications, the concern is expanded mainly towards the most challenging issue of power efficiency VLSI circuit design, especially with on-chip devices.

One of the major aspects of digital systems is analysis and design of sequential circuits. In sequential circuits, the output depends on present input as well as on the present state of circuit i.e. on the past inputs also. Thus the concluding remark about sequential circuits is that they have memory. In order to make these circuits synchronous, a clock pulse is inserted along with the input signal to make sure that state transition can take place at that instance only. Thus, the clock signal does not carry any useful information and is one of the main cause of dynamic power dissipation according to the mathematical equation:

\[ P_D = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f \]  

In the proposed design we are mainly concerned about the dynamic power consumption in electronic devices as the major part of this dissipation is due to system’s clock signal in which there will be 30-70% of total dynamic power consumption. As the FPGAs are absolute new intellect class of ICs they are used to amend digital designs. FPGAs are cost-effective and flexible for low volume applications since the user can freely change the function of its programmable logic blocks and the connection of programmable switch blocks. Despite these advantages, FPGAs have a large power overhead compared to custom VLSI.

Due to the above-mentioned characteristics of FPGAs, the design of the counter is implemented using ArtixTM-7(family), with device xc7A100TTM.

2. DESIGN OF 4-BITS COUNTER USING JK FLIP-FLOP

The counter is a sequential circuit that passes through a definite sequence of states when input clock pulse is given to the counter. The input clock pulse may be a clock pulse or some external signal generated by other circuitry. The basic building block of the counter is a flip-flop. A counter can be designed using a D flip-flop for achieving high-speed operations. A flip-flop is a 1-bit memory element which stores 1-bit data that stays at one binary as long as power is given to the circuit or until input changes its state. Various flip-flops are different from each other in terms of input they have and how input affects the binary state. D flip-flop is called a transparent flip-flop. It has two inputs D and a clock pulse. D input is sampled when CP=1 and if D=0 output Q goes to 0 and the circuit switches to clear state. In the design of the counter, D flip-flop is chosen because it uses less number of transistor counts. Design of D FF consists of 4 two inputs NAND gates and one inverter. All the NAND gates are connected in such a manner that overall delay of the circuit is low.

JK Flip Flop is chosen for the counter for the following reasons:

- A JK FF includes both set and reset feature which can also be synchronized with the clock. A T FF input to both J and K inputs.
- JK FF is designed using a positive edge triggered D FF as they are easy to design and less complex.
JK FF design consists of 2 inputs AND gate one inverter one or gate and one D flip-flop. For designing counter 4 JK FF and 3 two-input AND gates are connected. The input to first FF is T, a DC signal applied externally, both J and K inputs are connected to the same input to make T FF, another input is clock pulse. The input to AND gate is the output of FF and again is used as input of following flip-flops so that state of next flip-flop changes only when all the previous FF are in the state.

**Fig. 1:** RTL schematic of 4-bits counter

**3. FLOW CHART OF PROPOSED WORK**
Following steps are followed while designing and implement a counter at the front end.

**4. RESULTS**
Simulation results of 4 bits counter are given in figure 4 as below:

**Fig. 4:** Transient response of 4 bits counter

The designed 4 Bits counter for the front end is implemented using the VHDL coding, simulated using Xilinx ISE 14.7 simulator. Figure 5 shows the schematic diagram using Schematic- L editor and layout shown in figure 6 is designed in Virtuoso Layout- XL.
Simulation results given in figure 4 shows that this architecture consumes a very less dynamic power of 69.218 µW and 96.98 µW pre and post-layout simulation respectively that is at back-end design whereas, from X-Power analyzer results as given in table 3 on-chip dynamic power consumption is 1.11 mW.

Table 1: Pre-layout power analysis results (µW)

<table>
<thead>
<tr>
<th>Components of Power</th>
<th>Power (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Power</td>
<td>1.88</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>69.218</td>
</tr>
<tr>
<td>Total</td>
<td>71.10</td>
</tr>
</tbody>
</table>

Table 2: Pre-layout power analysis results (µW)

<table>
<thead>
<tr>
<th>Components of Power</th>
<th>Power (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static Power</td>
<td>1.89</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>96.98</td>
</tr>
<tr>
<td>Total</td>
<td>98.87</td>
</tr>
</tbody>
</table>

Table 3: Power calculations 4 Bits Counter (in watts)

<table>
<thead>
<tr>
<th>Components of Power</th>
<th>Power (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock</td>
<td>0.05</td>
</tr>
<tr>
<td>Logic</td>
<td>0.001</td>
</tr>
<tr>
<td>Signal</td>
<td>0.01</td>
</tr>
<tr>
<td>IOs</td>
<td>1.04</td>
</tr>
<tr>
<td>Static</td>
<td>82.16</td>
</tr>
<tr>
<td>Dynamic</td>
<td>1.11</td>
</tr>
<tr>
<td>Total</td>
<td>83.27</td>
</tr>
</tbody>
</table>

5. CONCLUSION
From the experimental results, it can be concluded that power consumption at the RTL level increases with the increase in clock frequency and switching activity. Power calculations are performed by implementing the 4 Bits counter on Artix™-7(family) FPGA, with device xc7A100T™ and there is approximately a 30% rise in power dissipation from pre-layout to post-layout simulation. It has been also found that there is a significant percentage rise of 90% from the back end to front end implementation of the proposed design. Hence conclusion can be made that there must be some power reduction techniques used at the system level of abstraction i.e., before the implementation of final design into FPGA.

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7. REFERENCES