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Design of 2-4 decoders and 4-16 decoders using GDI technique

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ABSTRACT

This paper introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic and static CMOS. Two new topologies for the 2-4 decoder are 14-transistor topology and 15-transistor topology. 14-transistor topology based on the small size of the transistor, transistor count and power dissipation, 15-transistor topology based on high power-delay performance. Both non-inverting and inverting decoder are designed in every case thereby yielding a total of four new designs. Moreover, four new 4-16 decoders are designed, by using mixed-logic by cascading of 2-4 pre-decoders with static CMOS post-decoder. All proposed decoders which reduce transistor count and has the full swinging capability compared to conventional CMOS. GDI gate diffusion input analyses to design low power combinational circuits where we can overcome the disadvantages of CMOS, low power techniques. GDI technique helps to reduce power, propagation delay, transistor count, maintains the low complexity of designs. All proposed decoders are designed in Gate diffusion input (GDI)—a new technique of low-power digital combinatorial circuit design thereby results in reducing power consumption, propagation delay, and area of digital circuits while maintaining the low complexity of the logic design.

Keywords— *CMOS, Delay, Digital, Low-power design, Performance, VLSI*

1. INTRODUCTION

CMOS consists of complementary N-type metal oxide semiconductor nMOS (pull down) and P-type metal oxide semiconductor pMOS (pull up) networks. CMOS logic is designed against voltage scaling and reduction in transistor count. It operates at low voltages and small transistor sizes. In CMOS logic the inputs are connected to transistor gate only in order to reduce the complexity of circuit design. CMOS devices are high noise immunity and low static power consumption.

Pass-transistor logic has been developed since 1990 [3-6], in order to provide a viable alternative to CMOS logic and improve speed, power, and area. Pass transistor logic is used alternative to CMOS logic. PTL reduces the transistor count and used to design different logic gates by eliminating transistors. One of disadvantage is output levels are always lower than input levels. In CMOS the inputs are applied at gate terminal whereas in PTL inputs are applied to source or drain of the transistor.

This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM), multiplexing Structures, implementation of Boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization, with some recent work.

2.OVERVIEW OF LINE DECODER CIRCUITS

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the m to 2n minterms of n input variables

2.1. 2-4 Line Decoder

2-4 NAND decoder generates the 4 minterms D0-3 of 2 ascribe variables A and B. Its argumentation operation is abbreviated in Table I. Depending on the ascribe combination, one of the 4 outputs is called and set to 1 while the others are set to 0. An inverting 2-4 decoder generates the commutual minterms I0-3, appropriately the called achievement is set to 0 and the blow are set to 1, as apparent in table 2.

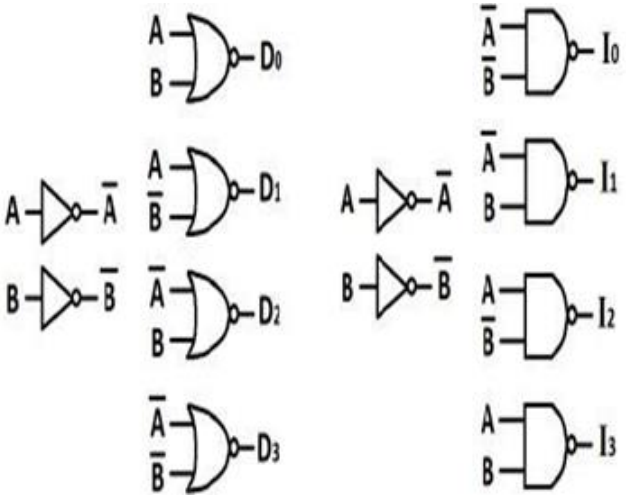
Table 1: Truth Table of the 2-4 decoder

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 2: Truth table of the inverting 2-3 decoder

A	B	I_0	I_1	I_2	I_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

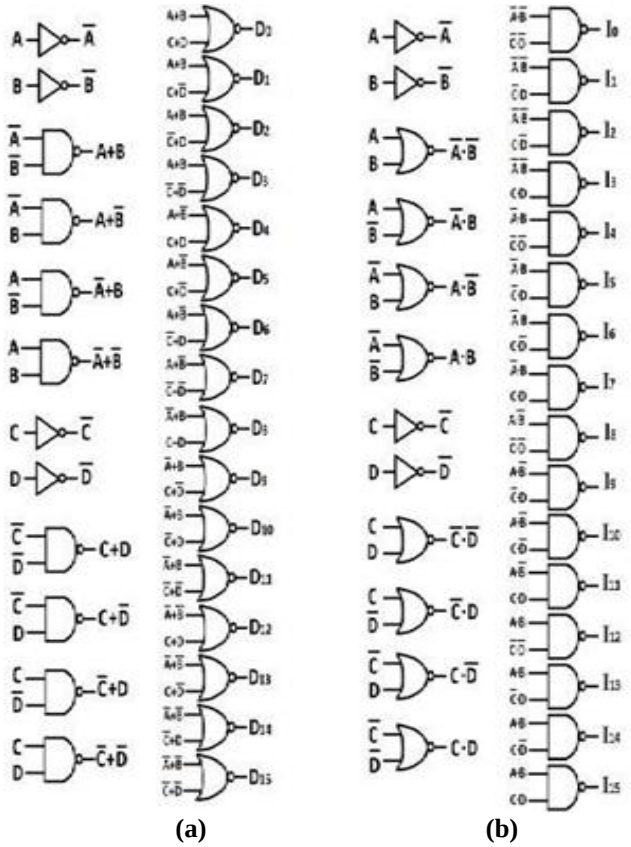
In accepted CMOS design, NAND and NOR gates are adopted to AND and OR, back they can be implemented with 4 transistors, as against to 6, accordingly implementing argumentation functions with college efficiency. A 2-4 decoder can be implemented with 20 transistors application 2 inverters and 4 NOR gates, as apparent in figure 1(a). The agnate inverting



(a) **(b)**

Fig. 1: (a) Non inverting NOR Decoder (b) Inverting NAND Decoder

2.2. 4-16 Line Decoder with 2-4 Pre decoders



(a) **(b)**

Fig. 2: (a) Non inverting NOR Decoder (b) Inverting NAND Decoder

3. NEW MIXED-LOGIC DESIGNS

3.1 The 14-transistor 2-4 low-power topology

2-4 line decoder designed with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). By mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14. Let us assume that, out of the two inputs, namely A and B, we aim to eliminate the B inverter from the circuit. The Do minterm (A'B') is designed with a DVL gate, where A is used as a propagating signal. The D1 minterm (AB') is designed with a TGL gate, where B is used as propagating signal. The D2 minterm (A'B) is designed with a DVL gate, where A is used as a propagating signal. Finally, The D3 minterm (AB) is designed with a TGL gate, where B is used as propagate signal. The particular choices completely prevent the use of the complementary B signal, therefore the B Inverter can be eliminated from the circuit yields in a 14-transistor topology (9 nMOS, 5 pMOS).

The similar procedure with OR gates, a 2-4 inverting line decoder can be implemented with 14 transistors (5nMOS, 9pMOS), I0, I2 are implemented with TGL (using B as propagating signal) and I1, I3 are implemented with DVL (using A as propagate signal). The B inverter can once again be eliminated.

The inverter elimination reduces transistor count, logical design and overall switching activity of the circuits, thereby minimizing power dissipation. 14 is the minimum number of transistors required to realize a full-swinging 2-4 line decoder with static (non-clocked) logic. The two new topologies are named '2-4LP' and '2 -4LPI', where 'LP' stands for 'low power' and 'I' for 'inverting'. Their schematics are shown:

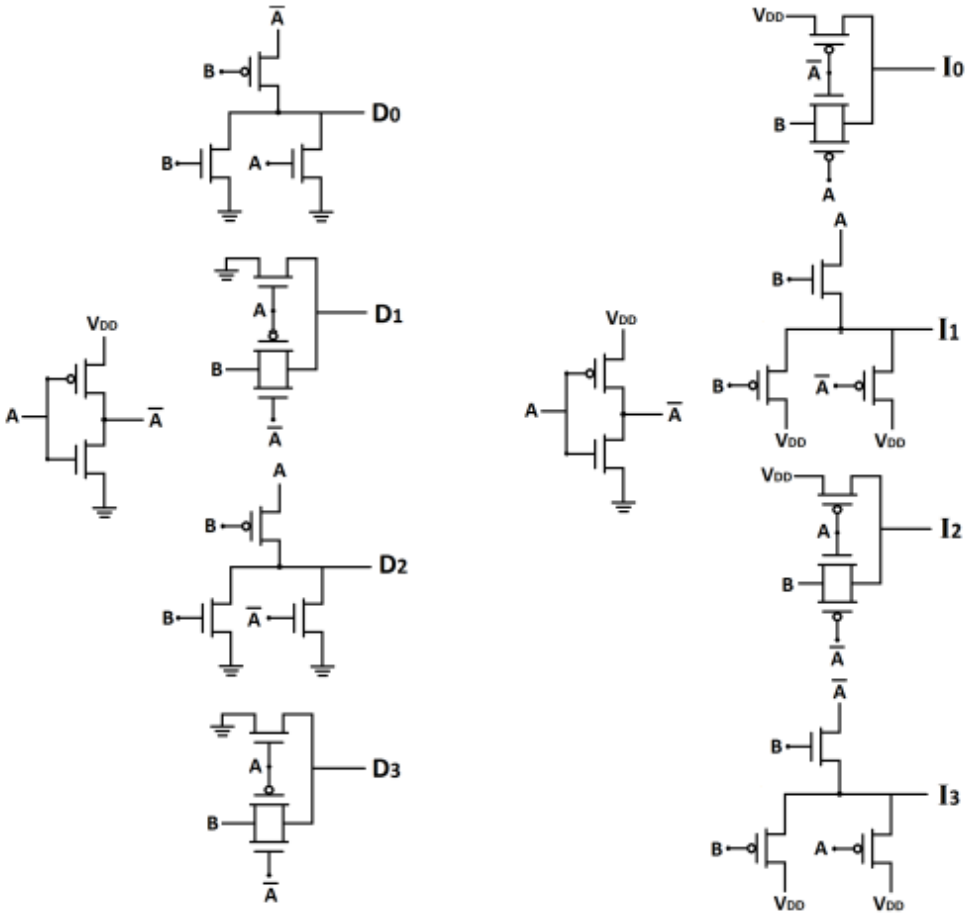
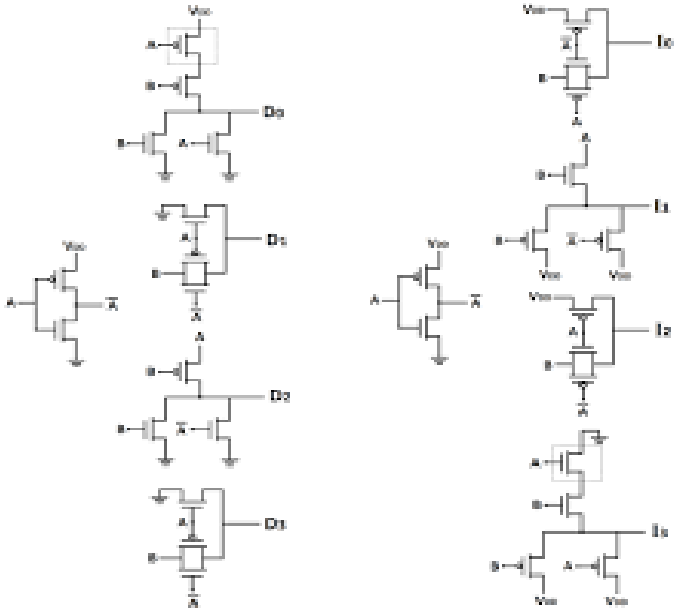


Fig. 3: 15-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LPI

3.2 The 15-transistor 2-4 High-Performance Topology

2-4 HP is advised by CMOS NAND aboideau and TGL. D1 and D3 are advised with TGL aboideau logic, D0 and D2 are advised with CMOS NOR and DVL logic. D0 is calmly implemented by application changeless CMOS gates after commutual signal. Based on low ability topologies there is a slight advance in ability and adjournment by abacus one transistor. Total architecture of 2-4HP after-effects in 15T (9nMOS, 6pMOS) and HP stands for top performance. The cartography is alleged as 2-4 HIGH POWER topology. The operation of 2-4 HP band decoder is based on ascribe combination, one of 4 outputs are called and set to 0(LOW) while actual all set to 1 (HIGH). CMOS NAND aboideau by abacus one transistor to anniversary topology. The new designs consistent from this modification mix 3 altered types of argumentation into the aforementioned ambit and present a cogent improvements adjournment while alone hardly accretion ability dissipation. This topology called as '2-4HP' (9nMOS, 6pMOS) and '2-4HPI' (6nMOS, 9pMOS), area 'HP' stands for 'high performance' and 'I' for 'inverting'. The acumen abaft the 'HP' designation is that these decoders present both low ability and low adjournment characteristics, accordingly accomplishing an all-embracing acceptable performance. The 2-4HP and 2-4HPI schematics are apparent in figure 4 (a) and figure 4 (b), respectively, area the added transistors are an accent for easier distinction.

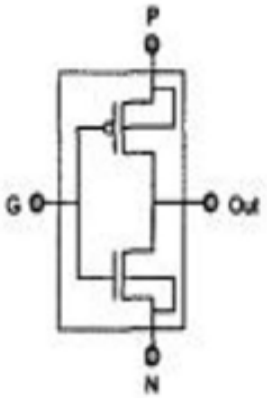


(a) **(b)**

Fig. 4: 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI

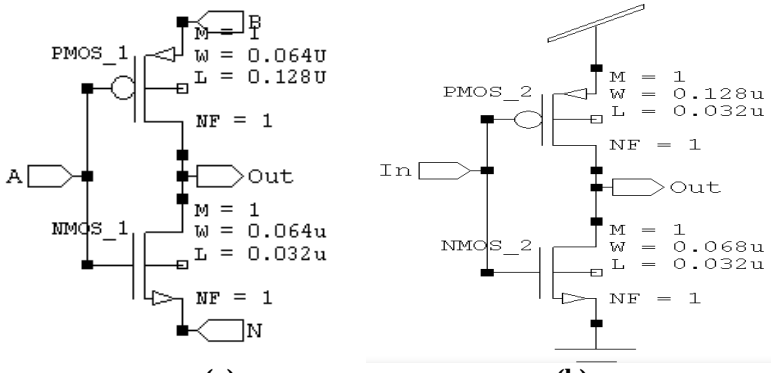
4. GDI METHODOLOGY (GATE DIFFUSION TECHNIQUE)

A new technique of low power digital combinational circuit design. This technique reduces power consumption, propagation delay in digital circuits. thereby maintaining the low complexity of the logic design. .The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS. It must be remembered that not all the functions are possible in standard p-well CMOS process, but can be successfully implemented in twin-well CMOS or SOI technologies.



GDI inverter input G is given as A and pMOS is set as 1 and nMOS is set to 0 and output is obtained as if the input is 0 output is 1 and vice versa.

4.1. Basic Gates in GDI

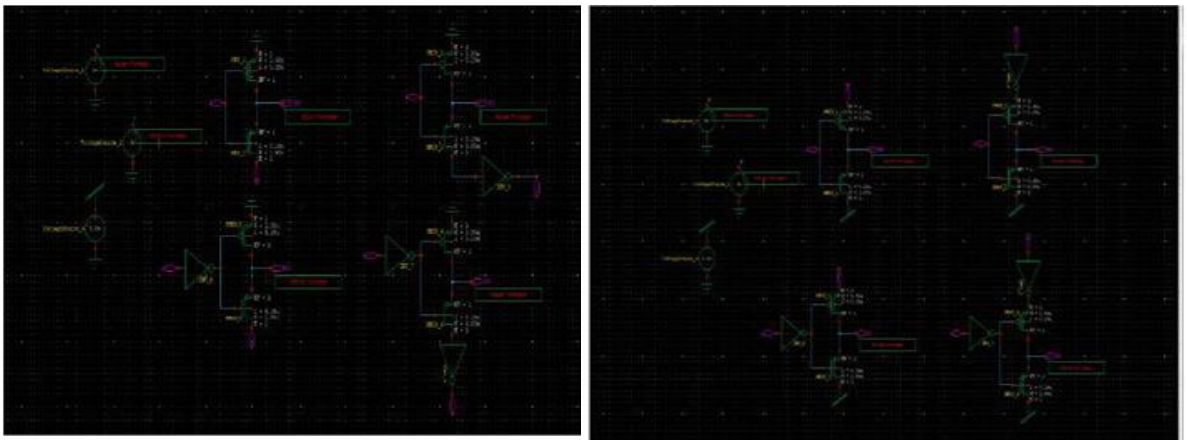


(a) **(b)**

Fig. 5: (a) OR gate (b) AND gate

4.2. 2-4 Inverting and NON-Inverting Decoder

GDI uses 4 AND gates and 2 Inverters and it requires a total of 12 transistors to design the 2-4 Decoder. Depending on the input combination one of output is selected and set as 1 and others are 0 thereby reducing the transistor count in GDI when compared to CMOS. The 2-4 inverting decoder uses 4 OR gates and 2 Inverters and it requires a total of 12 transistors. Reduced transistor count results in power dissipation.

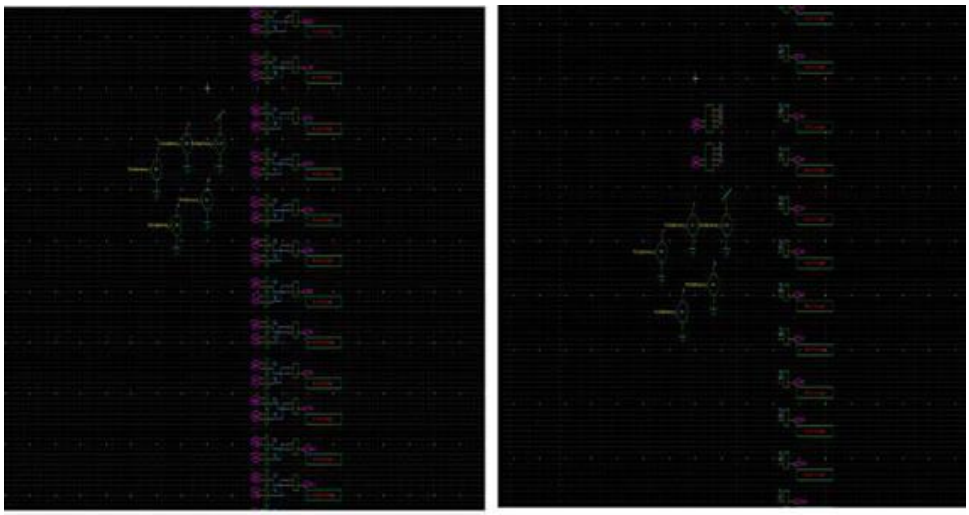


(a) **(b)**

Fig. 6: (a) Non-Inverting 2-4 NOR Decoder (b) Inverting 2-4 NAND Decoder

4.3. 4-16 Inverting and NON-Inverting Decoder

4-16 Non-Inverting 4-16 NOR Decoder is designed by using the 2 2-4 inverting decoders and 16 2-input NOR gates Inverting 4-16 NAND Decoder is designed by using 2 2-4 non-inverting decoders, 16 2-input NAND Gates.

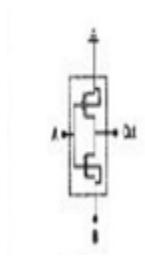
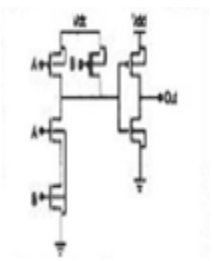
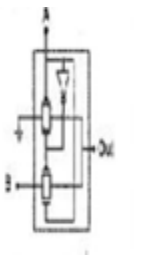
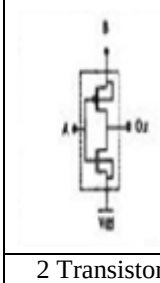
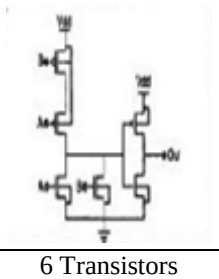
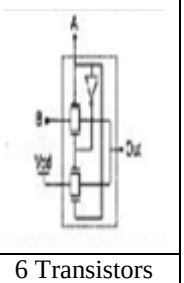


(a) **(b)**

Fig. 7: (a) Non-Inverting 4-16 NOR Decoder (b) Inverting 4-16 NAND Decoder

4.4 Comparisons of AND Gate, OR Gates transistors in different logics

Table 3: Comparison of gates

	GDI	CMOS	TG
AND			
	2 Transistors	6 Transistors	6 Transistors
OR			
	2 Transistors	6 Transistors	6 Transistors

5. SIMULATION RESULTS

The tanner EDA is used to calculate the power, delay, transistor count. All designs are compiled with 32nm technology and a typical library of tanner EDA is used to get the results.

Table 4: Comparison of Power of CMOS and GDI Technology

Decoders	Power (µW)					
	CMOS			GDI		
	0.8V	1V	1.2V	0.8V	1V	1.2V
2-4 NOR Decoder	1.801	6.36	51.89	0.342	6.21	17.93
2-4 NAND Decoder	3.82	6.83	54.91	1.82	6.0	36.6
4-16 NOR Decoder	5.88	20.5	140.3	4.02	15.84	85.5
4-16 NAND Decoder	5.551	108.9	135.04	23.5	92.1	21.3

Table 5: Comparison of Delay of CMOS and GDI Technology

Decoders	Delay (ns)					
	CMOS			GDI		
	0.8V	1V	1.2V	0.8V	1V	1.2V
2-4 NOR Decoder	1647.1	139.1	149.04.	1004.3	105.43	100.36
2-4 NAND Decoder	149.9	898.41	899.4	200.9	201.84	500.64
4-16 NOR Decoder	19041.7	25782.8	18439.9	2637.4	3767.6	8027.9
4-16 NAND Decoder	2201.9	25519.4	7905.8	1257.8	8432.7	1966.8

6. CONCLUSION

This paper introduced Associate in economical mixed-logic style for decoder circuits, combining TGL, DVL and static CMOS. By victimization this system, we have a tendency to developed four new 2-4 line decoder topologies, particularly 2-4LP, 2-4LPI, 2-4HP, and 2-4HPI, which supply reduced electronic transistor count and improved power-delay performance in reference to typical CMOS decoders. What is more, four new 4-16 line decoder topologies were conferred, particularly 4-16LP, 4-16LPI, 4-16HP and 4-16HPI, accomplished by victimization the mixed-logic 2-4 decoders as pre cryptography circuits and mixing them with post-decoders enforced in static CMOS logic? These styles mix the improved performance characteristics of passing electronic transistor logic with the restoring capability of static CMOS. We have a tendency to hope that the conferred results can encourage more analysis activities on GDI technique. The problem of serial logic style with GDI is presently being explored, further as technology compatibility for twin-well CMOS method. A lot of work recently exhausted automation of a logic style methodology supported GDI cells.

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