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A broader frequency range from Voltage Control Oscillator

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ABSTRACT

This describes a performance and well differ characteristics of a ring oscillator based VCO and the LC oscillator based VCO. The VCO is meant to operate in the PLL to generate local oscillations (LO) for an acquisition system. This work put forward the differential VCO design that has been wide operated tuning frequency range with reduced area, low power consumption, better phase-noise performance and good linearity between the frequency and control voltage. The circuit is to be designed and simulated on CMOS technology. The keyword on which it will be gone for the following parameter viz. Voltage controlled oscillator, ring oscillator, CMOS, frequency stability, power consumption. The digital CMOS process is being designed and their performances are compared based on the measurement results.

Keywords: *Control oscillator, Ring oscillator, CMOS, Frequency stability, Power consumption*

1. INTRODUCTION

1.1 Voltage Controlled Oscillator

Voltage control oscillator (VCOs) is the very necessary block for the designing of the RF transceiver for generated local oscillation frequency to up and down-convert the input signal. Oscillators generate periodic output sinusoidal signal. The block diagram of the oscillator is shown in figure 1.

Two conditions should be simultaneously satisfied for steady state oscillations:

- The loop gain | H (jωo) | = 1.
- The total phase shift around the loop must be 360° or zero.

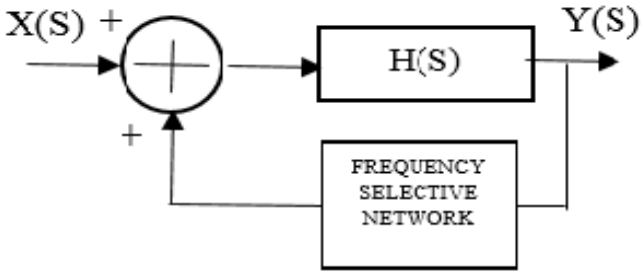

Fig. 1: Block diagram of oscillator

Frequency particular network is responsible to stabilize frequency. The VCOs can be constructed by two different senses, one is a differential VCO (DVCO) and the other is a balanced VCO (BVCO). The DVCO is convenient for cross-coupled differential configuration which has been mostly used because of its design simplicity and differential operation. Among CMOS BVCOs, the Colpitts BVCO is usually used. The conventional Colpitts BVCO uses only nMOS core, and its requirement a large supply current to start the oscillation.

The frequency of oscillation should be adjustable. The local oscillator frequency must be molded in well-defined steps; the output frequency of the oscillator frequencies varied with the help of the voltage then it is called as a voltage controlled oscillator to a particular sinusoidal modulation.

$$V_m = V_m \cos(\omega_m t)$$

1.2 Phase Locked Loop

A PLL is essential as feedback loop which locks the clock phase of the reference clock of an input clock signal. Phase locked loop is a closed loop system which compares the output with the input phase. It responses to both the frequency and the phase for the

input signals, automatically increasing or falling the frequency of a controlled oscillator until it's matched to the reference in both frequency and phase. A PLL is an example of a system using negative feedback which gets the phase changes which are in the bandwidth of the PLL. A PLL can multiply a low-frequency reference clock, to produce a high-frequency clock. The phase-locking is to be done after many iterations of comparing the reference. The goal of the PLL is to match the reference and feedback signals in phase. The state in which both the frequencies match is known as the lock state. After this, the PLL used to compare the two reference signals but since they are in lock mode, the PLL output is constant. The block diagram of PLL is shown below.

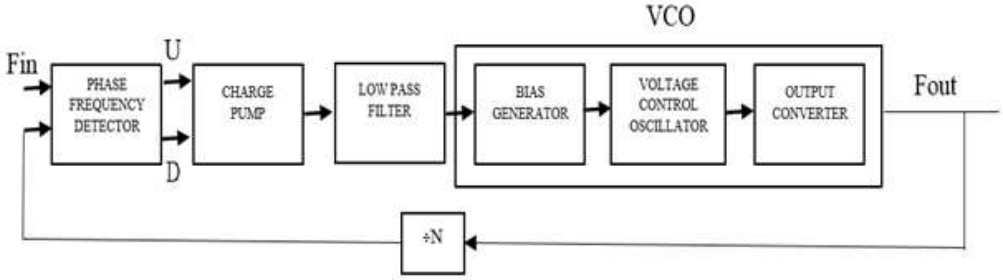

Fig. 2: Block diagram of PLL

A PLL consists of five main blocks:
1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

2. RELATED WORK

There is a wide area to work with a wide frequency range by VCO. Here is the some adoptive regarded technique has been figure out. [1] Design Techniques for a Low-Voltage VCO with Wide Tuning Range and Low Sensitivity To Environmental Variations. This represents implementation techniques to a low-voltage voltage-controlled oscillator (VCO) with a wider tuning range and poor sensitivity to process, voltage, and temperature (PVT) variations. For wide tuning range, a tuning scheme is penetrate coupled with voltage-boosting techniques with a manner that increases the quality factor and tuning range of a switched capacitor array. To reduce the design for a robust VCO, an adaptive body-biasing technique is proposed, which relaxes the starting constraint and improve the VCO's immunity to PVT variations. The proposed VCO is implemented in 0.18µm CMOS technology and operates at 2.4 GHz. It achieves phase noise of -117 dB c/Hz at 1MHz offsets and a tuning range of 20% while consuming 0.365mW of power. The figure-of-merit with the tuning frequency range is -197dBc/Hz, which is the lowest among the recent state of the art low-voltage VCOs [1].

Another technique represents an integrated voltage regulator to minimize supply pushing by LC voltage controlled oscillator (VCO). [2] A wide tuning 1.3 GHz LC VCO with fast settling noise filtering voltage regulator in 0.18 µm CMOS process. The integrated voltage regulator considered an on-chip low-frequency noise filter to minimize the phase noise on VCO. The **VCO** achieves current consumption of 15.9 mA with single integrated low-Q LC tank, tuning the range of 620.8 MHz to 1384.5 MHz, the phase noise of -128 dB c/Hz at 1 MHz offset from 1.3 GHz carrier at room temperature. With the noise filter, 9 dB improve in phase noise is demonstrated in measurement. The frequency range can be extended to 38.8 MHz - 1384.5 MHz with integrated frequency dividers [2].

In this paper describes a new approach to low-phase noise LC VCO design based on trans-conductance of linearization of active components. [3] A Linearized, Low-Phase-Noise VCO-Based 25-GHz PLL with Autonomic Biasing. A prototype 25 GHz VCO based on this linearization approach integrated for dual-path PLL and achieves superior performance compared to the state of the skill. The design is implemented in 32 nm SOI CMOS technology and achieves a phase noise of 130 dB c/Hz at a 10 MHz offset from a 22 GHz carrier. Additionally, the paper penetrates a new path to approach for switched capacitor arrays that enable a wide tuning range of 23%. More than 1500 measurements of the PLL across PVT were varying, further validating the proposed design. Phase noise variation across 55 dies for four different frequencies is $\sigma < 0.6$dB. Also, phase noise variation across supply voltages of 0.7–1.5 V is 2 dB and across 60°c temperature variation is 3 dB. At the 25 GHz center frequency, the VCO FOM_T is 188 dB c /Hz. Additionally, a digitally assisted autonomic biasing technique is implemented in the PLL to provide a phase noise and power optimized VCO bias across frequency and process. Measure men results indicate the efficacy of the autonomic biasing scheme [3].

This presents the two-stage CMOS differential voltage-controlled ring oscillator (VCO). [4] A High Swing Low Power CMOS Differential Voltage-Controlled Ring Oscillator. The VCO is intended to operate as a frequency synthesizer in a PLL to generate local oscillator frequency (LO) for an acquisition system, providing in-phase/Q-phase outputs. This work proposes a differential VCO design that has a wide operating frequency tuning range with low power consumption, better phase-noise performance and good linearity between the frequency and control voltage. The circuit is implemented in 0.18 µm CMOS Process operates at frequency: 186 MHz to 1.58 GHz. The DC Supply of 1.8 V is applied and dissipates 11.38mW of power. The Phase noise is -113.5dBc / Hz [4].

Low Phase Noise Wide Frequency Range Ring VCO Based Scalable PLL with Sub-harmonic Injection Locking in 0.18µm CMOS. [5] A low phase noise ring VCO based PLL (frequency tuning range: 0.65-1.6 GHz) with sub-harmonic injection locking

was realized (PLL area: 0.1 mm2) by adopting 0.18µm CMOS technology and combining pMOS resistive loads with a circuit for shifting bias levels; this makes the rail-to-rail range of voltages usable as control voltages. For a 90-MHz input reference signal, without injection locking, the 0.2MHz-offset phase noise was -108dBc/Hz (PLL output frequency: 1.44GHz = 16 X 90MHz); with injection locking, the noise was -122 dB c/Hz (spurious level: -35 dB c; power consumption from a 1.8V power supply: 39mW). [5]

3. CONCLUSION

Design of VCO using CMOS differential voltage controlled ring oscillator for finding the area efficient CMOS ring VCO to reduce the overall area of PLL. The following steps are involved for verification and testing by mathematical calculation.

- O/P Frequency up to 1GHz.
- To avoid the large area by varying the W/L ratio minimizing the severity of the problem.
- Implementation has been done with the available tools.
- Verification and Testing will be done by matching the mathematical calculation and the result of the simulation.

The implementation can be done by the available tools like Tanner, Micorwind, etc…

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