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Comparison and analysis of various low power SRAM cells

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ABSTRACT

With the advancement of CMOS technology, an outsized variety of transistors used thanks to that scaling happens. Currently on a daily basis memory plays a crucial role within the entire chip and provides the most power to the SOC system. during this paper, 6-T HVP, 7-T HVP, 8-T HVP and 9-T HVP is projected that improve the soundness of SRAM cell, reduce power in read-write operation and reduce escape power in standby mode. 2 techniques accustomed reduce power and escape power. In 1st technique offer voltage of one.1V is taken to look at the power within the overall circuit. In second technique offer voltage of one.1V is taken and voltage given to inputs is about to zero and thence power and escape the power of projected circuits are reduced. The Designed SRAM cells are compared to Existing SRAM cells in term of power, escape power, SNM, RSNM, PULL UP ratio (PR), CELL quantitative relation (CR), Temperature and Voltage. The simulation meted out in Tanner EDA tool with 32nm technology at 1V and CADENCE VIRTUOSO tool with 45nm technology at 1.1V power offer severally.

Keywords: *Power, Leakage lower, SRAM, RSNM, PR, CR, Temperature*

1. INTRODUCTION

It is present that Static Random Access Memory (SRAM) with technology scaling occupies a lot of space and power consumption of the System on Chip (SOC) devices. Semiconductor memory is employed for storing the digital data within the massive extent of all digital system. Thus, these are peculiar elements in varied applications corresponding to hand-held devices and superior processors. There's continuously a high demand for larger knowledge storage capability associate degreed it ends up in an increased fabrication technology and development of memory with relevance compact style rules. due to of these aspects, an influence of the SRAM cell may be a major issue and because of this low power, SRAM cell styles square measure desired with the optimum worth of speed performance in VLSI styles [1]. Since several decades, efforts are created to scale down the CMOS devices to get higher performance with relevance speed, delay, power consumption, noise margin, and figure of benefit etc. it's ascertained with several studies that run power consumption will increase with the low worth of threshold voltage.

This study is intended for developing an extremely stable low power memory cell. During this study, a unique SRAM cell is meant for reducing the run power and simulation results has shown in forty-five nm and 32 nm CMOS technology. The remainder paper is presenting the entire theme of study in varied sections. Section II offers a quick rationalization of Existing Circuits of SRAM cells structures. Section III individual simulation results of the designed circuit are shown. Section IV shows comparison and analysis of designed circuits. Finally, section IV describes conclusions for designed circuits and existing circuit.

2. THE DESIGNED CIRCUIT OF SRAM CELL

2.1. 6-T HVP SRAM cell

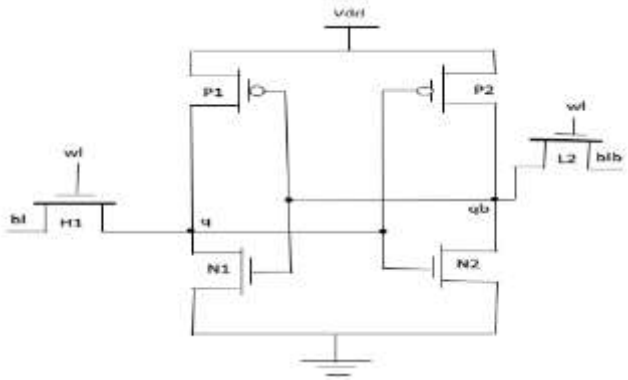

Fig. 1: Schematic of designed circuit 6-T HVP SRAM cell

A Designed Circuit of 6-T HVP SRAM cell is created of 2 access NMOS transistor (H1 and L2) that is created by High-Vt transistors to scale back the leakage power and power and 2 cross-coupled inverters (Latch). H1 and L2 act as pass transistor that's portrayed in Fig one whereas 2 cross-coupled inverters type a latch that acts as a storing component. As access transistor is enabled by victimization word line (wl) and every bit is keeping within the latch. As long as wl is low, H1 and L2 area unit disabled. Therefore, scan or write operations aren't performed throughout this state and hold state is needed. during this state, latch holds a small amount as long as voltage remains at Vdd and Gnd. H1 and L2 area unit enabled once wl becomes high and browse and write operations area unit performed throughout this state [3][4]. SRAM cell may be written with a replacement worth of a small amount in situ of an antecedently keep bit. H1 and L2 area unit enabled by victimization wl=1 to

perform a write operation. Bit Line (bl) takes needed knowledge to be written and Bit Line Bar (blb) takes the complemented worth of needed knowledge to be written. As an instance, if we tend to want to write down "1" to SRAM cell then bl and blb area unit set to "1" and "0" severally. As wl is modified to "0" the specified knowledge is written to the cell. SRAM cell is ready to speak its keep knowledge whereas it's in reading mode. wl is unbroken at high to read knowledge from SRAM cell and activates the H1 and L2. Currently relying upon the state of latch one bl is pre-charged to "1" to perform read operation and different bl would be discharged to ground. Therefore as long as bl remains charge, blb should be discharged or contrariwise.

2.2. 7-T HVP SRAM cell

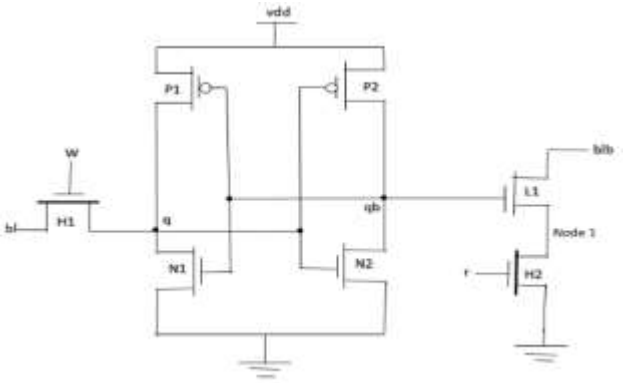

Fig. 2: Schematic of designed circuit 7-T HVP SRAM cell

Figure 2 depicts the Designed Circuit of 7-T HVP SRAM cell. So as to reduce the ability consumption and circuit area, a new information is written to designed SRAM cell by employing a single bit line and one pass semiconductor. By exploitation, these style of cross-coupled inverters facilitates within the successful transfer of each bits "0" and "1" to the designed memory cell. bl is pre-charged to Vdd before reading operation. For the read operation, read signal r goes up to Vdd whereas write signal w is unbroken at gnd [2] [7] [8]. If we have a tendency to want to store "1" at Node one, bl is discharged by L1 and H2 (high- Green Mountain State semiconductor to scale back escape power). Similarly, if we have a tendency to want to store "0" at Node one, bl is unbroken at Vdd associated not absolutely discharged through an L1-H2 stack.

For the write operation, bl is charged (discharged) to Vdd (zero) to induce "1" ("0") onto Node 1. Write signal w goes up to Vdd whereas read signal is unbroken at zero for the write operation. The pass transistor is high- vt transistor to reduce leakage power and should be stronger than the pull-up transistor P1 for writing "0" onto Node one. Equally, pass transistor H1 should be stronger than pass transistor N1 for writing "1". As H1 transfers degraded "1" (because of vt drop across N-channel access transistor), the electrical converter created by N2 and P2 got to have an occasional price of switching threshold voltage for helping a full "1" transfer onto Node one.

2.3. 8-T HVP SRAM cell

The 8-T HVP SRAM cell style uses 2 additional transistors to isolate read and write ways [10] [5]. Separate improvement of write and read operations is completed as shown in Fig three. The pass transistors H1 and L2 are high vt transistors those are used for reducing discharge power and reading, therefore, wl is unbroken low whereas reading. 2 stacked nmos L1 & H2 alongside isolated read bit line (rbl) constitutes the scanning circuitry for playing read operation. As information is read through single-ended read bit line, scan word line (rwl) goes high. Hence, they improve performance altogether the states of operation like scan operation, write operation and idle state.

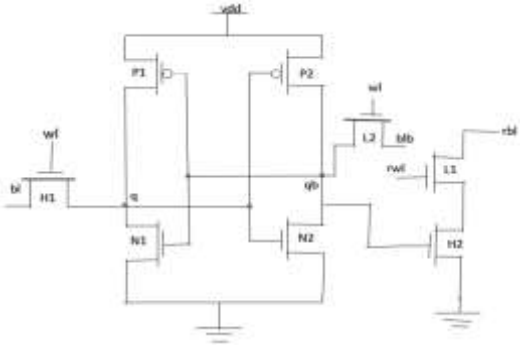

Fig. 3: Schematic of designed circuit 8-T HVP SRAM cell

2.4. 9-T HVP SRAM CELL

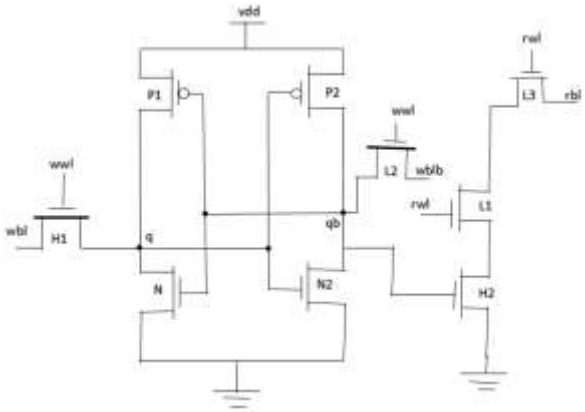

Fig. 4: Schematic of designed circuit 9-T HVP SRAM cell

The Designed Circuit of 9-T HVP SRAM cell is represented in Fig 4. It uses 2 totally different methods for write and read operations. During this schematic, write operation is performed by wbl and wblb whereas read section activation is performed by a single rbl. During this means, power consumption is increased .so pass transistor H1 and L2 is created by high-Vt transistors to cut back leakage power Stack transistors (L1 and L3) suppresses the escape current for enhancing read operation. The look of this structure is predicated on standard 9T SRAM cell [9]. AN electrical converter is employed as a buffer for analytic the storage nodes from reading operation path remaining unchanged. L1 is employed to reduce escape current yet on eliminating the requirement of a charge pump for a variable ground voltage that reduces escape the current.

3. SIMULATION RESULTS

The Analysis & Comparison of the Designed circuit of SRAM cells is carried out in term of SNM, RSNM, Cell Ratio (CR), Pull up Ratio (PR), Temperature and voltage.

3.1 Temperature with respect to SNM of designed circuits

For calculation of SNM, the temperature is varied from 23ºC to 73 ºC. Shows that designed SRAM cells show a decrease in SNM over temperature.

3.1.1 6-T HVP SRAM CELL

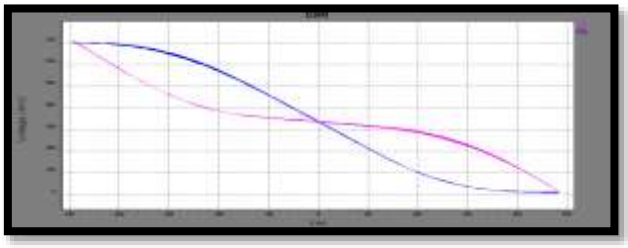

Fig. 5: Output waveform during temperature vs. SNM

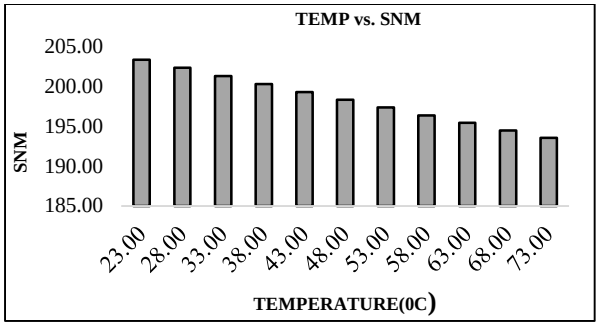

Fig. 6: Temperature vs. SNM (mv)

3.1.2 7-T HVP SRAM cell

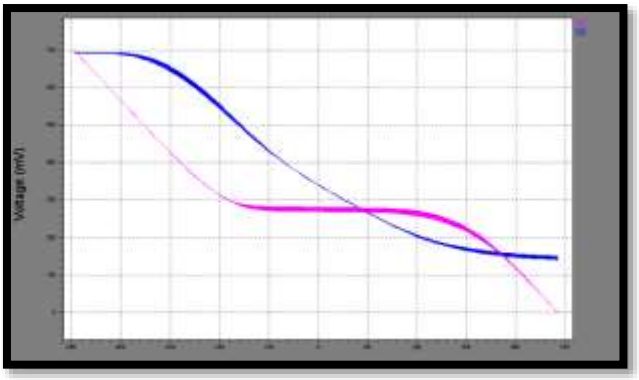

Fig. 7: Output waveform during temperature vs. SNM

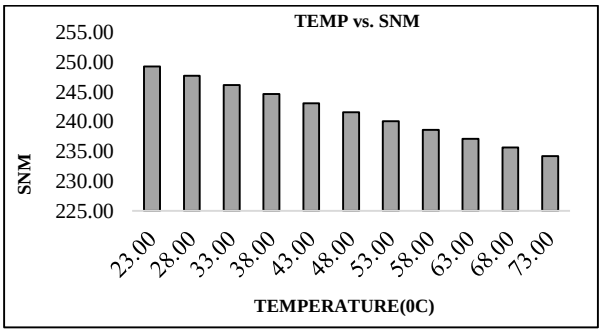

Fig. 8: Temperature vs. SNM (mv)

3.1.3 8-T HVP SRAM Cell

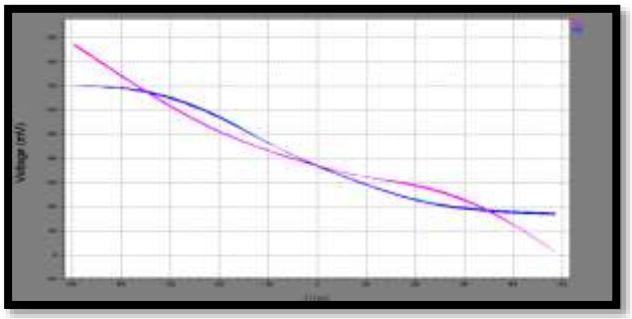

Fig. 9: Output waveform during temperature vs. SNM

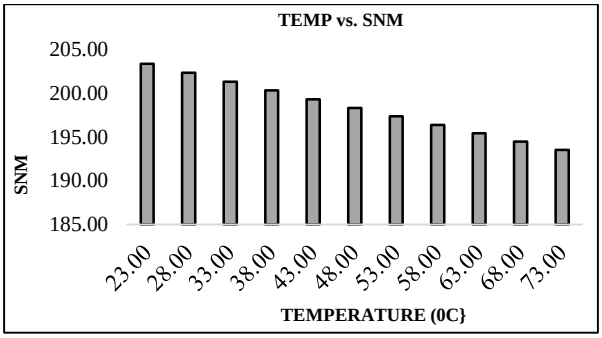

Fig. 10: Temperature vs. SNM (mv)

3.1.4 9-T HVP SRAM cell

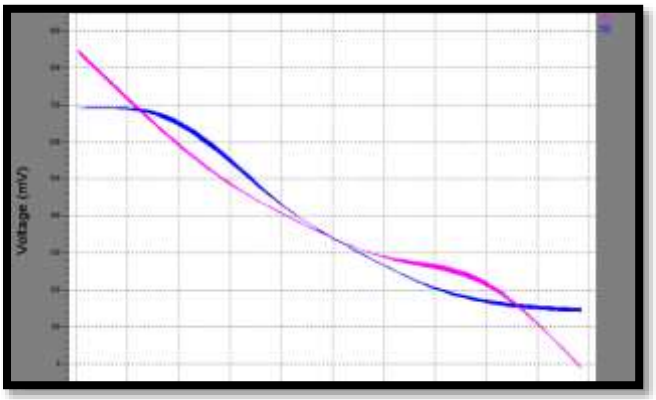

Fig. 11: Output waveform during temperature vs. SNM

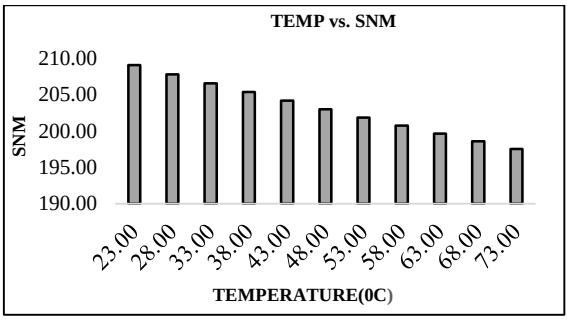

Fig. 12: Temperature vs. SNM (mv)

3.2 Pullup Ratio (PR) vs. RSNM of designed circuits

Pull up the ratio of transistors. Pull up ratio is that the ratio of sizes of load transistor to the access transistor. Read static noise margin (RSNM) could be a measure of what proportion noise voltage needed at the node storing "0" to flip the state of AN SRAM cell whereas reading. Fig shows that SRAM cells have high RSNM as a voltage increase.

3.2.1 6-T HVP SRAM cell

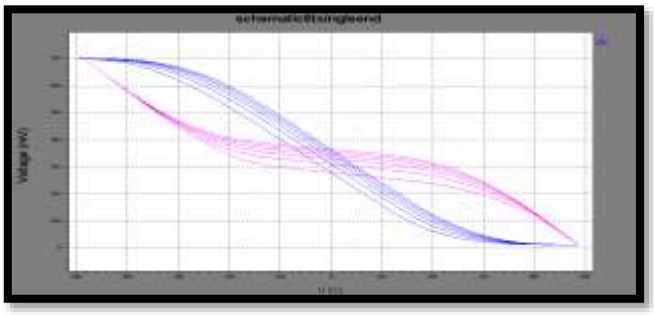

Fig. 13: Output waveform during Pullup Raatio (PR) vs. RSNM

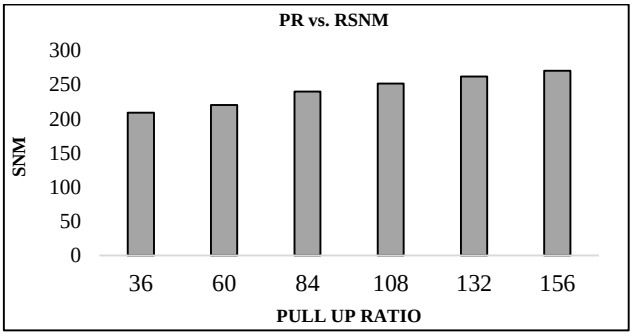

Fig. 14: Pullup Ratio (PR) vs. RSNM (mv) of designed circuit

3.2.2 7-T HVP SRAM cell

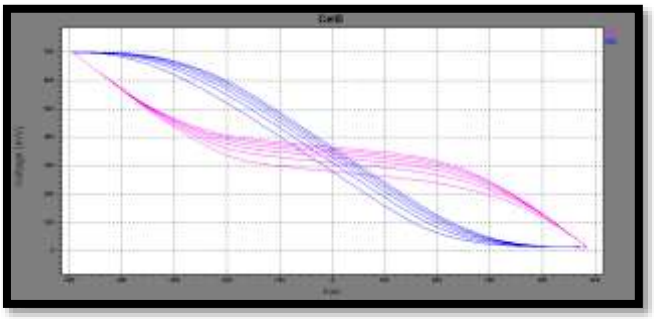

Fig. 15: Output waveform during Pull up Ratio (PR) vs. RSNM

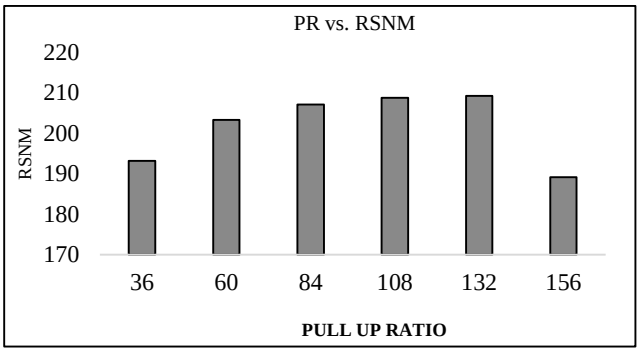

Fig. 16: Pull up Ratio (PR) vs. RSNM (mv)

3.2.3 8-T HVP SRAM cell

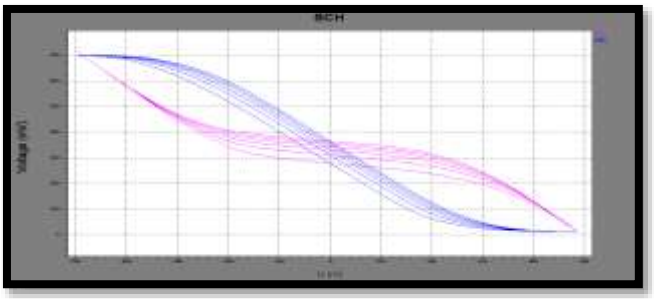

Fig. 17: Output waveform during Pull up Ratio (PR) vs. RSNM

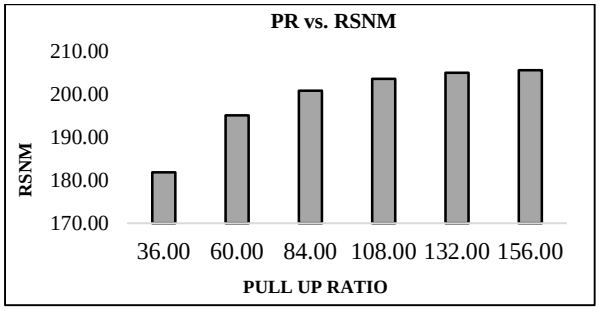

Fig. 18: Pull up Ratio (PR) vs. RSNM (mv)

3.2.4 9-T HVP SRAM cell

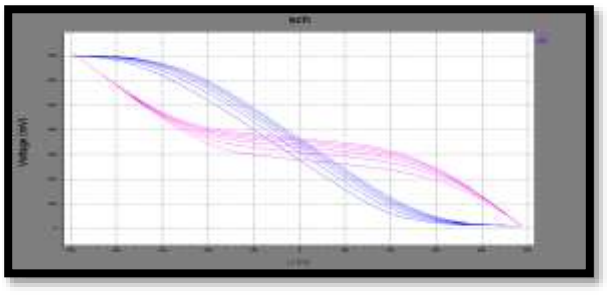

Fig. 19: Output waveform during Pull up Ratio (PR) vs. RSNM

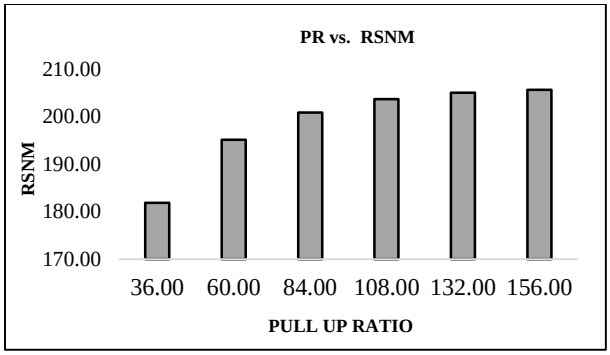

Fig. 20: Pull up Ratio (PR) vs. RSNM (mv)

3.3 Cell Ratio (CR) vs. RSNM of designed circuits

The SNM of SRAM cell depends on the scale of the device. The device size describes in terms of cell ratio. Cell ratio is that the ratio between sizes of the driver transistor to the access transistor throughout a read operation. Read static noise margin (RSNM) could be a life of what quantity noise voltage needed at the node storing "0" to flip the state of an SRAM cell whereas reading. Fig shows that RSNM of SRAM cell decreases because of the voltage increase.

3.3.1 6-T HVP SRAM cell

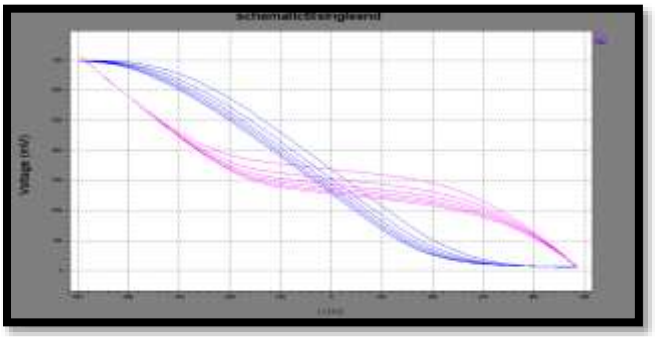

Fig. 21: Output waveform during Cell Ratio (CR) vs. RSNM

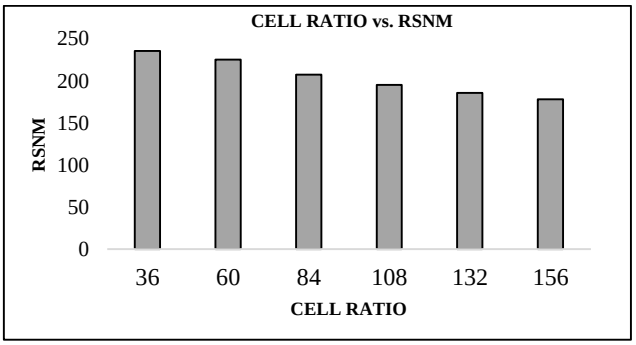

Fig. 22: Cell Ratio (CR) vs. RSNM (mv)

3.3.2 7-T HVP SRAM cell

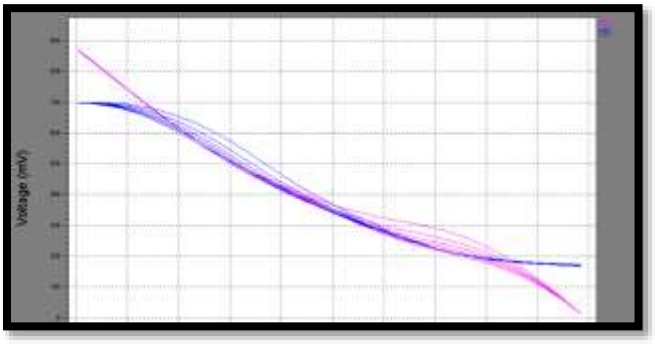

Fig. 23: Output waveform during Cell Ratio (CR) vs. RSNM

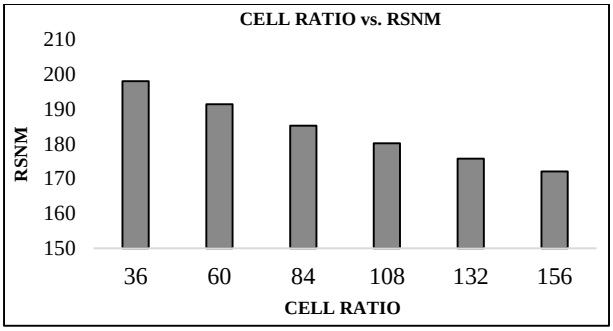

Fig. 24: Cell Ratio (CR) vs. RSNM (mv)

3.3.3 8-T HVP SRAM cell

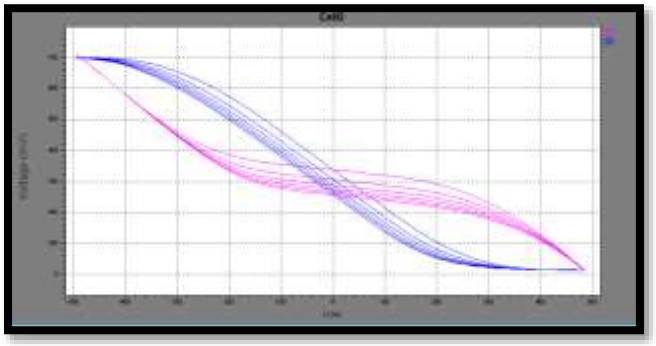

Fig. 25: Output waveform during Cell Ratio (CR) vs. RSNM

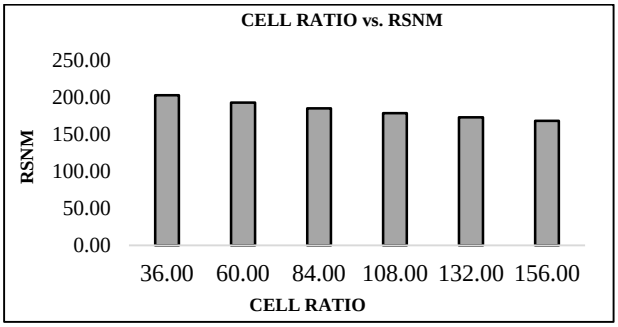

Fig. 26: Cell Ratio (CR) vs. RSNM (mv)

3.3.4 9-T HVP SRAM cell

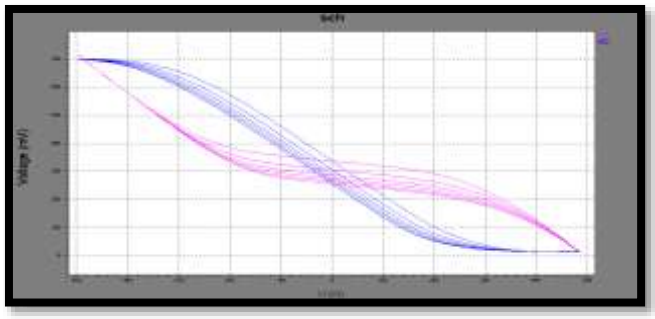

Fig. 27: Output waveform during Cell Ratio (CR) vs. RSNM

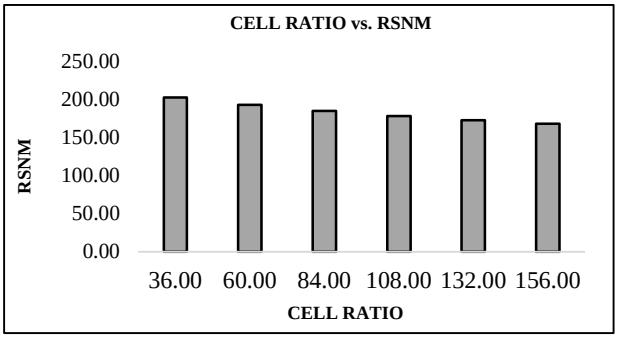

Fig. 28: Cell Ratio (CR) VS RSNM (mv)

3.4 Voltage (VDD) vs. RSNM of designed circuits

Read static noise margin (RSNM) could be a measure of what quantity noise voltage needed at the node storing "0" to flip the state of an SRAM cell whereas reading. Fig shows that RSNM of SRAM cell increase as a voltage increase.

3.4.1 6-T HVP SRAM cell

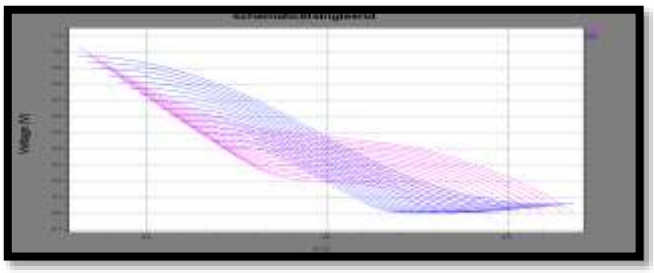

Fig. 29: Output waveform during voltage (VDD) vs. RSNM

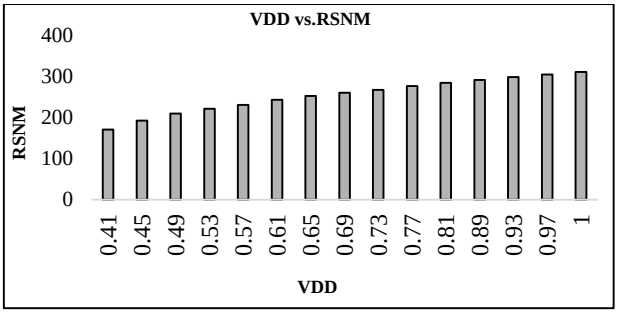

Fig. 30: Voltage (VDD) vs. RSNM (mv)

3.4.2 7-T HVP SRAM cell

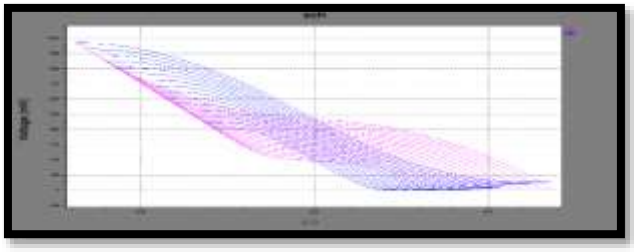

Fig. 31: Output waveform during Voltage (VDD) vs. RSNM

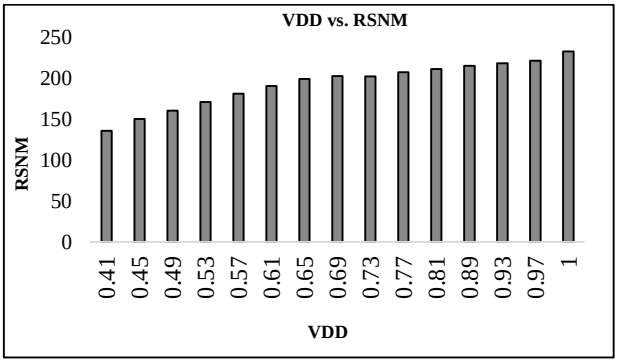

Fig. 32: Voltage (VDD) vs. RSNM (mv)

3.4.3 8-T HVP SRAM cell

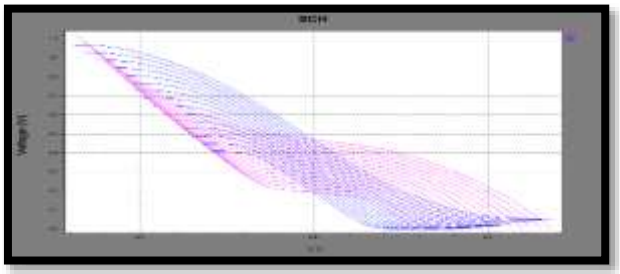

Fig. 33: Output waveform during Voltage (VDD) vs. RSNM

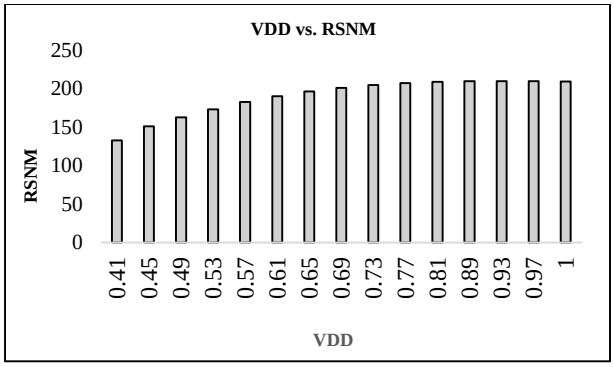

Fig. 34: Voltage (VDD) vs. RSNM (mv)

3.4.4 9-T HVP SRAM cell

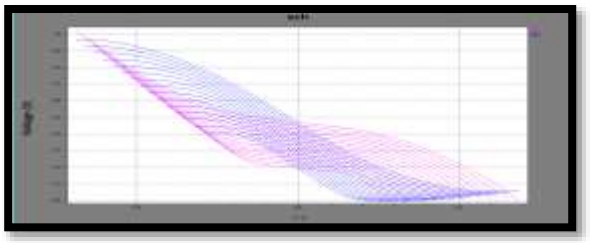

Fig. 35: Output waveform during Voltage (VDD) vs. RSNM

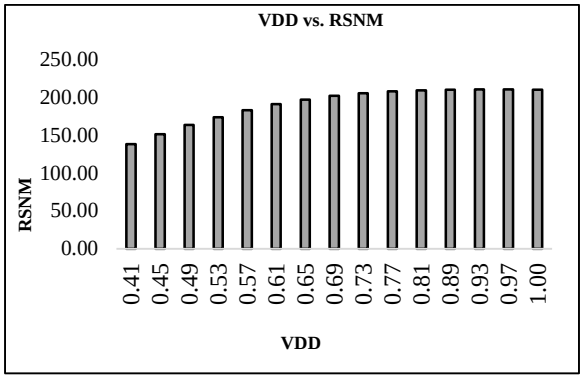

Fig. 36: Voltage (VDD) vs. RSNM (mv)

3.5 Voltage (VDD) vs. SNM of designed circuits

The SNM is outlined because the "maximum quantity of noise voltage which will be introduced at the output of the 2 inverters, specified the cell retains its data". SNM calculate the number of noise voltage needed at the inner nodes of the SRAM cell to flip the cell's knowledge. Fig shows that SNM of SRAM cell increase as a voltage increase.

3.5.1 6-T HVP SRAM cell

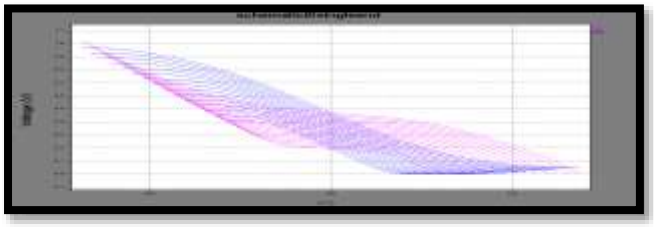

Fig. 37: Output waveform during Voltage (VDD) vs. SNM

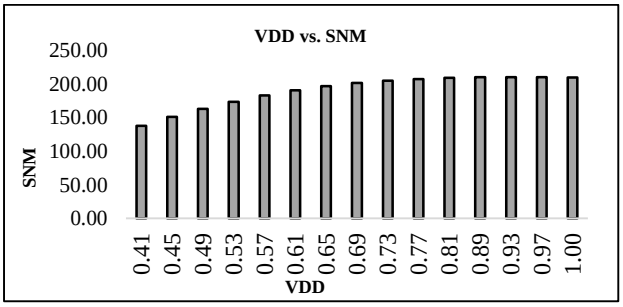

Fig. 38: Voltage (VDD) vs. SNM (mv)

3.5.2 7-T HVP SRAM cell

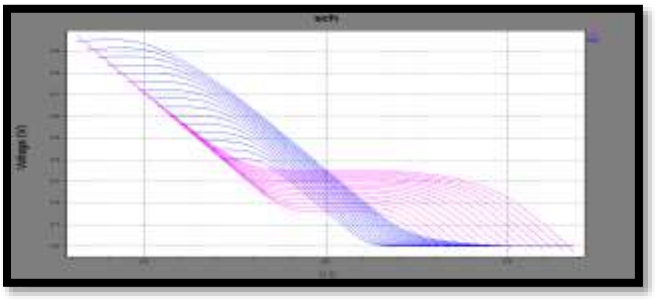

Fig. 39: Output waveform during Voltage (VDD) vs. SNM

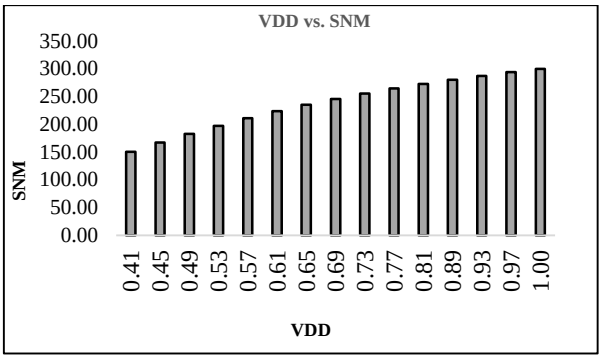

Fig. 40: Voltage (VDD) vs. SNM (mv)

3.5.3 8-T HVP SRAM cell

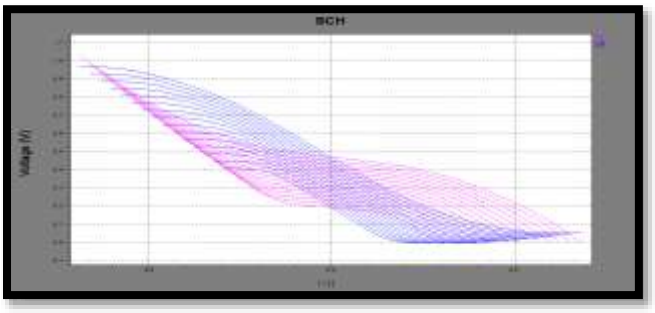

Fig. 41: Output waveform during Voltage (VDD) vs. SNM

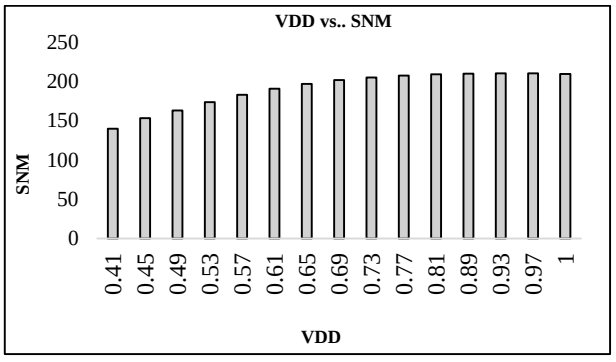

Fig. 42: Voltage (VDD) vs. SNM (mv)

3.5.4 9-T HVP SRAM cell

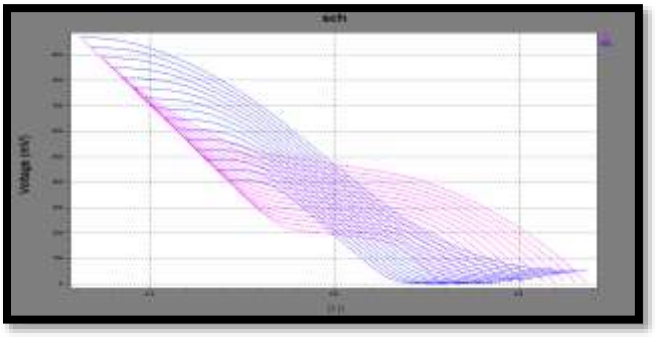

Fig. 43: Output waveform during Voltage (VDD) vs. SNM

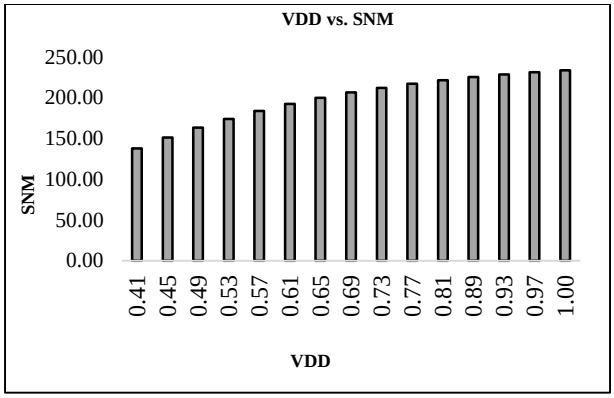

Fig. 44: Voltage (VDD) vs. SNM (mv)

4. SIMULATION RESULTS

The Analysis & Comparison of Existing SRAM cell and Designed circuit of SRAM cells is carried out in term of power, leakage power, SNM, RSNM, Cell Ratio (CR), Pull up Ratio (PR), Temperature and voltage.

4.1 Power Dissipation in Existing and Designed circuits

Table 1 shows the quantity of power dissipation within the time period of 20ns. it's been showed that power dissipation of projected circuit is a smaller amount as compared to Existing circuits in an exceedingly read-write mode in 7-T HVP and 9-T HVP, stay same in 8-T existing SRAM cell & 8-T HVP SRAM Cell and increase in 6-T HVP SRAM Cell as compared to 6-T existing SRAM Cell.

Table 1: Power dissipation (uw) in SRAM cells

SRAM cells (Existing)	Power Dissipation (UW)	SRAM cells (Designed)	Power Dissipation (UW)
6-T SRAM cell	0.000036	6-T HVP SRAM cell	0.000039
7-T SRAM cell	0.000025	7-T HVP SRAM cell	0.000018
8-T SRAM cell	0.000036	8-T HVP SRAM cell	0.000036
9-T SRAM cell	0.000081	9-T HVP SRAM cell	0.000068

4.2 Leakage Power in Existing and Designed circuit

Table 2 show the amount of Leakage power in the time period of 20ns. It has been showed that Leakage power of the proposed circuit is less as compared to Existing circuits in Standby mode.

Table 2: Leakage Power (PW) IN SRAM cell

SRAM cell (Existing)	Power Dissipation (UW)	SRAM cell (Designed)	Power Dissipation (UW)
6-T SRAM cell	17.65185	6-T HVP SRAM cell	11.12000
7-T SRAM cell	13.84389	7-T HVP SRAM cell	10.57599
8-T SRAM cell	17.65185	8-T HVP SRAM CELL	11.11607
9-T SRAM CELL	17.65100	9-T HVP SRAM CELL	11.11600

4.3 Temperature with respect to SNM of designed circuits

For calculation of SNM, the temperature is varied from 23ºC to 73 ºC. Fig (45) shows that 7-T HVP SRAM show high SNM over temperature.

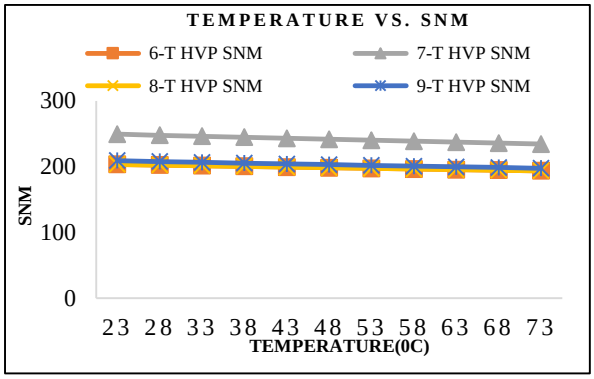

Fig. 45: Temperature vs. SNM (mv) of designed circuits

4.4 Pullup Ratio (PR) vs. RSNM

Pull up the ratio of transistors. Pull up ratio is that the ratio of sizes of load transistor the access transistor. Browse static noise margin (RSNM) may be a measure of what quantity noise voltage needed at the node storing "0" to flip the state of an SRAM cell whereas reading. Fig (46) show that 6-T HVP SRAM cell has high RSNM as compared to others.

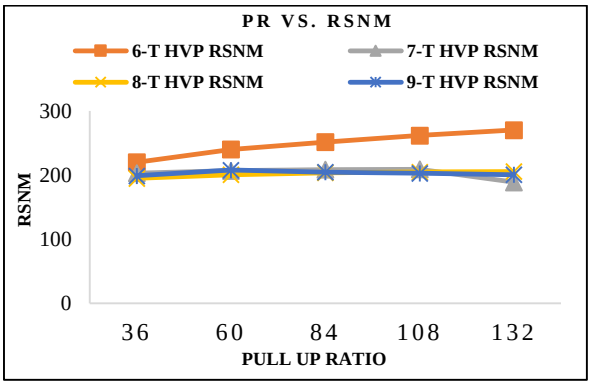

Fig. 46: Pullup Ratio (PR) VS RSNM (mv) of designed circuits

4.5 Cell Ratio vs. RSNM

The SNM of SRAM cell depends on the size of the device. The device size describes in terms of cell ratio. Cell ratio is that the ratio between sizes of the driver junction transistor to the access transistor throughout a Read operation. Read static noise margin (RSNM) could be a measure of what quantity noise voltage needed at the node storing "0" to flip the state of an SRAM cell whereas reading. Fig (47) show that 6-T HVP SRAM cell has high RSNM as compared to others.

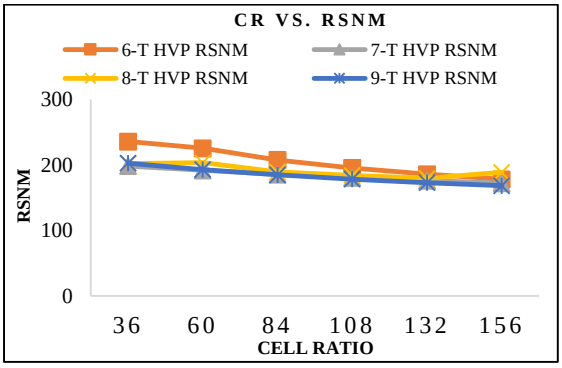

Fig. 47: Cell Ratio (CR) vs. RSNM (mv) of designed circuits

4.6 Voltage (VDD) vs. RSNM

Read static noise margin (RSNM) is a measure of how much noise voltage required at the node storing "0" to flip the state of an SRAM cell while reading. Fig (48) show that 6-T HVP SRAM cell has high RSNM as compared to others.

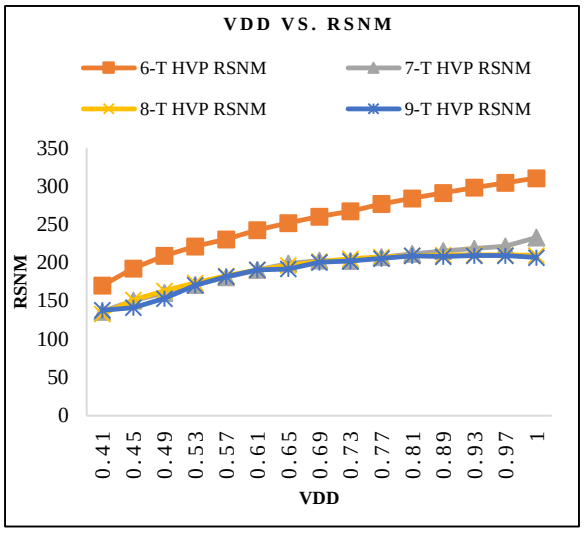

Fig. 48: VDD vs. RSNM (mv) of designed circuits

4.7 Voltage (VDD) vs. SNM

The SNM is defined as the "maximum amount of noise voltage that can be introduced at the output of the two inverters, such that the cell retains its data". SNM calculate the amount of noise voltage required at the internal nodes of the SRAM cell to flip the cells data. Fig (49) show that 7-T HVP SRAM cell have high SNM as compared to others.

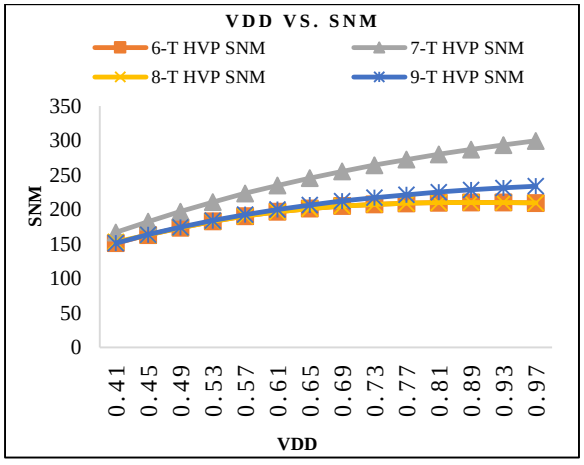

Fig. 49: Voltage (VDD) vs. SNM (mv) of designed circuits

6-T HVP SRAM cell, 7-T HVP SRAM cell leakage power is also reduced by 23%, in 8-T HVP SRAM cell leakage power is also reduced by 37.02% and in 9-T HVP SRAM cell leakage power is also reduced by 37%.

5. CONCLUSION

If we compared Designed circuit with Existing circuit SRAM SNM is improved in 6-T HVP SRAM cell is 40%, SNM is improved in 8-T HVP SRAM cell is 14% and SNM is improved in 9-T HVP SRAM cell is 17.95% improved in TANNER EDA tool at a 1V voltage in 32nm Technology. Leakage power is also reduced by 37%.

6. REFERENCES

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