INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume 4, Issue 3)
Available online at: www.ijariit.com

Low power and area efficient shift registers using pulsed latches

Ippe Nikhila
i.nikhila428@gmail.com
Geethanjali Institute of Science and Technology, Nellore, Andhra Pradesh

K. Divya
divyapandu53@gmail.com
Geethanjali Institute of Science and Technology, Nellore, Andhra Pradesh

P. Raghava Reddy
raghavareddypemmu@gmail.com
Geethanjali Institute of Science and Technology, Nellore, Andhra Pradesh

ABSTRACT

The power consumption and area reduction are the key challenges in the Very Large Scale Integration (VLSI) circuit design. The shift register is the main building block in the VLSI circuits. The shift register is composed of clock interconnection network and timing elements such as flip-flops and latches this clock entomb association system and timing component is the primary power and region expending component in the move enlist. This clock interconnection network and timing element is the main power and area consuming element in the shift register. This project introduces a low power and area efficient shift register using pulsed latch and pulse generation circuit. The area and power consumption will be reduced to 50%in the shift register if the Flip-Flop is replaced with the pulsed latch. This technique explains the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals as an alternative of the conventional single pulsed clock signal.

Keywords: *Shift registers, Flip-flop, Pulsed latches, Low power, Efficient area*

1. INTRODUCTION

Flip-flops are the fundamental stockpiling components utilized widely in a wide range of advanced outlines. As the element size of CMOS innovation process downsized by Moore's Law, fashioners can coordinate numerous quantities of transistors onto a similar bite the dust. The more transistors there will be all the more exchanging and more power disseminated as warmth or radiation. Warmth is one of the wonder bundling challenges in this age, it is one of the primary difficulties of low power plan approaches and hones. Another driver of low power look into is the unwavering quality of the coordinated circuit. Additional exchanging infers higher normal current is removed and thusly the likelihood of unwavering quality issues happening rises. We are moving from PCs to tablets and much littler figuring computerized frameworks. With this profound trend continuing and without a match trending in battery life expectancy, the more low power issues will have to be addressed. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today's and future integrated chips. The power consumption of very large Scale Integrated design is given by Generalized relation, $P = CV^2f$. Since power is proportional to the square of the voltage as per the Relation, voltage scaling is the most prominent way to reduce power dissipation. In any case, voltage scaling is brought about edge voltage scaling which bows to the exponential increment in spillage control.

In spite of the fact that few commitments have been made to the craft of single edge activated flip-flounders, a need clearly happens for a plan that further enhances the execution of single edge activated flip failures designs. The engineering of a move enlist is very basic. An N-bit move enroll is made out of arrangement associated N information flip-flops. The speed of the flip flounder is less vital than the region and power utilization in light of the fact that there is no circuit between flip-flops in the move enlist. The littlest flip-tumble is appropriate for the move to enlist to diminish the territory and power utilization. As of late, beat hooks have supplanted flip-tumbles in numerous applications, in light of the fact that a beat lock is significantly littler than a flip-flop.

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2. METHODOLOGY

An ace slave flip-slump utilizing two hooks can be supplanted by a beat lock comprising of a lock and a beat check motion in Fig.2.1. All beat locks share the beat age circuit for the beat clock flag. Therefore, the zone and power utilization of the beat hook turns out to be half of those of the ace slave flip-tumble. The beat hook is an appealing answer for the little region and low power utilization. The beat hook can't be utilized as a part of move enrolls because of the planning issue. The move enrolls in Fig 3.1 comprises a few locks and a beat clock flag (CLK_pulse).

The activity waveform in Fig 2.2 demonstrates the planning issue in the shifter enlist. The yield flag of the main lock (Q1) changes accurately in light of the fact that the info flag of the principal hook (IN) is steady amid the clock beat width. Yet, the second lock has a dubious yield flag (Q2) on the grounds that its info flag (Q1) changes amid the clock beat width.

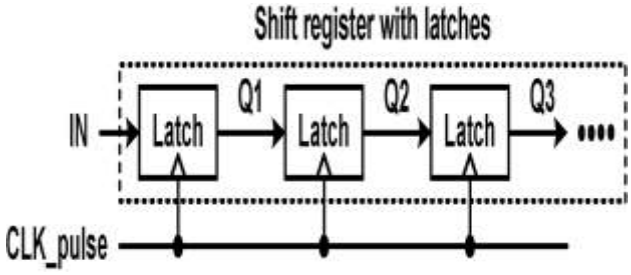

Fig. 2.1: Shift register with Latches

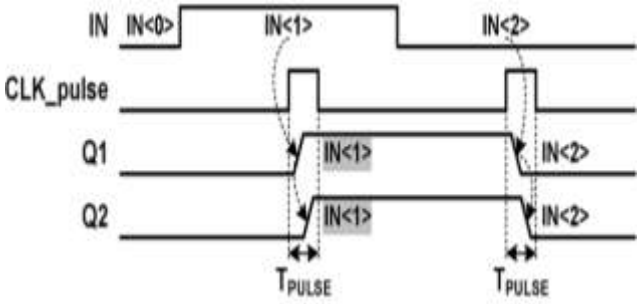

Fig. 2.2: waveforms

One solution for the timing problem is to add delay circuits between latches, as shown in Fig 2.3. The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig 2.4 the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and there is no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads.

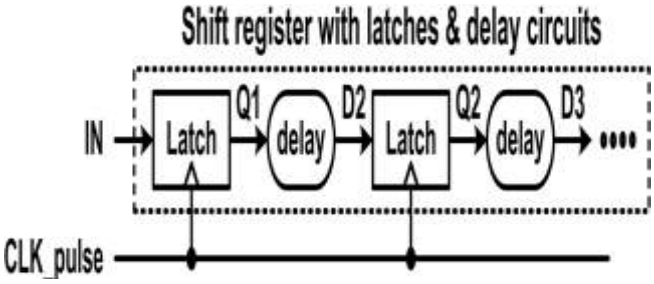

Fig. 2.3: Shift register with latches and delay circuits

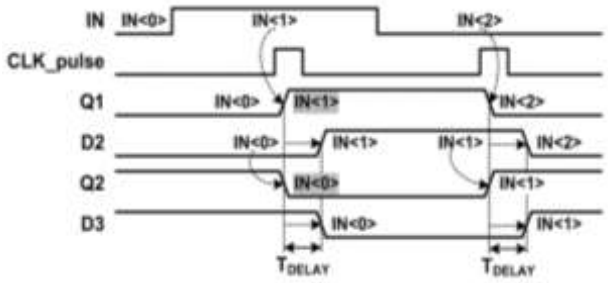

Fig. 2.4: Waveforms

Another solution is to use multiple non-overlaps delayed pulsed clock signals, as shown in Fig 2.5. The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each hook utilizes a beat clock flag, which is postponed from the beat check flag utilized as a part of its next lock.

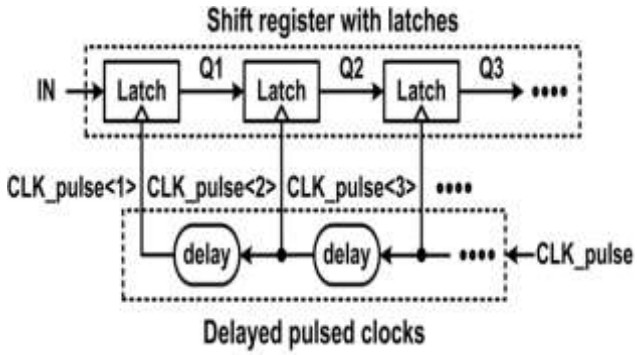

Fig 2.5: Shift registers with Delayed pulsed clocks

Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and there is no timing problem occurs between latches. However, this solution also requires many delay circuits. The proposed shift register is divided into two sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register contains five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK pulse⟨1:4⟩ and CLK pulse⟨T⟩). In the 4-bit sub shift register #1, 4 latches store 4-bit data (Q1-Q4) and the newest latch stores 1-bit temporary data (T1) which will be deported in the first latch (Q5) of the 4-bit sub shift register #2.

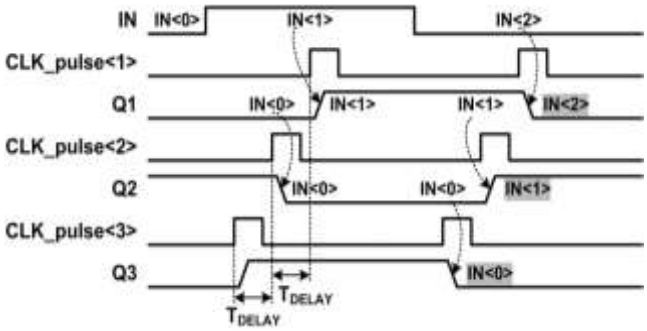

Fig. 2.6: Waveforms

Fig 2.6 demonstrates the task waveforms in the proposed move enroll. Five non-cover deferred beat clock signals are created by the postponed beat check generator in Fig 2.6. The succession of the beat check signals is on the contrary request of the five locks. At first, the beat clock flag CLK_pulse (T) refreshes the hook information T1 from Q4. And afterward, the beat clock signals CLK_pulse (1:4) refresh the four lock information from Q4 to Q1 consecutively. The hooks Q2– Q4 get information from their past locks Q1– Q3 yet the main hook Q1 gets information from the contribution of the move enroll (IN).

The activities of the other sub move registers are the same as that of the sub move enlist #1 with the exception of that the primary lock gets information from the impermanent stockpiling hook in the past sub move enroll. The suggested shift register diminish the number of delayed pulsed clock signals certainly, but it increases

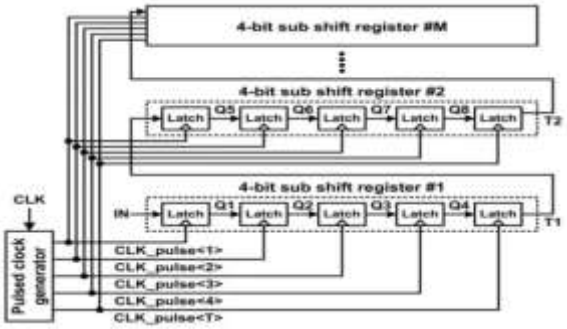

Fig 2.7: Block Diagram

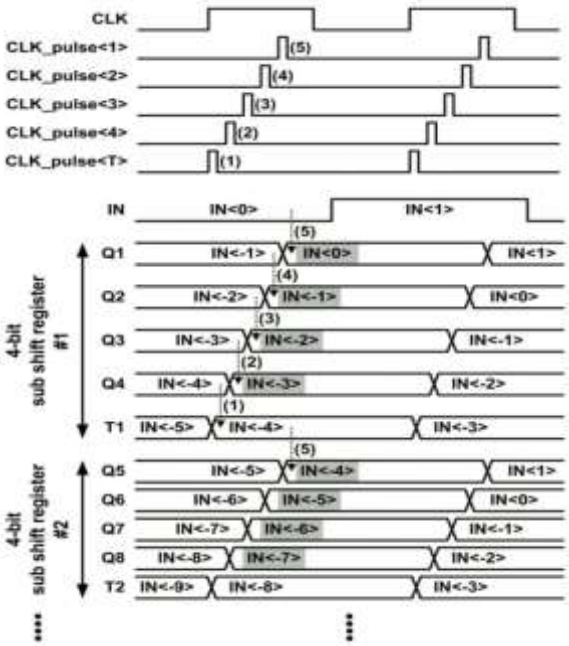

Fig 2.8: Waveforms

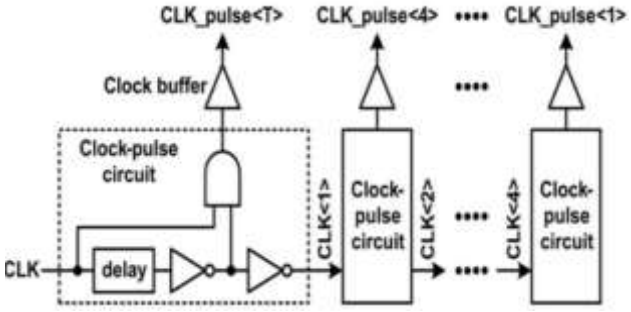

Fig 2.9: Pulsed Clock generator

The number of latches because of the supplementary temporary storage latches. As shown in Fig 2.9 each pulsed clock signal is generated in a clock-pulse circuit consisting of a delay circuit and an AND gate. When a shift register is divided into two sub shift registers, the number of clock-pulse circuits is the number of latches. A subshift register consisting of latches requires pulsed clock signals. The number of sub shift registers becomes, each sub shift register has a temporary storage latch. As a result, the latches are added for the temporary storage latches.

The normal delayed pulsed clock circuits in Fig 2.5 can be used to save the AND gates in the delayed pulsed clock generator in Fig 2.9. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. Though, the delayed pulsed clock generator in Fig 2.9 the clock pulse width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is produced from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals.

The quantities of hooks and clock-beat circuits change to give to the word length of the sub move enroll chose by thinking about the zone, control utilization, speed.

In a long shift register, a short clock pulse cannot finish a long wire due to parasitical capacitance and resistance. At the end of the wire, the clock pulse shape is degraded because of the rising and falling times of the clock pulse increase due to the wire delay. A simple solution is to increase the clock pulse width for keeping the clock pulse shape. But this decreases the maximum clock frequency. Another solution is to insert clock buffers and clock trees to send the short clock pulse with a small wire delay. But this increases the area and power overhead. Moreover, the multiple clock pulses make the more overhead for multiple clock buffers and clock trees.

2. RESULT

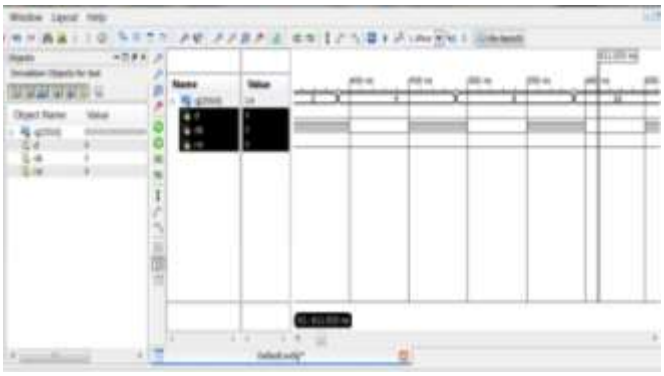

Fig. 3.1: Waveform of the Proposed shift register

The above figure shows the measured waveforms of the proposed 256-bit shift register. The system-level testing is performed with ISIM simulator for the Verilog code of shift register. The above figure shows the waveforms of proposed shift registers. Here the input is given through test bench and the 256-bit output is shown in the above-simulated waveforms

4. PERFORMANCE COMPARISION

Table 1: Comparison of the Existing method and the proposed method

Method name	Area	Delay	Power
	IOB's	Total Delay	Overall power
Flip- Flop based shift register (Existing)	259	4.134ns	39µw
Proposed Latch based shift register (Proposed)	256	4.047ns	38µw

The above table gives the comparison of existing method and proposed method. Here we compared both methods by taking the parameters area, power, and delay. By this analysis, the area and power consumption of the proposed shift register are compared to that of the conventional Shift register.

5. FUTURE SCOPE

SRAM is a type of semiconductor memory which is volatile in nature (retains the data as long as power is being supplied). It performs both read and write operations to store and fetch the data, based on the particular address. The read and write operations are controlled by the word line. Based on the bit line condition the data in it is stored and consists of one-bit latch to store the data.

6. CONCLUSION

A detailed performance analysis of Low Power and Area Efficient Shift Registers Using Pulsed Latches have been studied and presented in this project thesis. The Shift register using pulsed latches has been designed according to the modules in the block diagram. Each of these modules has been implemented, simulated and analyzed. Each of the modules was analyzed for the power consumption, delay, and area. Each module is synthesized and simulated using ISM tool.

Finally, Shift register design is analyzed based on simulation results and compared with the existing standard designs. This project work gives more insight and deeper understanding of Shift register to help the designers in making the choice which provides low power and efficient area

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