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# Design of hardened by design charge pump PLL

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## ABSTRACT

***The PLL is a feedback system used to generate clock signal in microprocessors, and frequency multiplication (FM) etc., The PLL consists of several components such as Phase frequency detector (PFD), Charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO) and frequency divider (FD) circuits. The struck at single-event-effects (SEEs) such as latch-up, single-event-transient and multiple bit upsets which affect the PLL performance. PFD and FD which are free from dead zone due to their digital characteristics but the CP are affected by SEEs which causes the CP output to be degraded and which affect the VCO input hence PLL will lose lock. The PLL and its components are implemented in cadence virtuoso tool using 180nm technology.***

**Keywords:** *PLL, PFD, CP, LPF, VCO, FD, SEEs, SET.*

## 1. INTRODUCTION TO PLL

The application of phase locked loop (PLL) is for clock recovery and clock generation in a microprocessor, networking, data communication and frequency multiplication. Due to increases in speed of circuit function, it requires a PLL circuit to operate at high speed. And thus PLL to operate in GHz frequency range with less lock time. The PLL is a simple feedback system it compares the phase and frequency of input and VCO output signal. PLL consists of a phase frequency detector (PFD), a charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO) and a frequency divider (FD) as shown in figure 1.

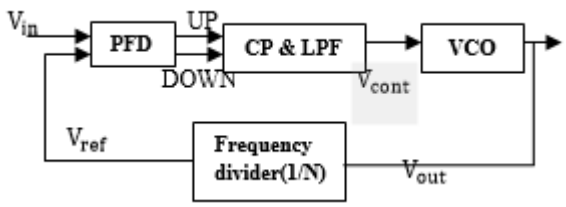



**Figure 1. Phase locked loop**

The PFD output is applied to the CPLPF and the output controlled voltage of CP is applied to the VCO and its output is feed as input to the PFD through FD. The single event effects in CP can be overcome by designing a single-event-transient hardened-by-design CP instead of traditional CP.

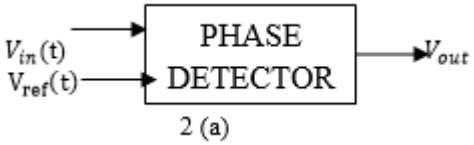
The PLL basically operates in three states as free running, capture, and locked range.

Free running: Before applying the input the PLL operates in the free running state. Capture: Once the input is applied VCO continues to change the output frequency and the device is in capture mode. Locked: The VCO continues to change the output frequency until its equal to the input frequency and the PLL is in a locked state.

## 2. ARCHITECTURE OF PLL

### A. Phase frequency detector (PFD)

Phase detector which works exactly as X-OR gate s the phase/frequency difference between two input varies then only it produces an output. The average output voltage which is directly proportional to the phase difference $\Delta\emptyset$ as shown in figure 2 and figure 3.




2 (a)

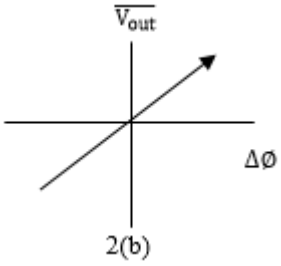



**Figure 2. Definition of the phase detector**

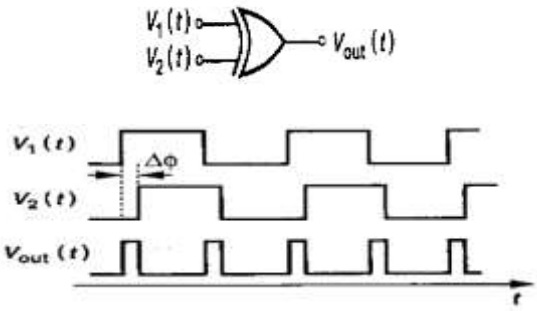



**Figure 3. Exclusive OR gate as a phase detector**

The Phase Frequency Detector (PFD) generate a phase error (UP/DOWN) signal by comparing the phase of the input signal with the VCO output signal. UP signal will be HIGH when the phase of input signal leads to VCO output signal otherwise DOWN signal will be HIGH. The generated pulse signal on the UP (DOWN) line, represents the phase difference between the leading edges of the inputs will activate the charge pump model to the source (sink) the current to (from) the low pass filter.

The PLL compares the phase of the applied input $V_{in}$ and the feedback $V_{ref}$, so the phase difference between the applied input $V_{in}$ and the feedback $V_{ref}$is expected to be invariable in the steady state. That is to say, when $F_{in}$and $F_{ref}$ does not change with time, the PLL is in lock state. Here, $F_{the\ in}$ and $F_{ref}$ are those phases of the input $V_{in}$ and the feedback signal $V_{ref}$ respectively. Therefore

$$\frac{\partial \emptyset_{ref}}{\partial t} - \frac{\partial \emptyset_{in}}{\partial t} = 0 \text{ -----Eq.1}$$

Where, $\emptyset_{in}$ is input phase

$\emptyset_{ref}$ is the reference phase

The gain of PFD is given by,

$$K_{PFD} = \frac{V_{DD}}{\pi} \text{ -----Eq.2}$$

$$= \frac{1.8}{\pi}$$

$$= 0.5729 \text{ V/ radians}$$

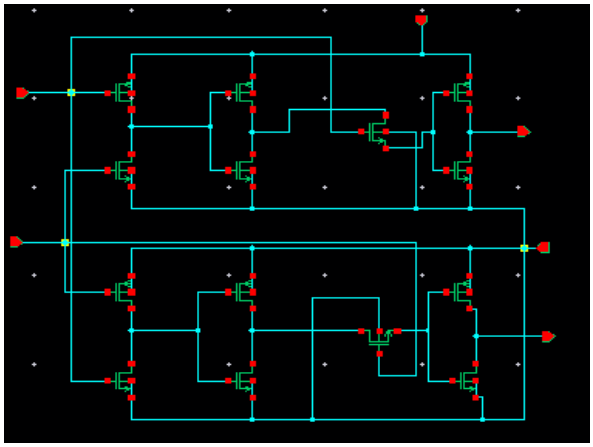


**Figure 4. Proposed PFD**

**B. The charge pump and low pass filter (CPLPF)**

The charge pump is an important part of PLL which converts the phase/frequency output of PFD into a voltage and given as input to the LPF. The LPF is used to remove the undesirable high-frequency components present in PFD output response and its output signal is applied as input control signal to the VCO. The charge pump consists of two switches it converts the up and down signals of the PFD into the current.

The charge pump output current is given by,

$$I_{CP} = K_{CP} \times \Delta\emptyset \text{ -----Eq.3}$$

$$\text{Where, } K_{CP} = \frac{I_{PUMP}}{2\pi} \text{ -----Eq.4}$$

$$\Delta\emptyset = \emptyset_{in} - \emptyset_{ref} \text{ -----Eq.5}$$

The loop is in lock condition when the phase difference $\Delta\emptyset$ is zero.

A SET on the CP causes a poverty of the output phase. The CP output is directly connected to the capacitor of LPF, so the charge collected by capacitor will directly affect the control voltage $V_{cont}$ of the VCO. And there is a frequency balance in the VCO, and which will cause the PLL to lose lock. Therefore, the SET on the CP will be mainly discussed here. To improve SET tolerance of the PLL, a SET-HBD-CP is discussed in this paper, as shown in figure 5.

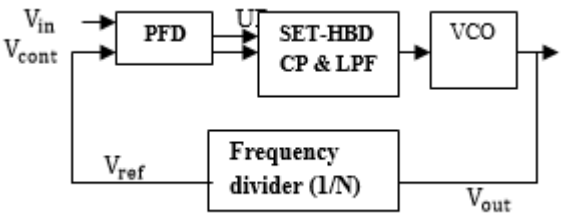



**Figure 5. Proposed SET-HBD PLL**

The SET-HBD-PLL is implemented by adopting the planned SET-HBD-CP instead of the conventional CP, and the architecture of the proposed SET-HBD-PLL is shown in figure 5. These modules including PFD, VCO and FD are entirely the same as that adopted in the PLL. The proposed SET-HBD-CP consists of a basic CP, a reference circuit, and a radiation-hardened circuit. The basic CP shown in

figure 6(a) consists of MOS transistors $M_1$~$M_8$ and amplifier$A_1$.

In figure 6(c), MOS transistors $M_9$ ~ $M_{14}$ and amplifier $A_2$ forms reference circuit, and which will provide bias voltages of the basic CP and the radiation-hardened circuit. MOS transistors $M_8$ and $M_{14}$, MOS transistors $M_7$ and$M_{13}$, MOS transistors $M_2$ and $M_{10}$ , and MOS transistors $M_1$ and $M_9$ have entirely the same width-length ratios respectively. The width-length ratio of MOS transistor $M_{12}$, and $M_{11}$ is two times that the width-length ratio of MOS transistor $M_6$ and $M_4$. Amplifier $A_2$ have high dc-gain and which forces the voltage $V_H$ of node H and the voltage $V_C$ of node C to be equal. It is concluded that $V_A = V_F$, $V_B = V_G$, $V_D = V_I$ and $V_E = V_J$. Here, $V_A$, $V_B$, $V_D$, $V_E$, $V_F$ , $V_G$ , $V_I$ and $V_J$ are voltages of node A, node B, node D, node E, node F, node G, node I, and node J respectively.

As shown in figure 6(b), MOS transistors $M_{C1}$~ $M_{C10}$ and resistor R1 forms the radiation hardened circuit. PMOS transistors $M_{C1}$~ $M_{C3}$ will determine whether nodes A ~ C of the basic CP are struck by SE and whether the radiation-hardened circuit starts to work. At the same time, MOS transistors $M_{C6}$~ $M_{C8}$ will determine whether node E, node D and node C of the basic CP are struck by SE Resistor R1 is adopted to isolate $V_{cont}$ from the output node C of the CP. Therefore, resistor R1 will also restrain the SET current into the LPF and reduce the perturbation of the voltage $V_{cont}$. MOS transistors $M_{C4}$- $M_{C5}$ and $M_{C9}$- $M_{C10}$ form the current mirror pairs respectively. When the basic CP shown in figure 6(a) is not struck by SE, all gate-source voltages of PMOS transistors $M_{C1}$~ $M_{C3}$ and NMOS transistors $M_{C6}$~ $M_{C8}$ are equal to zero. Current mirror pairs $M_{C9}$- $M_{C10}$ and $M_{C4}$- $M_{C5}$ work, and the SET-HBD-PLL is in normal mode. However, when a SE strikes on the basic CP nodes and whose voltage will increase or decrease. At the same time, all node voltages of the reference circuit shown in figure 6(c) are almost stable. These corresponding MOS transistors of the radiation hardened circuit shown in figure 6(b) will work and provide the return current so as to recompense the additional charge of the struck node.

For example, MOS transistor $M_{C1}$ is turned on when a SE strikes on the drain of MOS transistor $M_8$. The drain current of trthe ansistor $M_{C1}$is mirrored by cura rent pair $M_{C4}$- $M_{C5}$, and the drain current of transthe istor $M_{C5}$ will recompense the loss charge of capacithe tor in the LPF.

Similarly, when drains of transistor $M_7$ and $M_6$ are struck by SE, the transistors $M_{C2}$ and $M_{C3}$ are turned on respectively and the drain current of tranthe sistor $M_{C5}$ will recompense the loss charge of capacthe itor in the LPF. When drain of transistors $M_1$~ $M_2$ and $M_4$ are struck by SE, transistors $M_{C6}$~ $M_{C8}$ are turned on respectively and the drain current of transistorthe $M_{C10}$will recompense the loss charge of capacitor ithe n the LPF. Then, the perturbation of voltage $V_{cont}$ will be restrained, so PLL can quickly return to the lock state.

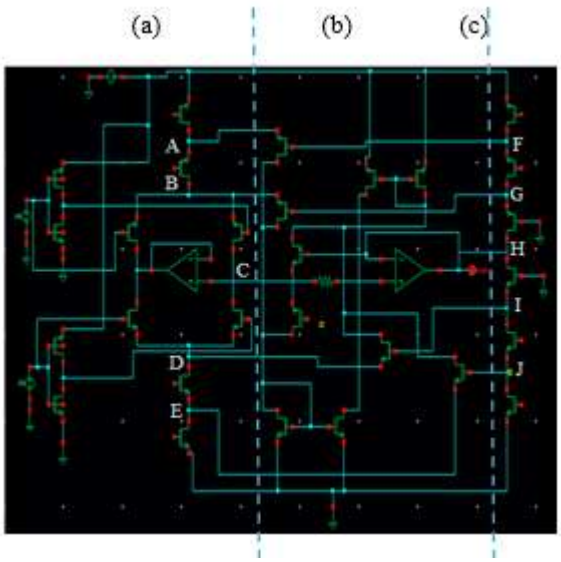



**Figure 6. The proposed SET-HBD-CP**

**(a) Basic CP (b) radiation-hardened circuit (c) reference circuit**

**C. Voltage controlled oscillator (VCO)**

A voltage controlled oscillator generates an output signal with respect to its control voltage. The frequency of the output voltage is frequently relative to the control voltage. The control voltage is from the Loop Filter. If the input voltage rises the VCO produces an output with a higher frequency and vice versa. In the locked state control voltage becomes stable, thus the output frequency of the VCO clock is also fixed.

A current starved VCO consists of an odd number of inverter stages. Here five-stage current starved voltage controlled oscillator (CS-VCO) [5] is used it will generate a sinusoidal oscillation and the last inverter is used to translate sinusoidal wave into a square wave. The output node of the last inverter is linked to the input node of the first inverter and the schematic diagram of five-stage CS-VCO is as shown in figure 7.

The VCO input voltage is given by,

$$V_{VCO} = K_f \times I_{CP} \text{ -----Eq.5}$$

Where,

$K_{CP}$ is charge pump gain
$K_f$ is low pass filter gain

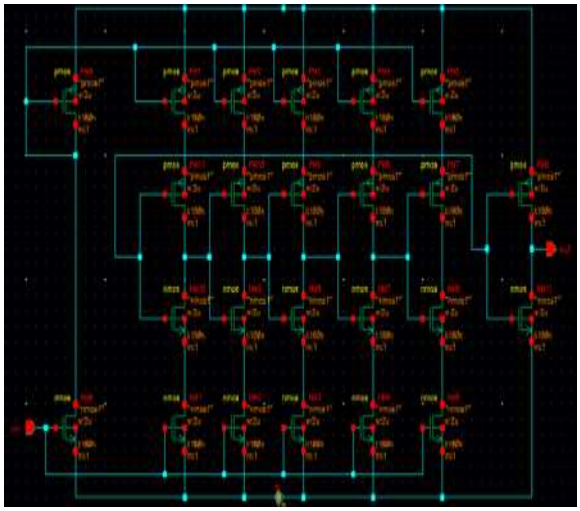


**Figure 7. Proposed five-stage CS-VCO**

### D. Frequency divider (FD)

A frequency divider is used in the feedback path to divide the output frequency of VCO and send the signal as a one of the input to the phase frequency detector. A simple D-flip flop is used as a frequency divider. A designed FD is as shown in figure 8.

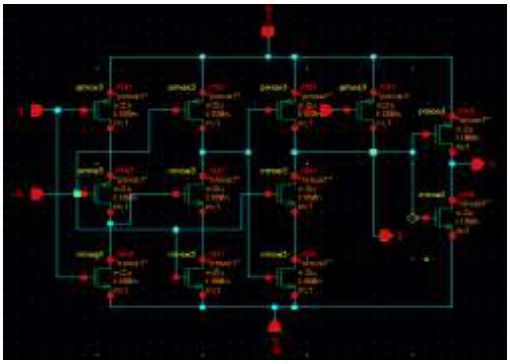


**Figure 8. Proposed Divided by 2 Frequency Divider**

## 3. RESULTS AND DISCUSSION

The PFD compares the input and VCO frequency and generates a dc response voltage which is proportional to the phase difference between the two input frequencies. The PFD generates two output signals UP and DOWN as shown in figure 9, that switches the charge pump.

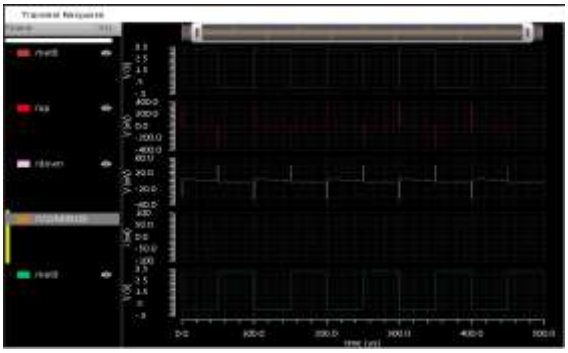


**Figure 9. Transient response of PFD**

The charge pump is a circuit used to combine both the UP and DOWN outputs of the PFD and give a single output which is fed to the input of the LPF. The LPF is used to convert back the charge pump current into the voltage and the simulation result for SETCP LPF is as shown in figure 10 & 11. The output voltage of LPF controls the VCO response.

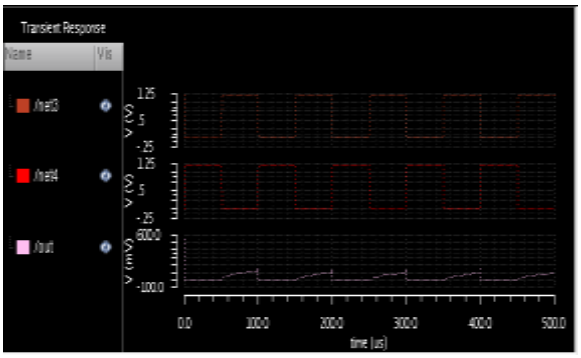



**Figure 10. Transient response of SET CP with LPF**

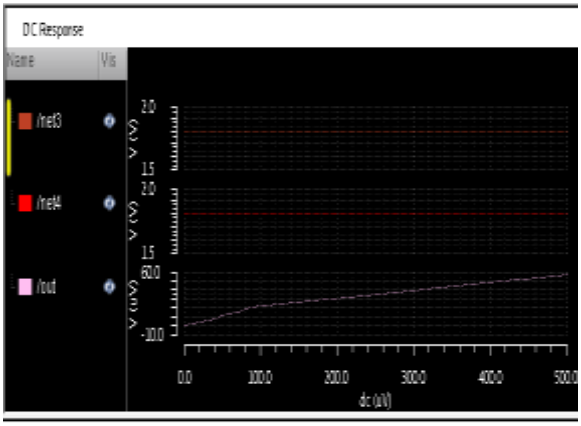



**Figure 11. DC response of SET CP with LPF**

The characteristic curve of CS-VCO is as shown in figure 12. The CS-VCO gain is given by,

$$K_{VCO} = \frac{f_{max}-f_{min}}{V_{max}-V_{min}} \quad \text{-----Eq.6}$$

$$= \frac{1M-0.1M}{1.8-1.2}$$

$$= 1.5$$

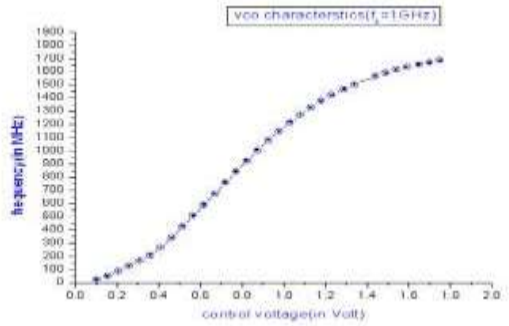



**Figure 12. Frequency vs input voltage for 5 stage CS-VCO**

The output of the VCO is given as an input to the frequency divider circuit. Which forms a closed loop. Here divide by 2 frequency divider is used. The output waveform of the divider is as shown in figure 13.

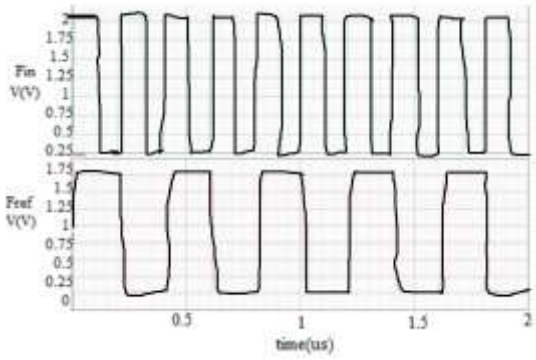



**Figure 13. Divided by 2 Frequency divider waveform**

**Table 1. Design parameters**

| Parameter | Result |
|---|---|
| Technology | 180nm |
| VDD | 1.8V |
| Frequency | 1GHz |
| Transistors W/L ratio | 2um/180nm |
| Supply voltage | 1.8 V |
| Capacitor | 10pF |
| Resistor | 10KΩ |
| Power dissipation | 500mW |

## 4. CONCLUSION

Here the PLL with a better lock time is designed in cadence virtuoso 180nm technology using GPDK180 library. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. By properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values we can achieve a better lock time.

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