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## Study of low-noise amplifier in CMOS technology

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### ABSTRACT

*This paper presents the reviews of few previous works for low noise amplifier design (LNA). This paper will explore several architectures of LNA that focus on the frequency optimization of LNA. Besides, high gain, low noise, input and output matching are also reviewed. As to provide extremely low power and also optimized all characteristics aspects, the performance of each topology is discussed. Also, some basic LNA topologies are also reviewed.*

**Keywords:** Low noise amplifier, Gain, Noise figure, Impedance matching.

### 1. INTRODUCTION

Low noise amplifier (LNA) is the first component of any receiver front-end circuitry, on which receiver performance depends. It is the first amplifying block of the front end. Since the signals received from the antenna is very weak  $\sim 1\mu\text{Vp}$ . LNA is first to gain stage, which boosts the weak input signal from antenna without degrading the signal-to-noise ration (SNR). The key role of LNA is the amplification process. LNA is very simple from topology point. For industrial use, NMOS transistors are used in the design, by incorporating all components on the single chip. A broadband LNA must provide good input matching, appropriate power gain, and low noise figure (NF) over a multi-GHz bandwidth (BW), low-power consumption. Several CMOS LNA design techniques have been reported for ultra-wideband communication applications. Wireless communication technologies develop rapidly causing high requirements in performance of RF receiver. As the LNA is the first stage in a receiver circuit, several requirements needs to be fulfilled which results in a good system performance for overall circuit design. Such requirements are low power consumption, high gain, low noise figure, input and output matching especially noise that affected the receiver performance to a large extent. With the rapid proliferation of battery-operated wireless applications, such as smart phones, watches, and implantable devices, the demand for low-power and cost effective radios has increased significantly. In particular, in the case of wireless sensor networks (WSNs), power consumption is the most critical issue and in some cases is more important than their performance or even cost

### 2. TOPOLOGIES

#### 1) Forward Body Bias:

Due to the simplicity of the forward body bias technique; it is used in this topology as to lower down the value of power consumption of the LNA [10].

Bandwidth: 2.4GHz

Supply Voltage: 0.6V

Noise Figure (NF): 2.88dB

Gain: 10.1dB

Power Consumption: 0.84mW

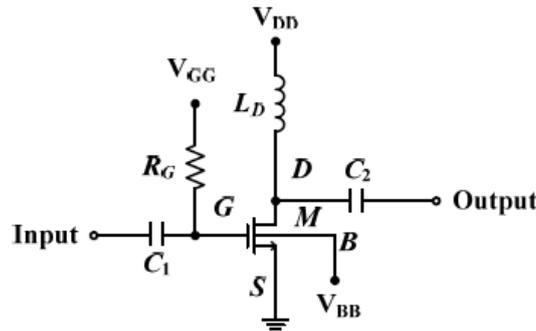


Fig.1. Schematic of LNA with a forward body bias technique

2) Self-Biased Inverter

One of the effective ways to minimize the LNA power is biasing the transistor in weak inversion areas. Hence, the value of  $g_m/I_D$  becomes higher. In order to gain acceptable gain, the low transconductance ( $g_m$ ) requires active low topologies. Based on the figure below, self-biased inverter gives the largest gain bandwidth if compared to single stage transistor. The total transconductance,  $g_{mT}$ , of self-biased is almost twice of the single transistor. Better linearity can be accomplished by varying the biased voltage on the gate. Via the feedback resistor, the input biased of the self-biased inverter can be set. Hence the value can be set by varying the size of NMOS and PMOS Transistor.

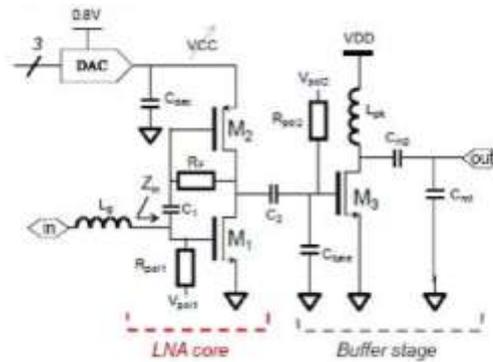


Fig.2. a simplified schematic based on self-biased

Bandwidth: 2.4GHz  
 Power Consumption: 60μW  
 Supply Voltage: 0.4V  
 Noise Figure (NF): 5.3dB  
 Gain: 13.1dB  
 CMOS Technology: 0.13μm

3) Common Source Cascade

The general circuit topology for LNA circuit core is the cascade amplifier. The achievement of high-input impedance and low-noise figure due to the Miller effect (normally refers to capacitance, any impedance connected between the input and another node exhibiting gain can modify the amplifier input impedance via this effect) make it suitable for this proposed LNA design[10].

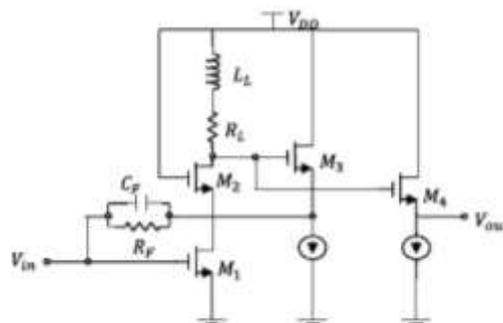


Fig.3. LNA circuit topology

Functioning:

$R_F$ :  $50\Omega$  impedance matching

$C_F$ : avoid overshoot in the frequency response of LNA

$M_1$ : Gives impact on noise figure.

#### 4) Cascode

The commonly used designing architecture is cascode. The main advantage of the cascode is it reduces the Miller effect, block the effects of the limited output impedance and provide a good reverse isolation.

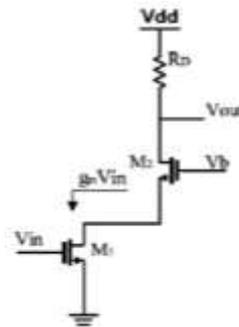


Fig.4. the cascode structure

Due to advantage of low noise figure, high gain, good linearity and good input impedance matching, the below schematic is widely used in wireless transceiver systems.

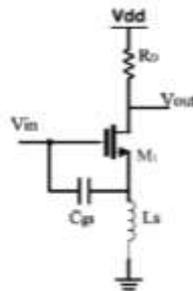


Fig.5. Common source amplifier with negative feedback of source

### 3. IMPEDANCE MATCHING

The input and output impedance matching networks in the circuit play an important role in the design for improving all the transistors have a complex input and output impedance, whereas the input and output impedance of the circuit is always 50 ohms. To fulfill the condition of maximum power transform theorem, there must be impedance matching network between the terminations and the transistor. Fig. elaborates the concept. According to the diagram,  $T_S$  must be the conjugate match of the input impedance of the transistor. Similarly,  $T_L$  should be the conjugate match of the output impedance of the transistor.

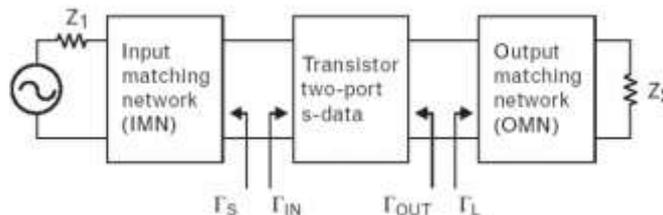


Figure. Impedance matching network

The input impedance matching network is for noise optimization. Ell matching network (also denoted as L matching network) is an arrangement of inductors and capacitors in the combinations of one in series and the other in parallel and vice-versa. The impedance of the network in this type keeps changing at every node. The Ell match obtained is optimized for the NF requirement of  $< 1$  dB.

### 4. NOISE PARAMETERS

Although many parameters specify an amplifier's noise performance, the two most important factors are voltage noise and current noise. Voltage noise is the voltage fluctuations at the input of an otherwise noise-free amplifier with shorted inputs. Current noise is the current fluctuations at the input of an otherwise noise-free amplifier with open inputs.

The typical figure of merit for amplifier noise is noise density, also called spot noise. Voltage-noise density is specified in  $nV/\sqrt{Hz}$ , while current-noise density is usually shown in units of  $pA/\sqrt{Hz}$ . These values are provided in all low-noise amplifier data sheets, and are usually specified at two frequencies: at less than 200Hz for the flicker-noise component, and at 1kHz for the flat-band component. For simplicity, these measurements are referred to the amplifier inputs to remove the need to account for the amplifier's gain.

### Calculating Total Noise

The standard expression for an op amp's total input-referred noise at a given frequency is:

$$e_t = \sqrt{e_n^2 + (R_p + R_n)^2 i_n^2 + 4kT(R_p + R_n)}$$

Where:

$R_n$  = Inverting input effective series resistance

$R_p$  = Noninverting input effective series resistance

$e_n$  = Input voltage-noise density at the frequency of interest

$i_n$  = Input current-noise density at the frequency of interest

T = Ambient temperature in Kelvin (°K)

k =  $1.38 \times 10^{-23}$  J/°K (Boltzman's constant).

### Effect of Amplifier Design on Noise Performance

Noise performance is a function of the amplifier design. The three common designs for low-noise amplifiers are bipolar, JFET-input, and CMOS-input. While each design can provide low-noise performance, their performances are not equal.

## 5. BANDWIDTH ADVANCEMENTS

Over the years, there has been advancements in the frequency of the Low-Noise Amplifier to a great extent. In the early days, Low-Noise Amplifiers had a 1-3 GHz frequency but as the higher frequencies are being tested in the field of communication, there has been a meteoric increase in the frequency of the device. Now, LNAs with frequency of more than 60GHz is available in the market.

## 6. REFERENCES

- [1] Design of CMOS Low Noise Amplifier for 1.57GHz, Namrata Yadav, Abhishek Pandey, Vijay Nath
- [2] CMOS Low-Noise Amplifier Design Optimization Techniques Trung-Kien Nguyen, Chung-Hwan Kim, Gook-Ju Ihm, Moon-Su Yang, and Sang-Gug Lee
- [3] Design of Low Noise Amplifier for Multiband Receiver Sriganayathri.y1, M.S.Yasanthi2
- [4] CMOS RF Low-Noise Amplifier Design for Variability and Reliability Yidong Liu and Jiann-Shiun Yuan, Senior Member, IEEE
- [5] 1 to 3 GHz Wideband Low Noise Amplifier Design, Abhay P. Kulkarni
- [6] A Review of LNA Topologies for Wireless Applications ,Anishaziela Azizan, S.A.Z. Murad, R.C. Ismail and M.N.M. Yasin
- [7] A Low power UWB CMOS Low Noise Amplifier for 3.1-10.6 GHz in Receivers, Amir. Mahdavi Fatemeh .Geran
- [8] A Wideband Low Power Low-Noise Amplifier in CMOS Technology Ali Meamar, Student Member, IEEE, Chirn Chye Boon, Kiat Seng Yeo, Member, IEEE, and Manh Anh Do, Senior Member, IEEE
- [9] 26–42 GHz SOI CMOS Low Noise Amplifier, Frank Ellinger, Member, IEEE
- [10] A Review of LNA Topologies for Wireless Applications Anishaziela Azizan, S.A.Z. Murad, R.C. Ismail and M.N.M. Yasin
- [11] J. Borremans, L. De Locht, P. Wambacq, and Y. Rolain, Nonlinearity analysis of Analog/RF circuits using combined multisine and volterra analysis, in: Proceedings of the Design, automation and test in Europe Conference and Exhibition, 2007, pp. 261–266.
- [12] Pranav C Pattewar, Performance Comparison of Various Low Noise-High Speed Amplifier Topologies for GPS Applications, International Journal of Current Engineering and Technology. 4 (1) (2014), 426-429.
- [13] Bosco Leung, VLSI for Wireless Communications, Prentice Hall Electronics and VLSI series, Springer, New York, 2011.
- [14] B. Razavi, T. Aytur, C. Lam, F.-R. Yang, K.-Y. Li, R.-H. Yan, H.-C. Kang, C.-C. Hsu, and C.-C. Lee, "A UWB CMOS transceiver," IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2555–2562, Dec. 2005.
- [15] J. Long, "Monolithic transformers for silicon RF IC design," IEEE J. Solid-State Circuits, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.