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A Review Paper on I2C Communication Protocol

Vivek Kumar Pandey
pandeyvivek2010@gmail.com
IMS Engineering College, Ghaziabad, Uttar Pradesh

Sparsh Kumar
mightykhanna@gmail.com
IMS Engineering College, Ghaziabad, Uttar Pradesh

Vimal Kumar
15995vimal@gmail.com
IMS Engineering College, Ghaziabad, Uttar Pradesh

Pankaj Goel
pankajgoel80@gmail.com
IMS Engineering College, Ghaziabad, Uttar Pradesh

ABSTRACT

The I2C communication protocol is a well known and famous serial communication protocol developed by Philips Semiconductor (now NXP Semiconductor) in the 1980s (nearly 25 years ago) to exchange information specially between slow and fast devices. It consists of only two wires SDA and SCL and its ability to transmit data without loss makes it simpler and cheaper than other protocols. This paper is focused and aimed to present the valuable research work about I2C protocol by different researchers over the years.

Keywords: *SDA, SCL, Master, Slave, I2C, Verilog HDL, Protocol, ACK, NACK.*

1. INTRODUCTION

In today's technological world, many applications such as auto mobiles, laptops, embedded devices and other peripherals need to connect multiple devices. We also need to make them able to communicate with each other and this requirement gives rise to the need for any medium or channel which can act as a bridge between these peripherals to share data or information. There are many communication protocols for this purpose. One of them is Inter-Integrated circuit (I2C or IIC) protocol.

I2C has two-wires named SDA (serial data line) and SCL (serial clock line), the bidirectional serial bus that provides a simple and efficient communication between devices. It is multi-master and multi-slave protocol but single-master and the multi-slave combination are mostly used. Master is a device which initiates transactions and generates a clock signal. The slave is a device which is being addressed by the master.

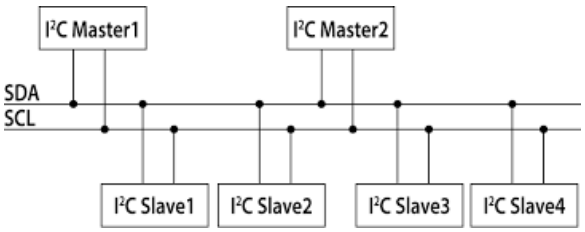

Figure 1: I2C Multi-Master Multi-Slave Configuration

Transmission of data over the I2C bus is divided into 7 states:

1.1 Start Condition: SDA line goes from high logic to low logic while SCL line remains at high logic. This is called "start signal"[1].

1.2 Slave address and R/W bit: 7-bit address of target slave is transmitted with one additional bit called R/W which defines the direction of data so total 8-bit are transmitted. Now slave will generate a signal (ACK or NACK) to acknowledge master [1].

1.3 Data Transfer: 8-bit data is transmitted over SDA line in an order such that MSB is transmitted first and LSB at last. An acknowledge signal is again generated by the slave when a byte (8-bit) is received from mater and again next byte of data is transmitted again depending upon the requirement and acknowledge signal is generated by the slave for every byte of data [1].

1.4 Stop Condition: SDA line goes from low logic to high logic and SCL line remains high, this is called as "stop signal"[1].

NOTE: When no data is transmitted between master and slave then SDA and SCL lines are at high logic, this is called ideal state [1].

The I2C interface has 3 modes of operations and transmission rate is different for each mode [1]:

- Normal mode - 100kbps
- Fast mode - 400kbps
- High-speed mode - 3400kbps

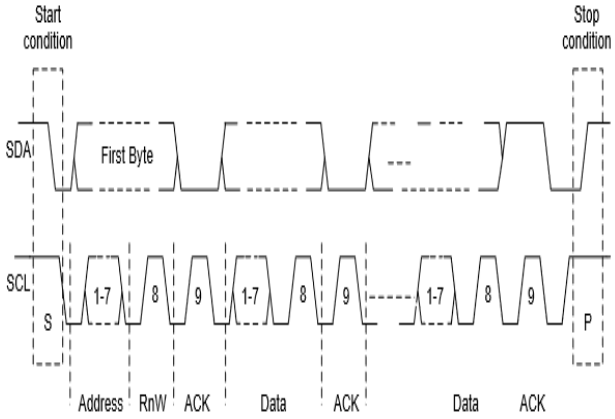

Figure 2: Data Transaction States

2. LITERATURE SURVEY

Researchers over the years have used Verilog HDL and VHDL language to design the I2C communication protocol. I2C is a standard protocol to exchange information, so it's working and designed properties are almost similar.

I2C or IIC is a multi-master multi-slave serial communication bus invented by Philips semiconductor in the 1980s and is generally used for communication in between high-speed devices and low-speed devices. The various applications of I2C–bus are in various control architectures like System management bus (SMBus), Power Management bus (PMBus), Intelligent Platform Management Interface (IPMI), Display Data Channel (DDC), and Advanced Telecom Computing Architecture (ATCA). All devices connected to the SDA and SCL wires must have an open drain or open collector outputs. Exchange of data between master and slave is synchronous to SCL on the SDA line byte by byte wise. The data frame is 8 bit (1 byte) long, with one SCL clock pulse for each data bit with MSB being transmitted first followed by an acknowledge bit for each transferred byte. The ideal I2C bus is well known for its high performance, flexibility and low cost in the market [1].

This paper focuses on the software implementation of the I2C bus and its interfacing with RAM. UART, CAN, SPI, USB and I2C are several serial interfaces. Serial interfaces are used in communication between sensors and PC, several embedded peripherals such analog to digital and digital to analog converters with PC or system. USB, SPI, and UARTS are a point to point protocols, USB used multiplexers to communicate with other devices. Only I2C and CAN use software addressing and I2C is very easy to design and handle as it is small in size, easy to install as only 2 wires (SDA & SCL) are in the I2C bus. In this paper, the I2C controller is considered as master and SDRAM as a slave. The data transaction takes place in 4 steps, START signal generation, slave address (7 bit) is transferred with one more bit known as R/W bit, Third state is data (8 bit) transfer to slave or taking data from slave depending upon operation followed by an acknowledge bit and finally STOP signal generated by master to terminate the transaction. The code of I2C master is written in VHDL and compiled on Xilinx ISE 14.5 simulation tool [2].

This paper is about the development and implementation of I2C and SPI protocol, with different modes of operation on FPGA using Verilog HDL with the 14.7 version of software Xilinx ISE Design suit. I2C and SPI protocols are most famous for the interaction and exchanging data among peripherals. I2C can be a single master single slave or multi-master multi-slave communication protocol. I2C has a particular bit called R/W (called read or write bit) bit which tells whether master wants to read the data from slave or wants to write data to the slave. The master transmits the 7 or 10 bits of the address of slave along with R/W bit according to read or write operation to be performed followed by 8 bit of data. For the implementation of the I2C protocol on FPGA, the frequency of SCL line was 396 KHz, SDA line is bidirectional. The exchange of information between master and slave begins with a START condition followed by the 7 or 10 bit of address of targeted slave followed by R/W bit followed by an ACKNOWLEDGE bit (ACK) or NOT ACKNOWLEDGE bit (NACK), which confirms whether the transaction was successful or not. After this 8-bit data is sent to slave or received at master followed by ACK or NACK bit again and the transaction is finished by STOP condition. The Verilog HDL coding of I2C implementation is more burst and complex than SPI protocol [3].

This paper focuses on optimization of I2C. I2C is communication protocol, has several modes of operations which are used according to the need and application. Chip select or arbitration logic is absent in I2C, makes it cheaper and simple to implement. I2C is having only two wires SDA and SCL, together with both transmit the 7-bit address of targeted salve followed by one control bit for reading or write operation (R/W) and 8-bits of data. Both lines will have high logic when there is no any transmission between master and slave. I2C master is having a bit and byte controller, interfacing registers, clock divider, etc receive commands and data from external source. Serial clock and data, the status signal is generated by a top module of I2C. The conclusion of this paper is that I2C allows faster devices to communicate with slower devices without data loss. Controllability, less power consumption, small size are some merits of I2C protocol [4].

In this paper, the author has designed the I2C controller bus using Verilog HDL in Xilinx 12.2, used as an interface in between EEPROM (24C02) and system level interconnect is minimized. Author has covered only 7-bits of address slaves, not 10-bits address in this paper. For an EEPROM (24C02) the 4 MSB's are fixed at 1010 and hence rest 3 can be programmed therefore 8 EEPROM (24C02) can be connected as 2^3 = 8 addresses. To select the slaves, we send 7-bit address of slave followed by R/W bit so total 8-bits or 1 byte over SDA line. after it the internal register number in which user wants to write to is selected and finally, 8-bit data is transmitted over SDA line and after it STOP signal or sequence is generated at last of transmission. in this paper FPGA is considered as master and EEPROM as a slave, I2C is easy to implement. I2C is flexible and any FPGA or MICROCONTROLLER can communicate with I2C devices even it has no special I2C interface [5].

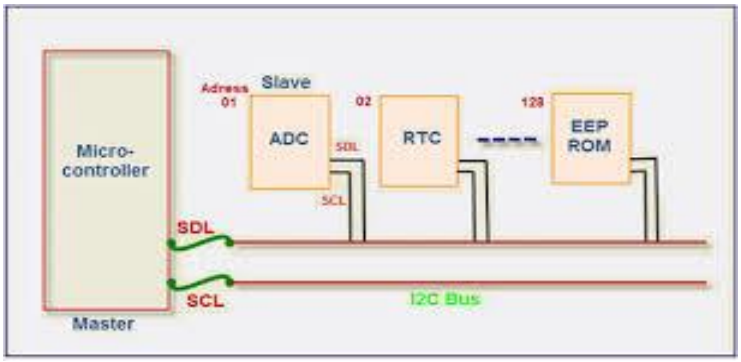

Figure 3: ADC, RTC, and EPROM as a slave on Common I2C bus

In this paper author has proposed the I2C master controller with multiple slaves, the design is done using Verilog HDL and simulated and synthesized in Questa-sim 10.0c and finite state machine (FSM) concept is used. During communication between master and slave master initiates the transaction and after START signal it transmits the 7-bit address along with a R/W bit over SDA line. The slave with which the 7-bit address matches with, that slave acknowledge the master by generating a signal (ACK). The R/W bit decides whether data will be written to that slave or read from slave by the master. This paper shows that I2C master can communicate with more than one slave, all connected through SDA and SCL lines [6].

In today's world where the physical size of the chip is going small and small year by year, a less amount of pin for serial data transfer is required. Protocols like RS-232, RS-422, SPI requires more pin connections in the IC. Also, other protocols like these protocols and mostly UARTS are all just 'one point to one point' data transfer bus systems. These protocols use data path multiplexing to perform communication. So to overcome these problems, the I2C protocol was introduced by Phillips semiconductor with only two physical wires, fewer pins connections, compact and small size. Author of this paper has used FSM for designing of the single I2C master using Verilog HDL, and simulated on ModelSim[9].

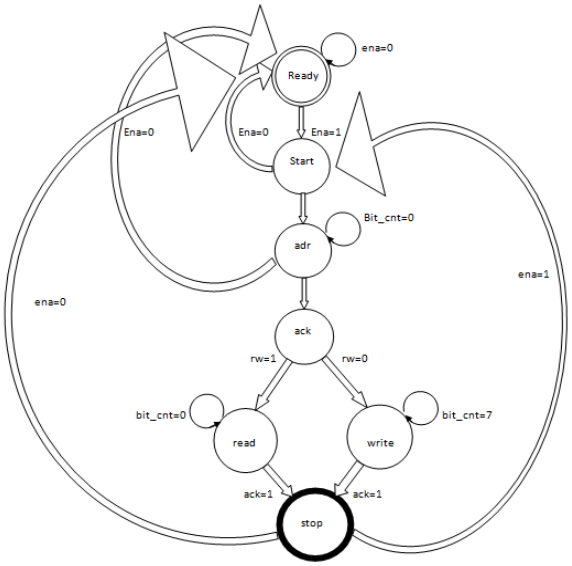

Figure 4: Finite State Machine for Design of Single Master [9]

3. CONCLUSION

This paper presents the view of many researchers along with the authors of this paper too. I2C is multi master and multi-slave bus and very useful for communication between fast and slow devices. I2C is also easy to design and implement either using Verilog HDL or VHDL language. It is an industry standard protocol which is widely used in various applications such as accessing real-time clocks, accessing low-speed DACs and ADCs, controlling small OLED or LCD displays, etc.

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5. BIOGRAPHIES

1. Vivek Kumar Pandey is currently pursuing his B.tech degree in Electronics and Communication stream from IMS Engineering College, Ghaziabad. He is born and grown in district MAU (U.P). His date of birth is 28 December 1996. He has done his schooling from Little Flower Children School, MAU (U.P). His field of interest is to work in electronics domain where he can apply his knowledge and skills to explore and develop himself.

2. Vimal Kumar is studying in IMS Engineering College, Ghaziabad. He is pursuing his B.tech degree in Electronics & Communication branch. He is born on 15th October and His hometown is in district Bareilly (U.P) and he completed his 10th and 12th from Army Public School, Meerut. He wants to get a reputed job after his graduation.

3. Sparsh Kumar is born on 25th July 1997 in district Rampur (U.P). He has done his schooling from Dayawati Modi Academy, Rampur. Currently, he is pursuing his B.tech degree in Electronics and Communication stream from IMS Engineering College, Ghaziabad.

