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FPGA – Based Electro Cardio Graphy Signal Analysis System using Least Square Linear Phase Finite Impulse Response Filter

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ABSTRACT

Proposed design for analyzing electrocardiography (ECG) signals. This methodology employs high pass least-square linear phase finite impulse response (FIR) filtering technique to filter out the baseline wander noise embedded in the input ECG signal to the system. Discrete wavelet transform (DWT) was utilized as a feature extraction methodology to extract the reduced feature set from the input ECG signal. The design uses back propagation neural network classifier to classify the input ECG signal. The system is a simulation on Xilinx system generator.

Keywords: *Electrocardiography (ECG), Discrete Wavelet Transform (DWT), FPGA, DSP, Bio-Medical Applications.*

1. INTRODUCTION

In recent years, cardiovascular disease, including heart disease and stroke, remains the leading cause of death around the world. Yet most heart attacks and strokes could be prevented if some method of pre-monitoring and pre-diagnosing can be provided. In particular, early detection of abnormalities in the function of the heart can be valuable for clinicians. Studying the electro cardiogram (ECG) signal provides an insight to understand life-threatening cardiac conditions. This typically is centered on the study of arrhythmias, which can be any disturbance in the rate, regularity, and site of origin or conduction of the cardiac electric impulse. Not all arrhythmias are abnormal or dangerous but some do require immediate therapy to prevent further problems. A subject's ECG information can be recorded using a portable Holter monitor which is worn by the subject. A Holter monitor typically employs a few electrodes and stores a recording of the subject's heart rhythm as they go about their daily activities over a 24–48 h period. The Holter monitor is then returned to a cardiologist who examines the recordings and determines a diagnosis. Examining these recordings is a time-consuming and hence any automated processing of the ECG that assists the cardiologist in determining a diagnosis would be of assistance. The basic problem of automating ECG analysis occurs from the non-linearity in ECG signals and the large variation in ECG morphologies of different patients. And in most cases, ECG signals are contaminated by background noises, such as electrode motion artifact and electromyogram-induced noise, which also add to the difficulty of automatic ECG pattern recognition. Many types of research depend on digital signal processing (DSP) techniques as a methodology to design automated ECG signal analysis systems. Most DSP systems use typical main stages for analyzing ECG signals; those main stages include de noising stages, feature extraction stages, and classification stages. This work discusses the problem of analyzing of electrocardiography (ECG) signals. A new system for analyzing ECG is presented. This system uses least-square linear phase FIR filter (LLFE) methodology to overcome the limitations of the previous methodologies.

2. EXISTING ECG SIGNAL QUALITY ASSESSMENT SYSTEM

In the existing system, an image-based electrocardiographic quality assessment technique has been utilized so that clinicians annotate ECG signal quality. But the outcome leads to a more fragile ECG based diagnosis of various cardiovascular conditions. So this method implies a denoising ECG signal which can only be implemented in MATLAB.

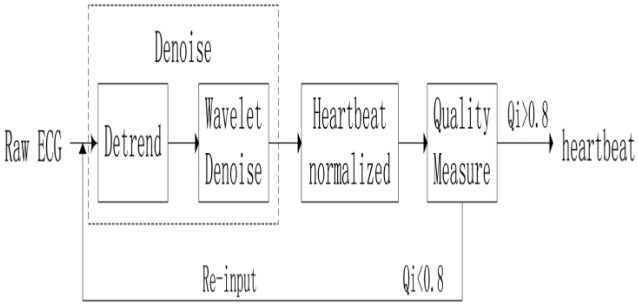


Fig 1. Existing ECG Signal Block Diagram

3. PROPOSED ECG SIGNAL ANALYSIS SYSTEM

The block diagram of the proposed design is shown in Fig. 1. The block diagram consists of three main blocks: de noising block, feature extraction block, and classifier block. Different blocks are described in the following subsections. The proposed design LLFE depends on classifying the input ECG signal into normal or abnormal ECG signal after passing through the three circuit main blocks, the result of this diagnosis can be sent further to a health caring professionals or remote health caring centers, to provide the required assistance. LLFE employs the basic blocks for a typical pattern recognition system.

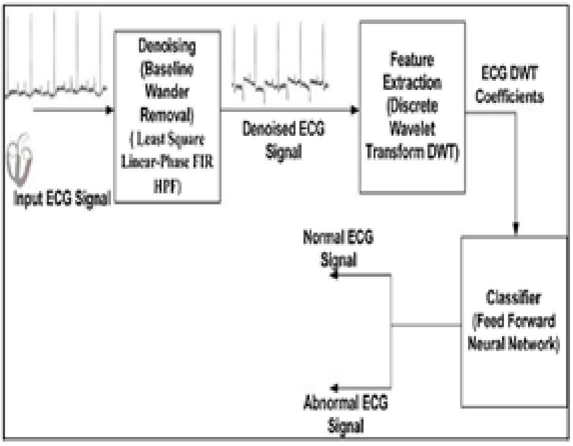


Fig 2.Block Diagram of Proposed LLFE Design

A. Input ECG Signal Acquisition

The input ECG signals to the proposed design are extracted from the standard MIT-BIH Arrhythmia Database normal/abnormal ECG beats based on MIT-BIH database that is considered are classified, such beats are considered to be processed using the discrete wavelet transform block. Each signal in the table is referenced from the MIT-BIH database by selecting the target database (MIT-BIH Arrhythmia Database (MITDB)) that contains the selected records. The records are digitized at 360 samples per second per channel with 11-bit resolution over a 10 mV range. Those records are fed to the de noising block to start the processing of the acquired ECG signals.

B. Denoising Block

In this block, ECG signals suffer from two main types of noise: (1) Low-frequency noise represented in baseline wander noise, (2) High-frequency noise such as power-line interference noise and muscle contraction. In LLFE, high-frequency noise is removed by discarding the first detail component resulting from the wavelet transform decomposition in the feature extraction block as will be discussed later.

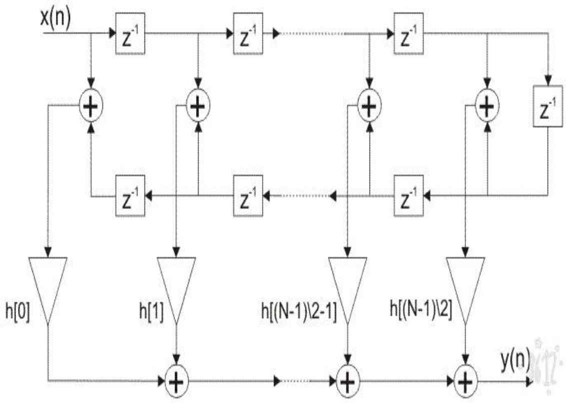
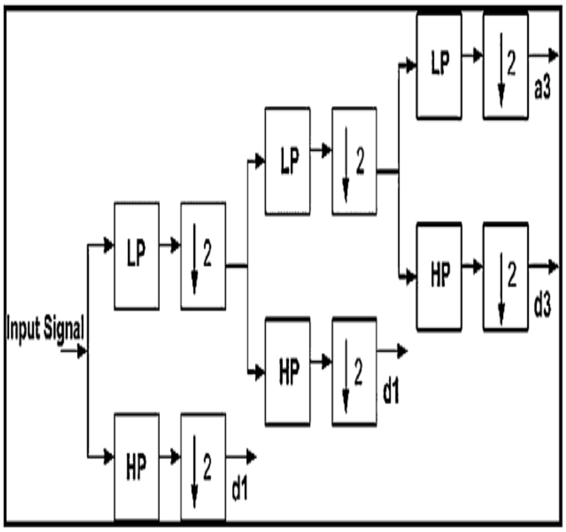


Fig 3. Linear Phase FIR Filter Design

The low-frequency noise is represented by baseline wandering noise. In the wandering baseline, the isoelectric line changes position. Primary possible causes for baseline wandering noise are the cables moving during reading, patient movement, dirty lead wires/electrodes, loose electrodes, in addition to other minor sources. Baseline wandering noise is removed in LLFE design using least square linear-phase FIR high-pass filtering. The high-pass filter type used in LLFE is least-square linear-phase FIR high-pass filter with cut-off frequency of 0.5 Hz to remove the low frequency baseline wandering noise embedded in the input ECG signal. The de noising block is modeled and implemented in Matlab Simulink using Xilinx System Generator blocks. The least-square linear phase FIR filter structure is modeled and implemented using Xilinx System Generator FIR Compiler block.

C. Feature Extraction – Discrete Wavelet Transform

LLFE feature extraction block uses discrete wavelet transform methodology. It has a filter structure as shown in Fig. 2. The input signal is filtered by the low-pass (LP) and the high-pass (HP) filters. The outputs from the low pass filter are called the approximation coefficients while the outputs from the high-pass filter are called the detail coefficients. The output of each filter is then down sampled by a factor of 2. The LP output is further filtered and this process goes on until enough steps of decomposition are reached. In LLFE the input signal is passed through three levels of filtering results in four signals (d1, d2, d3, and a3). The feature extraction is done by wavelet transform decomposition. In this step, the continuous ECG signals are transformed into individual ECG beats. The width of individual beats is approximated to 300 sample data, and the extracted beat is centered around the R peak. For each R-peak, the continuous signal for each beat start at R − 150 position is cutoff until R+ 149 position, therefore, a beat with 300 sample data in width is achieved. In this decomposition, Order 3 is used as a mother wavelet. In this method, the input signal is decomposed into 3 levels as shown in Fig. 2. The input signal with 300 samples will be down sampled by a factor of 2 in each stage, reaching only 38 samples in the 3rd stage (d3, a3). The detail d1 is usually noise signal and has to be eliminated. On the other hand, d2 and d3 represent the high frequency coefficients of the signal. Since a3, represented by 38 samples, represents the approximation of the signal and contains the main features of the signal, thus a3 is considered as the reduced feature vector that is used in the subsequent stage for the classifier.



Fig, 4. Wavelet Transform Filter Structure Block Diagram

The filter bank is implemented using Xilinx System Generator FIR complier blocks to implement both low pass and high pass filters.

D. Classification Block

The classifier which is implemented in LFEE is based on feed forward back-propagation neural network; the neural network output indicates whether the sample provided in the input of the design represents a normal ECG beat or abnormal ECG beat. The output y of each neuron of the neural network according to the input x, neurons weights w, bias b, and activation function g is shown below as in (1):

$$y = g(xiwi + b)$$

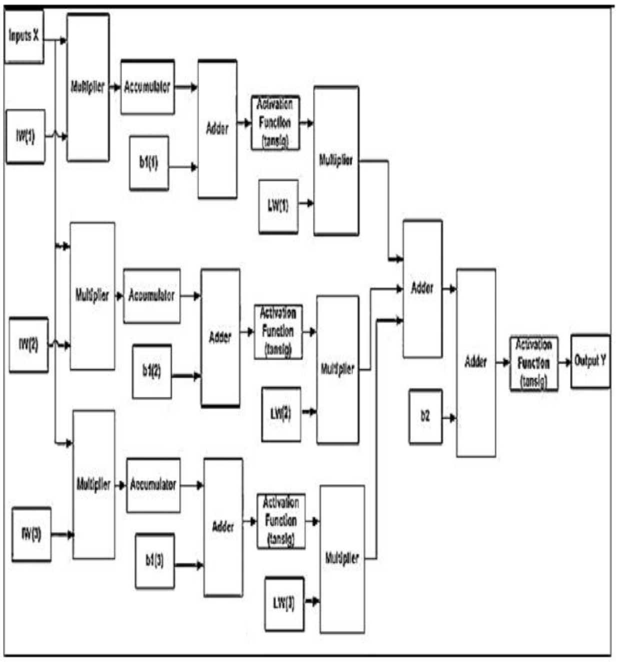
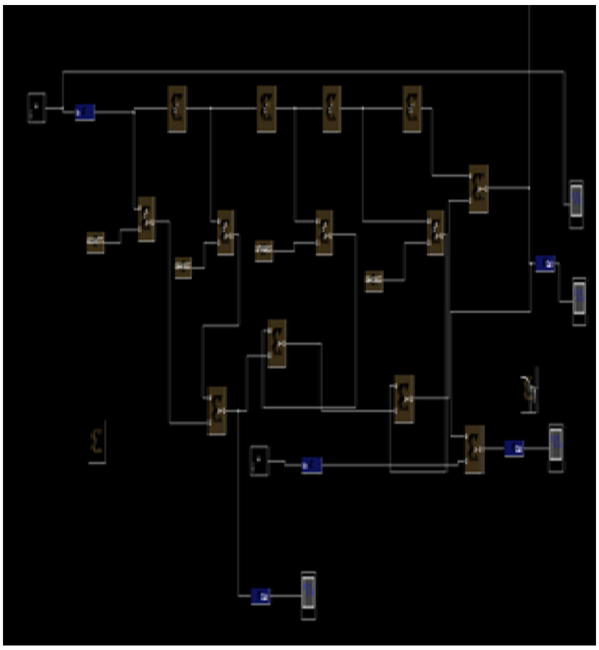


Fig 5. Classification Block of LLFE Design

The basic blocks of the neural network are multiplier blocks, adder blocks and the activation function blocks. The neural network in the proposed LLFE design has one hidden layer with 3 hidden neurons and 1 output layer. A block diagram of the neural network is shown in Fig. 3, the neural network is implemented using Matlab Simulink in terms of Xilinx System Generator blocks. The input to the neural network the approximated signal (a3) (Inputs X) output from the feature extraction block,along with the weight vectors IW and LW, along with the bias values b1 and b2, while the output of the neuralnetwork classifier is the diagnosed ECG signal (Output Y) which represents the diagnosed ECG signal. The proposed neural network classifier is created using newff Matlab function to create a feed-forward back propagation network. The neural network is trained using a supervised learning algorithm by using traingd Matlab function, traingd is anetwork training function that updates weights and bias values according to gradient descent, with a number of epochs of 100,000 used during the training phase.



Fig, 6. Proposed FIR Filter Output

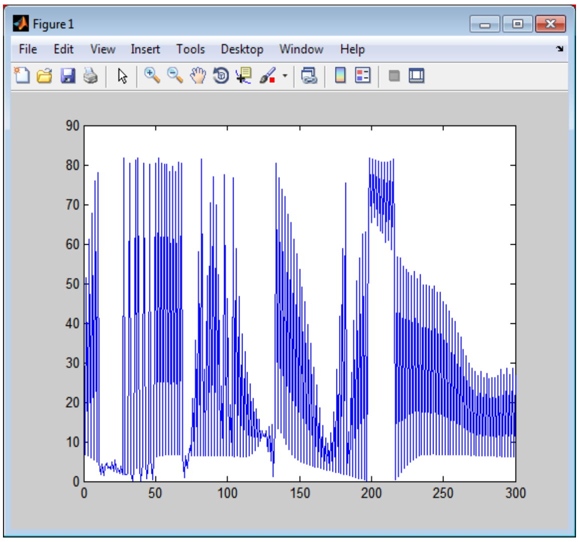


Fig 7. Recorded Original Input Signal

The recordings from the Holter monitor that stores the heart rhythm is been fed have the input signal has shown above figure.

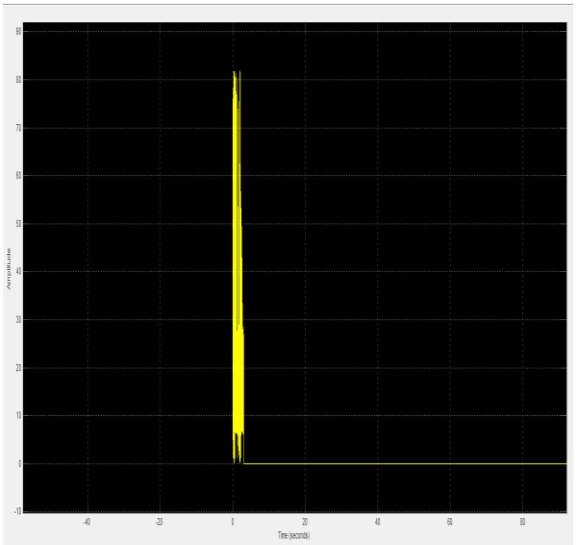


Fig 8.Filtered Input ECG Signal

The noisy part alone is being analyzed from the previously given input.

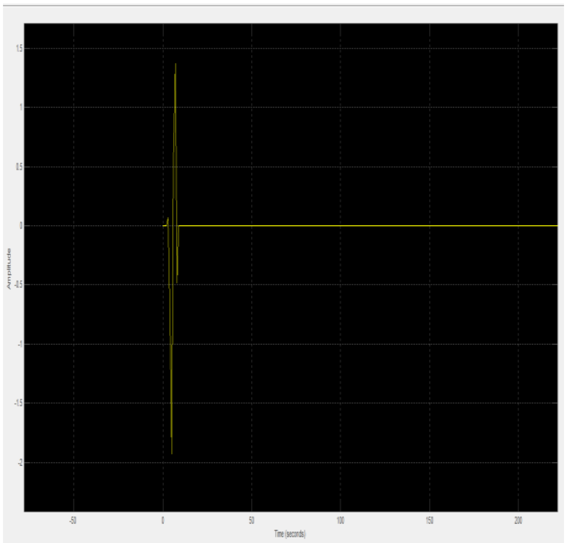


Fig 9. Identification and Removal of Low Frequency Noise

In this stage, low frequency noise is identified and has been removed.

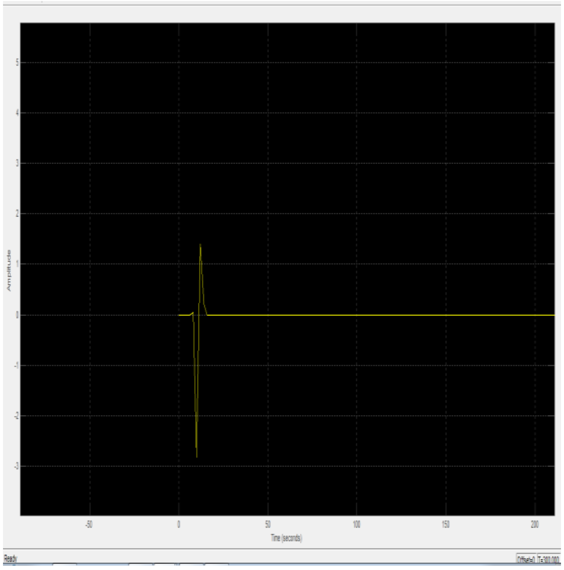


Fig 10. Identification and Removal of High-Frequency Noise

In this stage, high frequency noise has been removed.

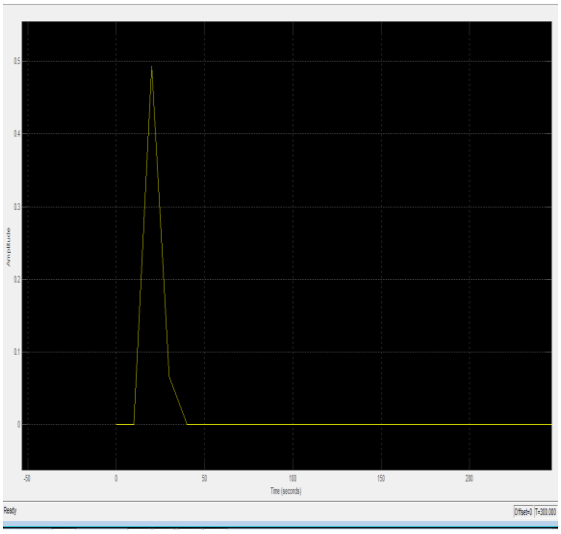


Fig 11. Original and Enhanced ECG Signal

Thus after the removal of baseline wander noise, the original and enhanced ECG signal is being detected.

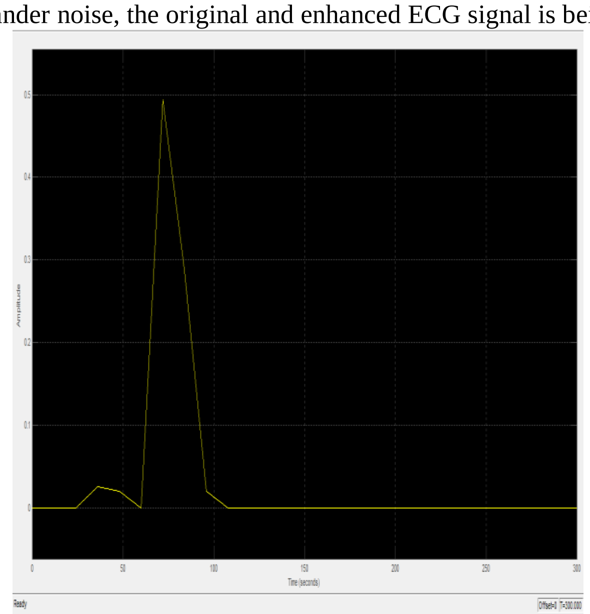


Fig 12.Real-Time ECG Signal DETECTION

Finally, a perfect noiseless ECG signal has been produced at this stage after several filterations of a noisy signal.

4. CONCLUSION

We have thus implemented the entire system in the FPGA kit for real time analysis. This is exactly similar to the simulation of the entire system in MATLAB. This helps in continuous monitoring of the patient in the absence of the doctor. A real time analysis help in enhancing the system for recording and analyzing the large number of patients simultaneously.

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