Design of Low Voltage two stage CMOS Operational Amplifier

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ABSTRACT

The method that presented in this paper is to design a low voltage CMOS operational amplifier, which operates at ±1V power supply. Due to this the demand of low voltage silicon chip systems has been increased. The supply voltage is scaled down to reduce the overall power consumption of the system. The objective of this project is to design a low voltage CMOS operational amplifier. The designed OP-AMP is a two-stage CMOS OP-AMP which exhibits a gain of 59.50 dB, phase margin of 79.431 and unity gain bandwidth is 7.717 KHz. Design and Simulation has been carried out in LT Spice tools.

Keywords: *2 Stage OP-AMP, CMOS, Gain, Phase Margin, Unity Gain Band Width.*

I. INTRODUCTION

The continuous trend of designing high performance analog integrated circuits is becoming most essential due to the reduced supply voltages. MOS is most success among all the analog integrated circuits because it can be scaled down to smaller dimensions for better performance. By scaling down the transistor size, we can integrate more number of transistor into it. Because of this we can increase the amplification rate also. A reduced supply voltage is necessary to decrease power consumption so this would reduce battery size and weight and enable longer battery life time.

The operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design. In two stage op-amp the first stage of an op-amp is a differential amplifier. This is followed by another gain stage, such as a common source stage, and finally by an output buffer. The implementation of a CMOS OPAMPs that combines a considerable dc gain with higher unity gain frequency has been a most difficult problem. There have been several circuits proposed to evaluate this problem. The purpose of the design methodology in this paper is to propose accurate equations for the design of high- gain 2 staged CMOS op-amp. For this, a simple analysis with some meaningful parameters (such as gain bandwidth, phase margin, etc.) is performed. The method handles wide variety of specifications and constraints. In this, we formulate the CMOS op-amp design problem. The method we present can be applied to a wide variety of amplifier structures, but in this paper we apply the method to a specific two stage CMOS op-amp. High gain in operational amplifiers is not the only desired figure of merit for all kind of signal processing applications. In this case, the slew rate will increase for an increase in current.

Thus, we can conclude that the selection of device sizes depends on trade-offs between stability and slew-rate. The addition of the compensating network consisting of a compensation capacitor, *Cc* and a zero-nulling resistor R2.Because the op-amp doesn't have an output buffer, it is limited to driving capacitive loads and very large resistances (comparable to the output resistance of a MOSFET, that is, mega ohms). Operational Amplifiers are the backbone for many analog circuit designs. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the Op-amp.

1.1 Single Stage Operational Amplifier

In this system we uses a simple CMOS differential amplifier as single stage amplifier with input biasing of 250 mV. Correspond to the input 500mV, the output generated is 705mV DC respectively. The gain of the single stage amplifier is very small so that we goes to two stage operational amplifier. . The main function of differential stage is to amplify the difference of the input signals v2 and v3. The transistor M3 and M4 act as the current mirror load for the difference stage. The transistor M6 and M5 are used for biasing the differential stage amplifier. Output of differential stage is given to the gain stage amplifier. Differential amplifier is most widely used in circuit building blocks in analog integrated circuits. It is used on the input of an amplifier to allow input voltages to move around so that biasing of the gain stage is not affected. The input stage of every op amp is a differential amplifier. BJT differential amplifier is the basis of very high speed logic circuit family, called emitter coupled logic.
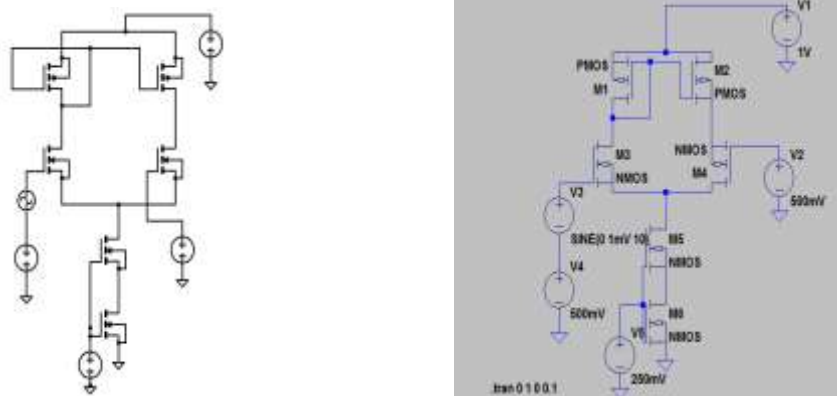

Figure 1. Single stage operational amplifier

DC Gain = vout /vin

= 705mV/1mV

= 56.93 dB

1.2 Common Source Amplifier

The output of the differential amplifier is very small so we uses a common source amplifier as the gain amplifier. The function of this stage is to amplify the output voltage of the differential amplifier. A PMOS and NMOS transistor as common source amplifier. Here a biasing voltage of 250mV is given to the circuit. Common source is the only stage that provides gain. The common source amplifier may be viewed as a transconductance amplifier or as a voltage amplifier. As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to ohm''s law. The cs-cg combination is called a cascode amplifier. The bandwidth of the common source amplifier tends to be low due to high capacitance resulting from the miller effect.
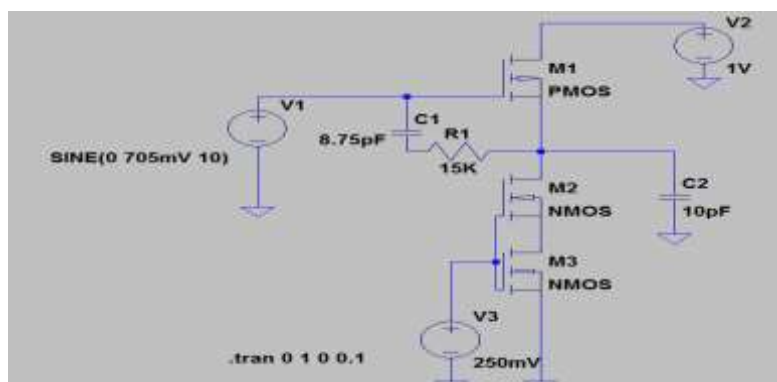

Figure 2. Common Source Amplifier

II. PROPOSED SYSTEM

This paper presents a design of Two Stage CMOS operational amplifier, which operates at ±1V power supply. The OP-AMP designed is a two-stage CMOS OP-AMP. The OP-AMP is designed to exhibit a unity gain frequency of 4.416MHz and exhibits a gain of 96dB with a 700 phase margin. Design and Simulation has been carried out in LT Spice tools**.** The operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design. Design of the op-amp consists of determining the specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the op-amp *A0L* (open-loop gain), CMR (common-mode range on the input), CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio), output voltage range, current sourcing/sinking capability, and power dissipation. The simplified Block Diagram is shown in figure 3. The first block is a differential amplifier. It has two inputs that are the inverting and non-inverting voltage. It gives a differential voltage at the output or a differential current which depends only on differential input voltage. The next block is a differential ended to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended output signal. Some architecture doesn't require the differential to single ended function; therefore this block can be eliminated in that. In circuits where, the gain provided by the input stages is not sufficient, so there is an additional amplification is required which is provided by the second stage, i.e. the common source amplifier, driven by the first stage output. As this stage uses differential input unbalanced output differential amplifier, so it provides the required extra gain. The biasing circuit is here to provide the proper operating point to each transistor in its saturation region. The output buffer stage provides the low impedance at output and larger output current needed to drive the load of op-amp or improves the slew rate. Even the output stage can be dropped since many applications do not need low output impedance. If the op-amp is intended to drive a small purely capacitive load, then output buffer is not required. When the output stage is not used the circuit is an operational transconductance amplifier, OTA. The motive of the compensation circuit is to decrease the gain at high frequencies and to maintain stability when negative feedback is applied to the op amp.

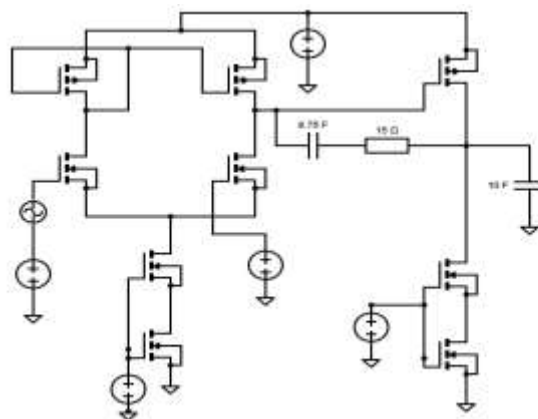### 2.1 Two stage operational amplifier

Figure 3. Two stage operational amplifier

Circuit diagram of two stage operational amplifier is consisted of differential stage, gain stage and output buffer. In this circuit it consists of differential stage and gain stage. When there is no output stage, we use compensation. The main function of differential stage is to amplify the difference of the input signals v2 and v3. The transistor M3 and M4 act as the current mirror load for the difference stage. The transistor M6 and M5 are used for biasing the differential stage amplifier. Output of differential stage is given to the gain stage amplifier. Second stage is the gain stage we uses common source amplifier as gain stage. The function of this stage is to amplify the output voltage of the differential amplifier. A PMOS and NMOS transistor as common source amplifier. This circuit has compensation, which is required for two stage operation amplifier especially when the load is purely capacitive or else the circuit becomes unstable at larger frequencies. For compensation the operational amplifier we use a coupling capacitor and zero nulling resistor between the output of the first stage and the input of second stage of the operational amplifier. The addition of the compensating network consisting of a compensation capacitor, *Cc* and a zero-nulling resistor R2.Because the op-amp doesn't have an output buffer, it is limited to driving capacitive loads and very large resistances

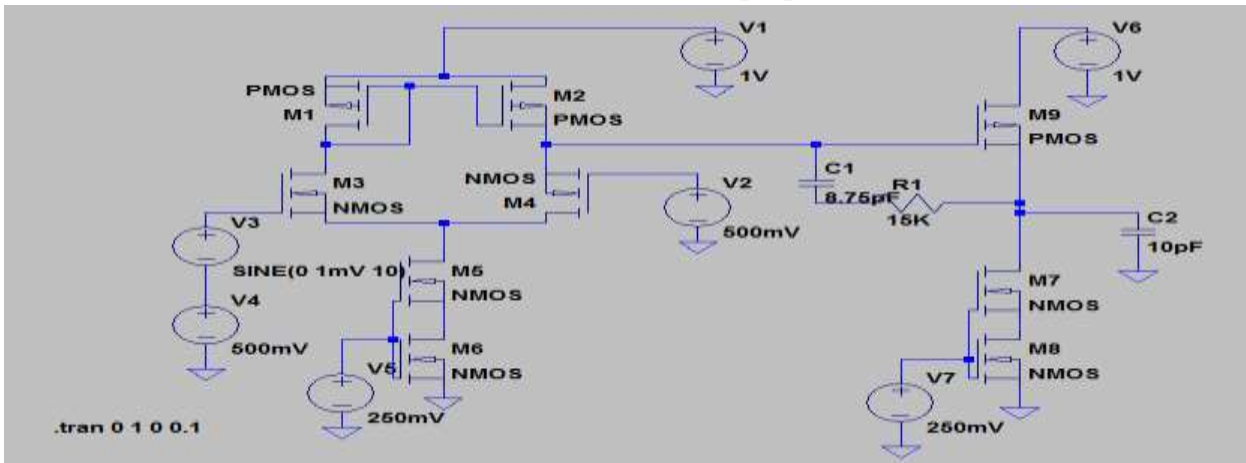## III . Results and discussions of proposed system

Figure 4. CMOS two stage operational amplier in Lt spiceIV

3.1 Transient Analysis

Here Cc =8.75pF and CL =10 pF.

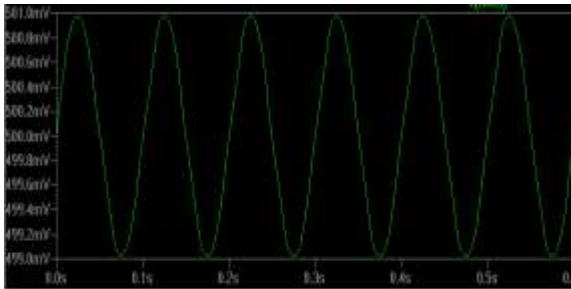The input applied to differential Amplifier is a 1mV and we are getting an output of 1V.

Figure 5. Input of two stage op amplifier
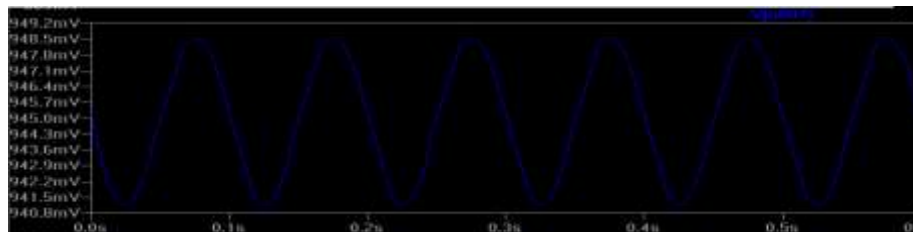

Figure 6. Output of differential amplifier

Figure 7. Output of two stage op amp

3.2 AC Analysis

In AC analysis we examine the Gain

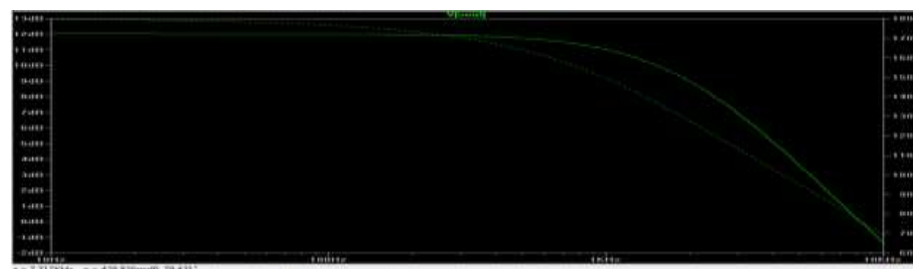☐ Start frequency = 10Hz   ☐ Stop frequency = 10 KHz

Figure 8. AC analysis of two stage op amp

- Gain = 59.50 Db
- Phase margin = 79.481
- Unity gain band width = 7.717KHz

3.3 Slew rate

Slew rate = $\dfrac{0.955-0.556V}{2.035-1.999}$
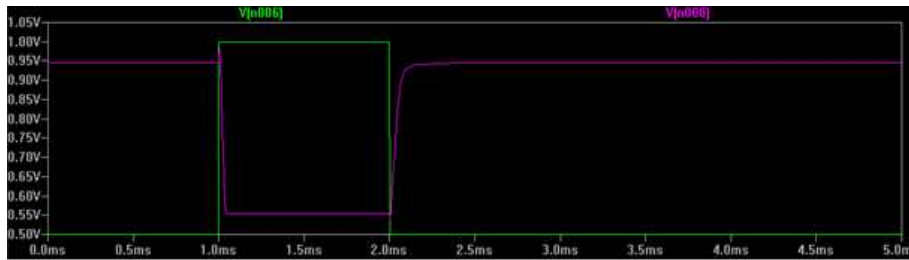
  = 8.81 V/ms

Figure 9. Response of op amp to step input

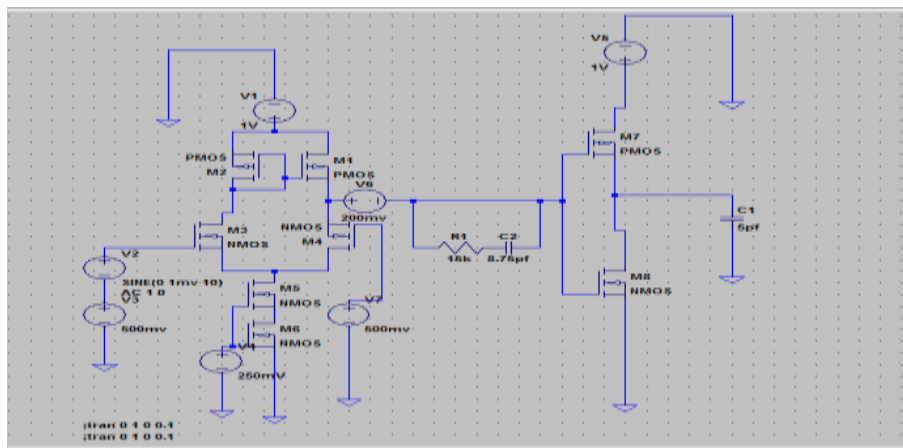# IV. Result and discussion of modified system

4.1 Circuit diagram

Figure 10. Circuit diagram

Modifications done

➢ Connecting nmos m8 as active load

➢ Adding constant dc source of 200mv between first and second stage amplifier

➢ Decreasing the capacitive load from 10pf to 5 pf.

All the above modifications increases the gain of the second stage amplifier.

4.2 Transient Analysis

Here Cc =8.75pF and CL =5 pF.
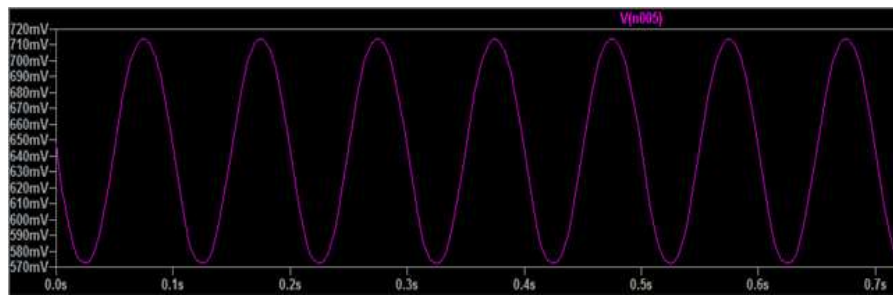The input applied to differential Amplifier is a 1mV and we are getting an output of 1V.

Figure11. Output of two stage op amp

4.3 AC Analysis

In AC analysis we examine the Gain ☐ Start frequency = 10Hz ☐ Stop frequency = 10 KHz
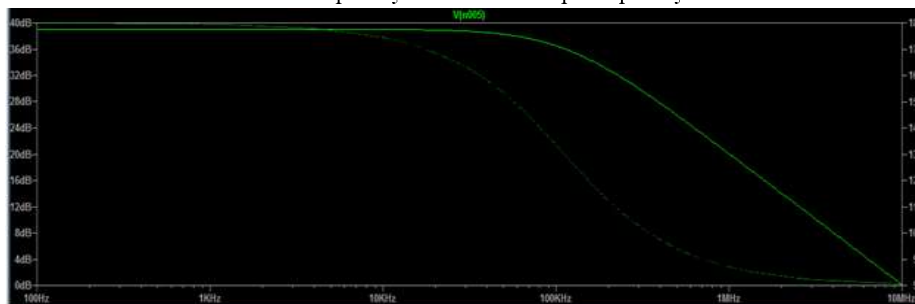

Figure 12. AC analysis of two stage op amp

    1) Unity gain bandwidth=9.818 MHz
    2) Gain=39.015 db,
    3) Gain margin=177.785 degree

4.4 Slew rate

Vin   = 1V
Vout   = 0.650-0.480 = 0.170V
t2 - t1   = 1.26-1   = 0.26us
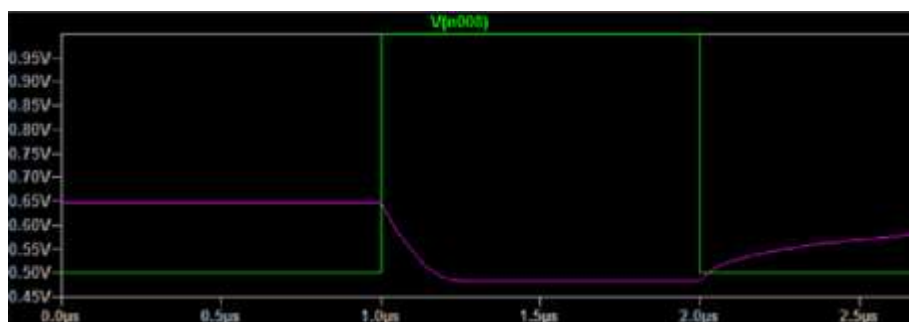Slew rate = 0.170v/0.26 = 0.65v/us.

Figure 13. Response of op amp to step input

V. CONCLUSION

This paper presented the full design and analysis of a two stage CMOS Op-Amp. The results shows that the amplifier designed has successfully satisfied all the design specification given in advance. The designing of high performance analog integrated circuits is becoming most essential with the continuous trend towards the reduced supply voltages and transistor channel length. . The purpose of the design methodology in this paper is to propose accurate equations for the design of high- gain 2 staged CMOS op-amp.

This paper presented a design of Two Stage CMOS operational amplifier, which operates at ±1V power supply. The OP-AMP designed is a two-stage CMOS OP-AMP. The OP-AMP is designed to exhibits a gain of 59.50 dB. Design and Simulation has been carried out in LT Spice tools.

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