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Layout Design of 5 Transistor D Flip Flop for Power and Area Reduction and Performance Comparison in Different Scaling Technologies

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Abstract

Due to increasing in demand for portable devices low power dissipation is an essential need for device design. Due to advances in low power applications, low power digital CMOS has become more important, and the process technology has been advanced. In this paper, a SET D flip flop with 5 transistors is proposed. This D flip flop has been implemented using different scaling technologies such as 180 nm, 90 nm, 70 nm and 50 nm. Both power dissipation as well as area has been compared. The layout of the 5 transistor D FF is designed. It has been observed from simulation result that the fully custom design has shown 39% reduction in area and 37% reduction in power as compared to fully automatic design. This design technique achieves lowest power consumption with reduced transistor count. It can be used in applications like buffers, registers, digital clocks etc.

Keywords: *D Flip Flop, CMOS, Low Power VLSI, Power Consumption, Scaling Technologies*

I. INTRODUCTION

The major concerns of the VLSI industry were area, performance, cost, and reliability; power consideration was mostly of only secondary importance. Now days, power has equal importance as area and speed considerations. The primary driving factor for this trend has been the growth of the class of personal computing devices and wireless communications systems which demand swift computation and highly complex functional modules with low power consumption. Average power consumption is a critical design concern in these applications. Power consumption is a very important consideration in IC design. Flip flops are the basic building block of all electronic devices. Hence proper designing of flip flops are required to achieve the designated functionality with low power consumption. The most common type of flip flop is the D flip flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output [1]. There are two types of FF single edge triggered (SET) and double edge triggered (DET). Single edge triggered samples data either on rising or on falling edge of the clock, on the other hand, double edge triggered samples data on both clock edges. DET is energy efficient compared to SET but has a more complex design. Many transistors had to be employed in the implementation of conventional FF and those FF required a large area. In this paper, a semicustom design which is realized using few transistors has been suggested and also occupy less area and has less power consumption than auto generated layout of design

II. LITERATURE REVIEW

Kawaguchi & Sakurai (1998) presented a reduced clock-swing flip flop (RCSFF), which is made up of a condensed swing clock driver and a special flip-flop which consists of the leak current cut-off mechanism. The RCSFF system reduces the clock system power of a VLSI behind to one-third compared to the conventional flip-flop. As the Leakage current is eliminated through back gate bias, the reduced clock swings down to 1 V there by helping to attain the progress in power factor. The interconnect which consumes RC delay and power can be reduced to less than one-half compared to the

conventional flip-flops. Fabaian Klass et al (1999) introduced a new family of edge triggered flip-flops, with an objective to decrease the pipeline overhead. The flip-flops fit in to a class of semi dynamic and dynamic circuits that can interface both static and dynamic circuits. Since each flip-flop can be viewed as a unique logic gate that serves as a synchronization element, this characteristic significantly reduces the pipeline overhead of the processor by allowing the elimination of one or more gate delays from a path leading to the flip-flop. The flip-flop family explained has played a vital role in meeting the cycle-time goal of the microprocessor. Koichi Nose et al (2000) described the closed-form expression for a short-circuiting power dissipation of CMOS gates which takes short-channel possessions into consideration. The outcome showing the change in the short circuit power, caused by the scaling in relation to the charging and discharging power, is discussed and concluded that essentially power ratio will not change with scaling. Mark C Johnson et al (2002) discussed the use of transistor stacking in single threshold CMOS. In this technique, the state dependence of leakage can be broken to attain modest leakage savings in Complementary Metal Oxide Semiconductor (CMOS) circuits. Nevertheless, one can transform circuits allowing for state dependence and accomplish enhanced savings. The author identifies a low-leakage state and inserts leakage-control transistors only where desirable.

This is proficient with no shortest impact on presentation since the method is only practical to gates which are off the critical path. There is also a negligible direct impact on switching power since no capacitances are additional to logic-signal paths in the circuit. Massimo Alioto et al (2010) explained the clock slope on the rate of diverse classes of flip-flops (FFs) and on the overall energy dissipation of both FFs and clock field buffers is analysed which shows that an optimum clock slope exists that minimizes the energy exhausted in a clock domain. The proposed technique shows that the clock slope condition can be undisturbed with deference to conventional assumptions. The impact of such an optimization in terms of additive skew and jitter contributions is discussed, together with the analysis of the impact of technology scaling. Extensive post layout simulations on a 65-nm CMOS technology are performed to check the validity of the underlying assumptions and approximations. A revision of the outcome of technology scaling has exposed that optimization of the clock slope will be more significant in the future and that the most favourable clock slope will shift towards smoother values. Peiyi Zhao et al (2011) surveyed a mixture of design techniques for a low power clocking system and the Power consumption is the foremost blockage of system performance. Among them, the effective way to cut down the capacity of the clock load is to minimize the number of clocked transistors. To effect this, a novel clocked pair shared flip-flop is presented which minimizes the number of local clocked transistors and the cutback of the clock driving power is obtained. In observation of power consumption of clock driver, the new CPSFF outperforms prior arts in flip-flop design.

Hwang et al (2012) produced a novel low-power pulse-triggered flip-flop (FF) design. In order to speed up the discharge along the critical path. As an outcome, pulse-generation circuit and transistor sizes in delay inverter can be reduced for power saving. In comparison, the presented design features the best power-delay-product presentation in seven FF design than the conventional model. Baccarin et al (2012) presented a novel technique to lessen the leakage current of FinFET forced stacks under a given delay constraint. This takes advantage of the four-terminal FinFETs with a unique feature allowing separate tunable back bias voltages for different transistors. In both cases, the resulting leakage reduction has been shown to be in the order of magnitude or more at no cost in terms of dynamic energy and delay. It was shown that tolerating a small and pre-defined delay penalty enables a larger leakage reduction. Shmuel Wimer (2014) presented a Design Flow for Flip-Flop Grouping in Data-Driven Clock Gating.Clock gating is a main technique 26 used for power saving. The author intended a useful explanation based on the toggling movement correlation of FFs and their physical location closeness constraint in the layout. Data-driven gating aims to put these data driven out of exploit into an Electronic Design Automation (EDA) commercial backend design flow achieving total power reduction for various types of large-scale state-of-the-art industrial and academic designs.

Peiyi Zhao et al (2007) presented a dual edge triggered flip-flop by using clock branch sharing scheme. In this flip-flop design, two latching stages share the clock allocation network to capture and deliver the input data. Clock branch-sharing scheme decreases the number of clocked transistors in the model. The projected design also employs conditional discharge and split path techniques which further help to reduce the short-circuit currents during the switching activity. Manan Joshi et al (2014) introduced a high speed explicit pulsed dual edge triggered D flip flop by introducing efficient explicit clock pulse generator. The dual edge clocking is achieved by explicit clock pulse generation network. This design avoids the stacking of MOS transistors, reduces internal node switching activity. This flip flop uses the minimum number of clocked transistors and overcomes the drawbacks of a dynamic logic family with improved delay and power delay product parameters [2].

III. D FLIP FLOP

The latch is an electronic device that stores one bit of information The D latch latches the logic level present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch.

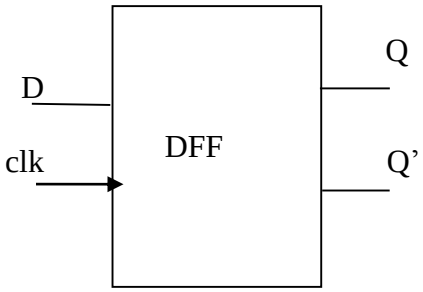

Fig. 1 Symbol of D Flip Flop

The Fig .1 shows the symbol and Fig .2 shows the logic diagram of D flip flop [2]. D flip flop works similar to the D latch except. that the output of D Flip Flop takes the state of the D input either at the moment of a positive edge at the clock pin or negative edge if the clock input is active low and delays it by one clock cycle. That's why it is called as delay flip flop. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. D flip flop is the preferred type of flip flop in integrated circuit applications. S R flip flop has an indeterminate state when both inputs are high. The JKFF simplifies the RSFF truth table but has two inputs.

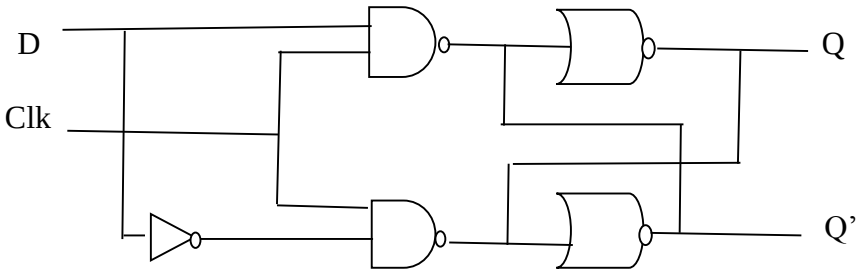

Fig. 2 Logic diagram of D Flip Flop

The Fig.3 shows the timing diagram of a positive edge triggered D Flip Flop. From the figure it can be seen that the output Q changes only at the positive edge of C. At each positive edge, the output Q becomes equal to the input D at that instant and this value of Q is held until the next positive edge. The D Flip Flop can be implemented in different transistor logic such as Static, Dynamic, Pseudo NMOS, True single phased clock, double edge triggered clock and so on [3]. In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.[4] This reduces the number of active devices but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input [5]. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value.

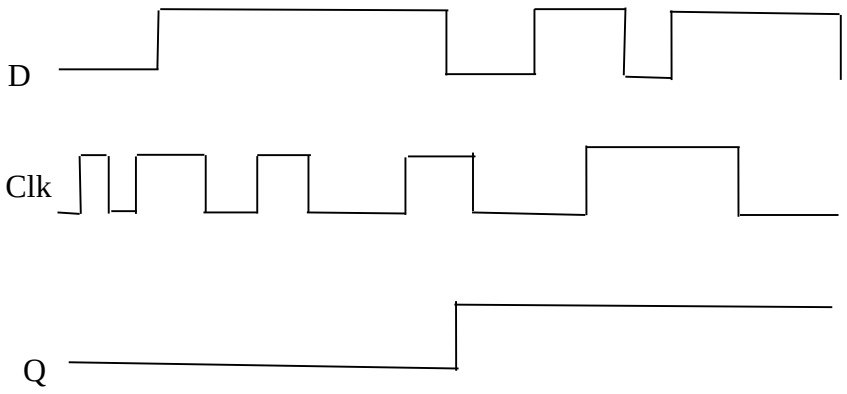

Fig. 3 Timing Diagram of Positive Edge Triggered D Flip Flop

IV. PROPOSED DESIGN

The D-latch has many applications in digital circuit design, primarily for temporary storage of data or as a delay element. The circuit shown in Figure 4 shows a basic two-inverter loop and two CMOS transmission gate (TG) switches. In principle, a transmission gate made up of two field-effect transistors, in which – in contrast to traditional discrete field-effect transistors – the substrate terminal (bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET, and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a NOT gate (inverter), to form the control terminal. Unlike with discrete FETs, the substrate terminal is not connected to the source connection. Instead, the substrate terminals are connected to the respective supply potential in order to ensure that the parasitic substrate diode (between gate and substrate) is always reversely biased and so does not affect signal flow. The substrate terminal of the p-channel MOSFET is thus connected to the positive supply potential and the substrate terminal of the n-channel MOSFET connected to the negative supply potential [6]. The TG at the input is activated by the clock signal, whereas the TG in the inverter loop is activated by the inverse of the clock signal. Thus, the input signal is accepted (latched) into the circuit when the clock is high, and this information is preserved as the state of the inverter loop when the clock is low [7]

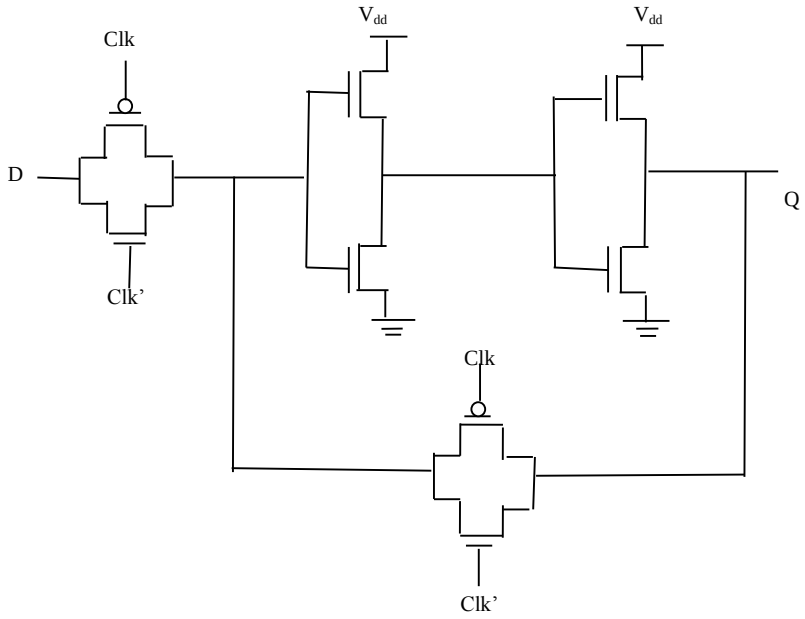

Fig. 4 D Flip flop using Transmission Gate

The circuit shown in figure 5, shows CMOS implementation of D FF using 10 transistors. The circuit consists of two tri state inverters. In the tri state inverter at the input, the NMOS transistor is driven by a clock signal (clk) and the PMOS transistor is driven by an inverse of the clock signal (clk'). When clock becomes high, the first tri state inverter behaves as the input switch with the input signal.

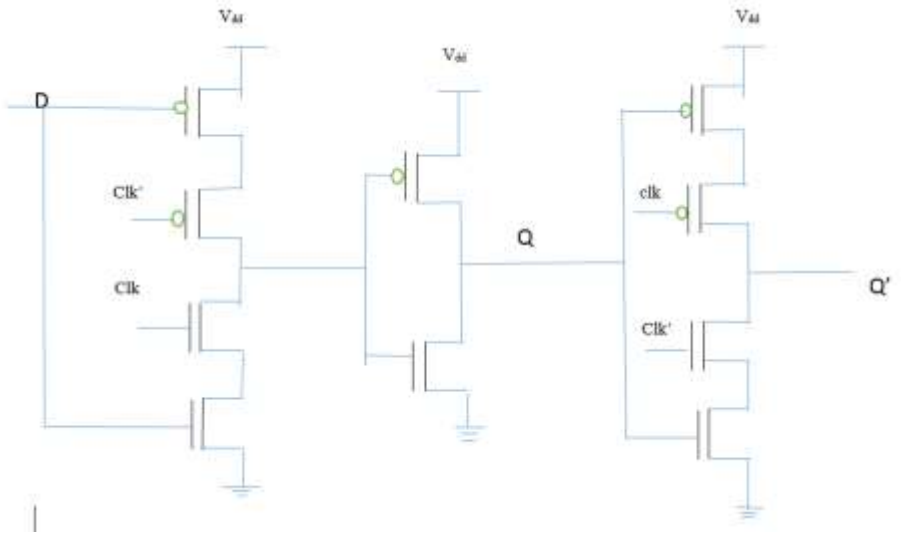

Fig. 5 D Flip flop using tri state

On the other hand, second tri state inverter shows high input impedance state and output follows the input signal. When the clock signal becomes low, second tri sate inverter completes the two inverter loop which holds its state until the next clock signal [7].Positive edge triggered 5 transistor D latch is shown in figure 6 [8]. When both clock and input (in) becomes high then the transistors M1, M5 gets into the off condition and remaining transistors M2, M3, M4 gets into the on condition. The output becomes high. During on clock period whatever is the value of the input, it becomes output.

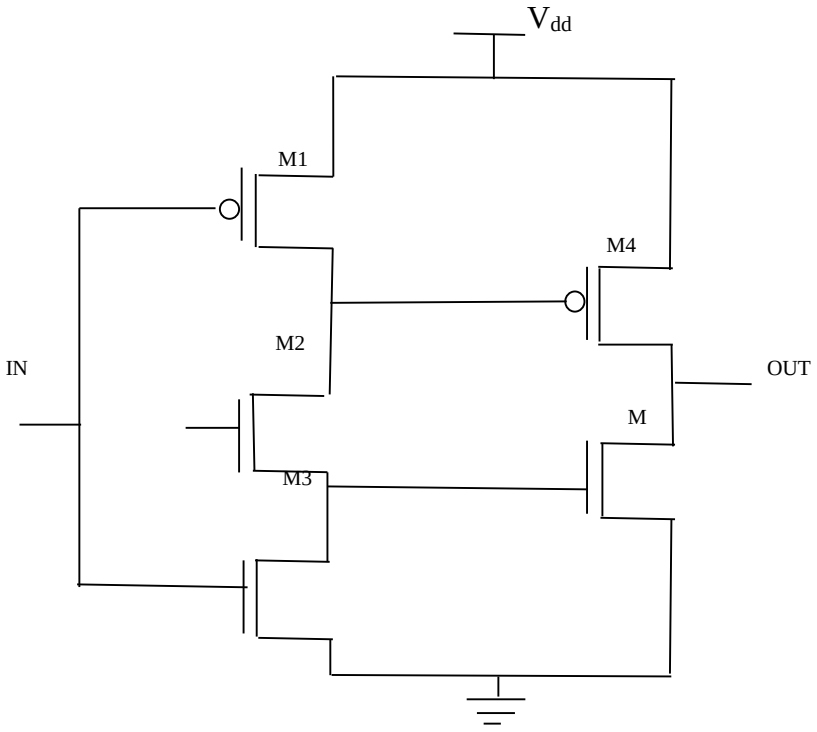

Fig. 6 D Flip flop using 5 transistors

V. SIMULATION AND RESULTS

The designs are implemented using DSCH and layouts are obtained using Microwind3.1.The circuits are simulated using 180 nm, 90nm, 70nm and 50nm technologies. The circuit diagram of the proposed SET D FF is shown in figure 7. Figure 8 shows the layout of D FF shown in figure 6. The design used 5 transistors. The circuit has one clock signal. When both Clock and input becomes high, out 1 becomes high or the LED turns on. The design is implemented using DSCH software to calculate area and power consumption. Figure 9 shows the timing diagram of the proposed flip flop. In this design layout of all NMOS and PMOS are called from the library. The functionality of the proposed layout has been verified and recorded in table I and a comprehensive study of the area and power dissipation has been done in different scaling technologies.

From the table I it is obvious that the power consumption decreases from auto generated layout design to proposed fully custom layout design.

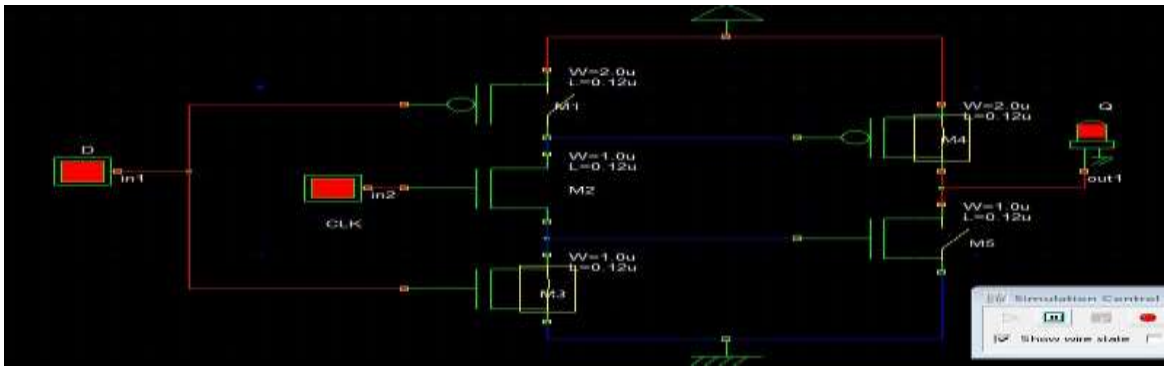

Fig. 7 Circuit Diagram of the Proposed SET D FF

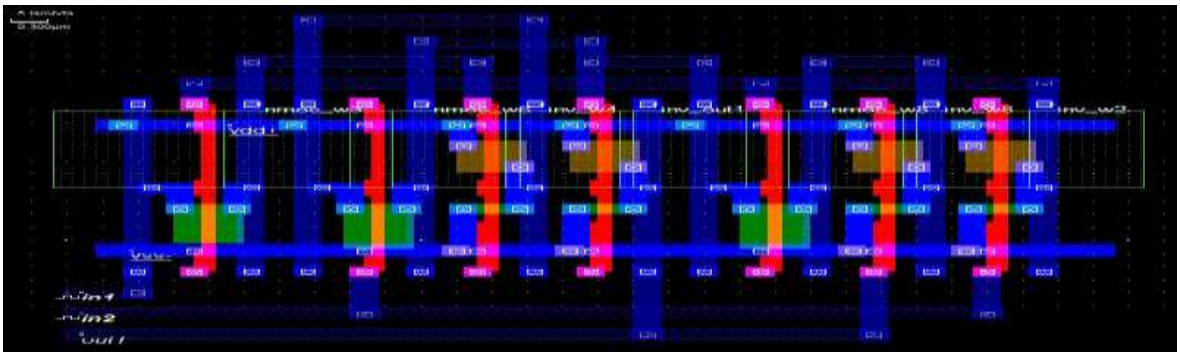

Fig. 8 Layout of D FF

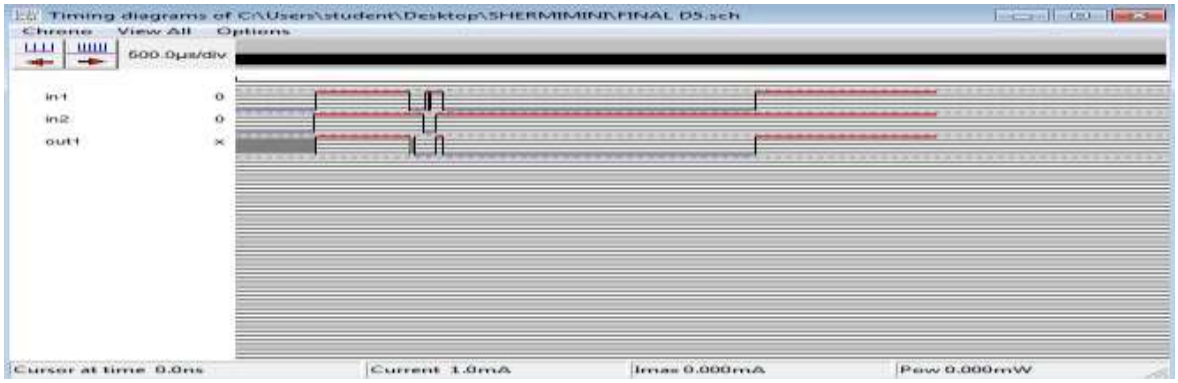

Fig. 9 Timing Diagram of the Proposed flip flop

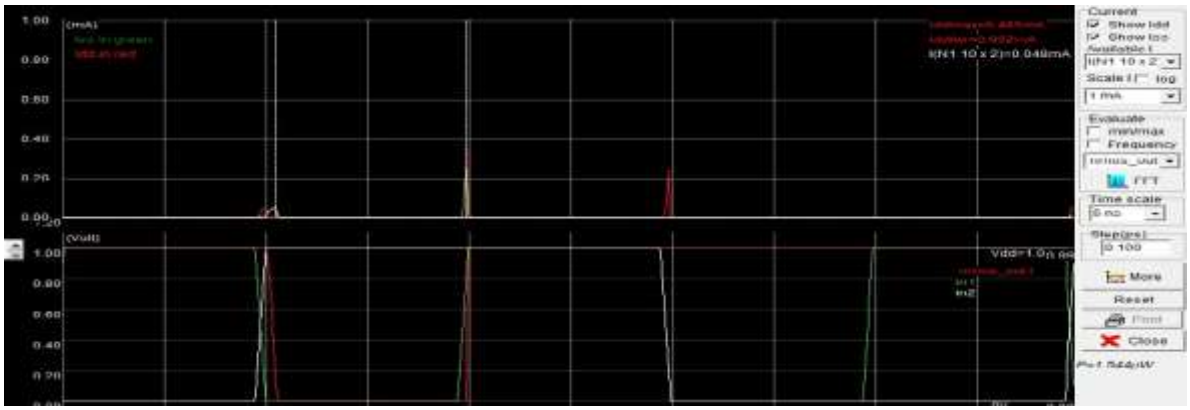

Fig. 10 voltage vs current graph in 180 nm

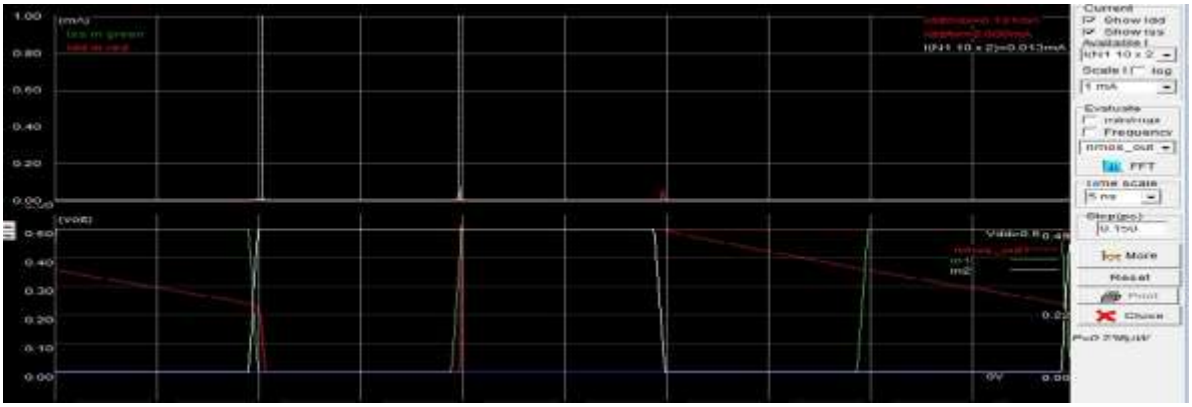

Fig. 11 voltage vs current graph in 90 nm

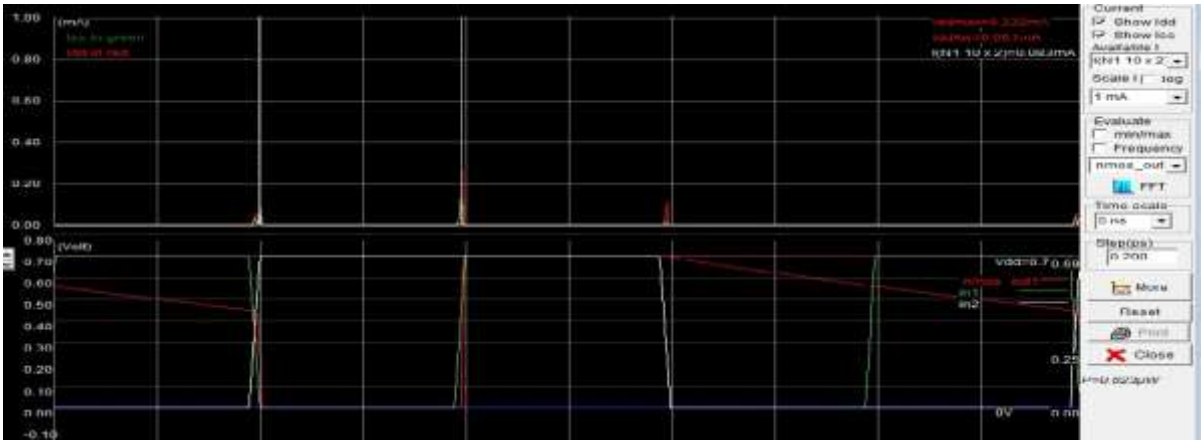

Fig. 12 voltage vs current graph in 70 nm

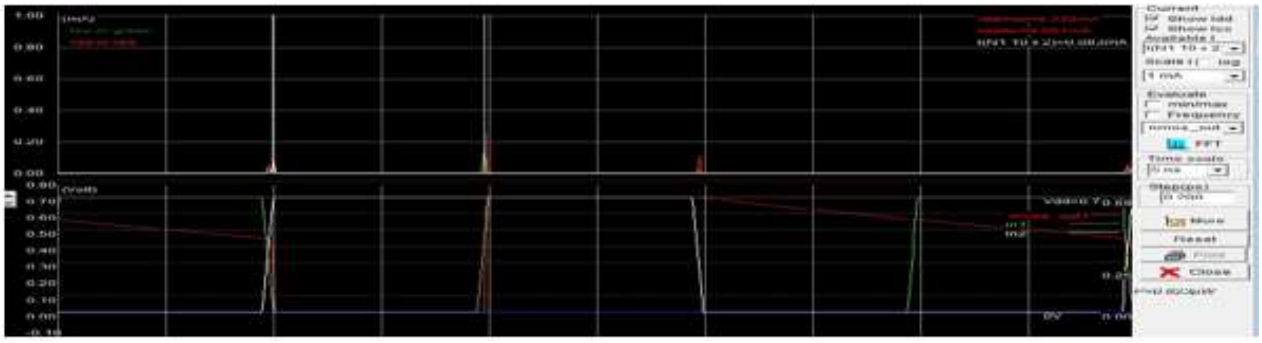

Fig. 13 voltage vs Current Graph in 50 nm

TABLE I
Power and Area comparison of the proposed design in different scaling technologies

Parameters	**180 nm**	**90 nm**	**70 nm**	**50 nm**
Area (μm^2)	197.1	94.1	42.1	25.5
Power (μW)	.411	9.32	5.28	2.53

VI. CONCLUSION

In low power applications, area and power consumption by the device are the main technological aspects to prefer a design over the other designs. In this paper, the D flip flop is implemented using 5 transistors. The proposed design of SET D flip flop shows better performance in terms of power dissipation and area among previous designs. The relative percentage power reduction in the proposed design is from 37 % to 52 % with respect to the previous designs. The design also has a reduction in area from 39 % to 73.6 %.

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