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Automatic Power Factor Correction by Fine Tuning of Graded Capacitors

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Abstract: ***Today's power system demands improved power factor in order to harness various advantages associated with improved power factor. Till date, various methods have been deployed to improve the power factor of the power system. This paper mainly focuses on a novel methodology for reactive power compensation and thereby power factor improvement at the load end. This paper presents a novel approach of capacitance grading for achieving fine tuning of power factor. The concept for automatic power factor correction by fine tuning of graded capacitors with the help of microcontroller and binary logic is proposed, simulated, and implemented. The method presented is of iterative nature and is cost competitive over other deployed methods. An algorithm is developed and a model is made to deploy the concept of iteration with binary logic. The same is tested on an induction motor and results obtained are analyzed.***

Keywords: APFC- Automatic Power Factor Correction, ZCD- Zero Crossing Detector, CT- Current Transformer, PT-Potential Transformer, OpAmp- Operational Amplifier

I. INTRODUCTION

In the present scenario of technological revolution, it is observed that power is very precious. The industrialization is primarily increasing the inductive loading and the inductive loads affect the power factor so the power system loses its efficiency. There are certain organizations developing products and carrying R&D work in this field to improve or compensate the power factor. In the present trend, the designs are also moving towards the miniature architecture; this can be achieved in a product by using programmable devices. Whenever we are thinking about any programmable devices then the embedded technology comes into the forefront. The embedded technology is now a day's very much popular and most of the products are developed with Microcontroller based embedded technology. The power factor correction can be achieved by using the same microcontrollers and embedded systems.

Automatic power factor correction device reads power factor from line voltage and lines current by determining the delay in the arrival of the current signal with respect to the voltage signal from the function generator with high accuracy by using an internal timer. This time values are then calibrated as phase angle and corresponding power factor is determined. Then the motherboard calculates the compensation requirement and accordingly switches on different capacitor banks. This is developed by using 8051 microcontrollers.

II. FUNCTIONAL BLOCK DIAGRAM, SCHEMATIC DIAGRAM, AND METHODOLOGY

A. Functional Block Diagram

The method of automatic power factor correction by using graded capacitors is represented in the form of simplified block diagram as shown in figure 1. A current transformer and voltage transformer senses the current and voltage of the system. The ZCDs are used to convert the sinusoidal output of CT and PT into corresponding square waves. These square waves are then fed to the micro controller which measures the time difference between voltage and current square waves. The micro controller is programmed in such a manner so as to compare the time difference between voltage and current signals. The micro controller generates an output signal to switch the graded capacitors corresponding to the time difference between voltage and current waves.

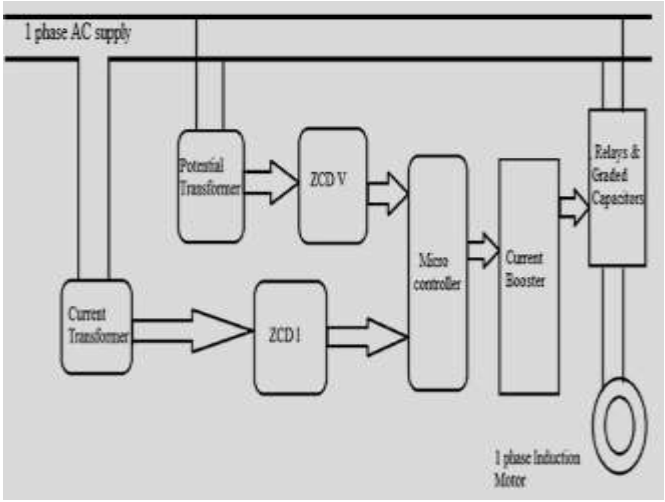

Fig.1 Functional Block Diagram

B. Schematic Diagram

As shown in Fig.2, the APFC consists of various blocks like the power supply circuitry, ZCD, Microcontroller, Graded Capacitor bank, Current booster. The power supply circuit consists of a transformer which steps down the voltage and serves as an input to the rectifier and regulator which gives 5 Volts constant output. This output power is given to the microcontroller as a power source Vcc. The transformer is also used as a PT to provide the voltage input to the ZCD. The current input to ZCD is taken from the CT connected to the motor supply lines. The ZCD first converts the sine waves of current and voltage into square waves, then finds out the time difference the two square waves crossing the x axis. Op-Amp IC-741 is configured to work as zero crossing detectors. Two ZCDs are employed; one is for converting the sinusoidal voltage signal into the corresponding square wave and other for converting the sinusoidal current signal into a corresponding square wave. The difference between the time instances of the two waves is the angle 'ø'. This difference ø is then fed as an input to the microcontroller 8051. The microcontroller is programmed in such a manner that it generates output signals in proportion to the time shifts between voltage and current wave. [1]

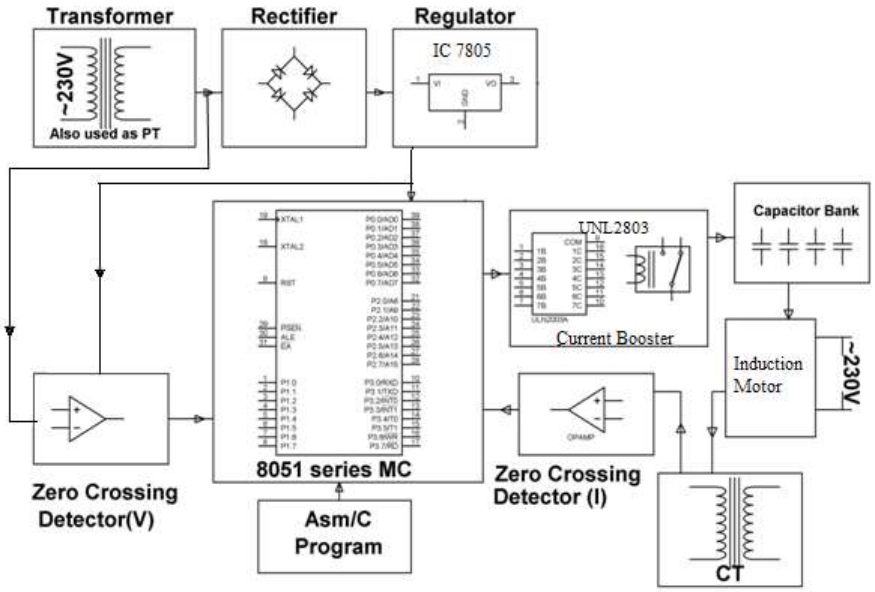

Fig.2 Schematic Diagram of APFC

The output current sourcing capacity of 8051 micro controller output pin is 10 mA per pin or 26 mA per port. The current required for pick-up relay JQC-3F (T73) is 90 mA at 5V. Hence, in order to drive relay through microcontroller UNL2803 is used as a current booster. Output port 2 of micro controller is connected to input pins (I0-I7) of UNL2803 and output pins (O0-O7) of UNL2803 are used to drive relays. The output generated by UNL2803 is used to drive the relays which are connected to the graded capacitors. The capacitors are switched in correspondence with the binary logic. [2]

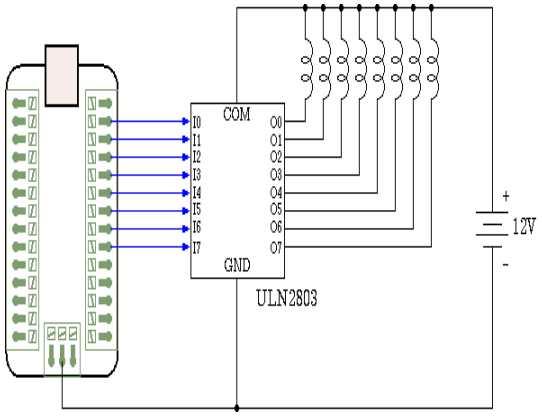

Fig. 3 Connection of ULN2803 with µC and relays

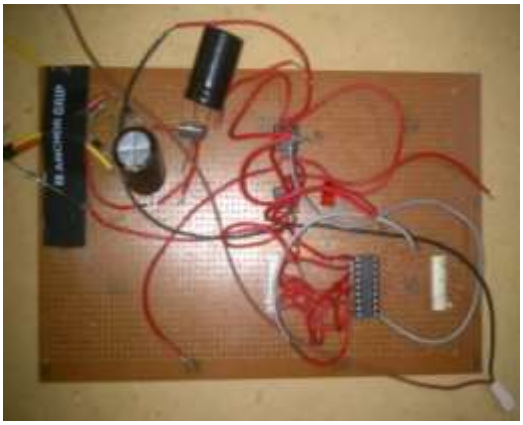

Fig. 4 Practical Circuit of ULN2803

In order to maintain the power factor precisely at the set value, the exact amount of reactive power consumed by the load must be supplied by the capacitors. This is important in order to avoid over or under compensation. In this approach values of each 8 capacitors connected in parallel with the load are kept proportional to the weight of bits in 8 bit binary number. According to this logic, each capacitor can take the following values.

Table. I Binary Logic Grading of Capacitors

Capacitor	1st	2nd	3rd	4th	5th	6th	7th	8th
Values (in µF)	1	2	4	8	16	32	64	128

By connecting above capacitors in different combination, the effective capacitance of 0 to 255µF with a minimum variation of 1µF can be achieved.

Fig. 5 Graded Capacitors

III.IMPLEMENTATION

APFC is implemented on 200V, 0.75 hp single phase induction motor. Maximum reactive power required by the motor is 506 VAR. Hence the value of capacitors in capacitor bank should be selected in such a way that it can supply maximum 506 VAR. Combination of capacitors shown in table-1 would supply maximum 3204 VAR which is way more than the actual requirement. In order to avoid over the designing value of each capacitance in the table-1 is reduced by 50%. This reduction not only helps to avoid over designing but with this fine tuning of 0.5 µF is possible. By applying this, the new values of capacitors will be as follows. By connecting below capacitors in different combination, the effective capacitance of 0 to 98.5µF with a minimum variation of 0.5µF can be achieved.

Table II Capacitor Values Reduced by 50%

Capacitor	1st	2nd	3rd	4th	5th	6th	7th	8th
Values (in µF)	0.5	1	2	4	8	16	32	64

The setup is shown in fig.6 (a) and 6(b) which consists of the algorithm of the Binary Graded capacitor switching and its testing after burning the code into the microcontroller. The algorithm is such that it first senses the value of the power factor by using ZCD and determines whether the value of power factor is lagging or unity and then takes the corresponding decision to switch on the capacitors in order to fulfil the exact reactive power requirement of the circuit. The algorithm is converted to machine language code and is fed to the microcontroller. The coded microcontroller is tested by using LED combinations as shown in figure 6 (b).

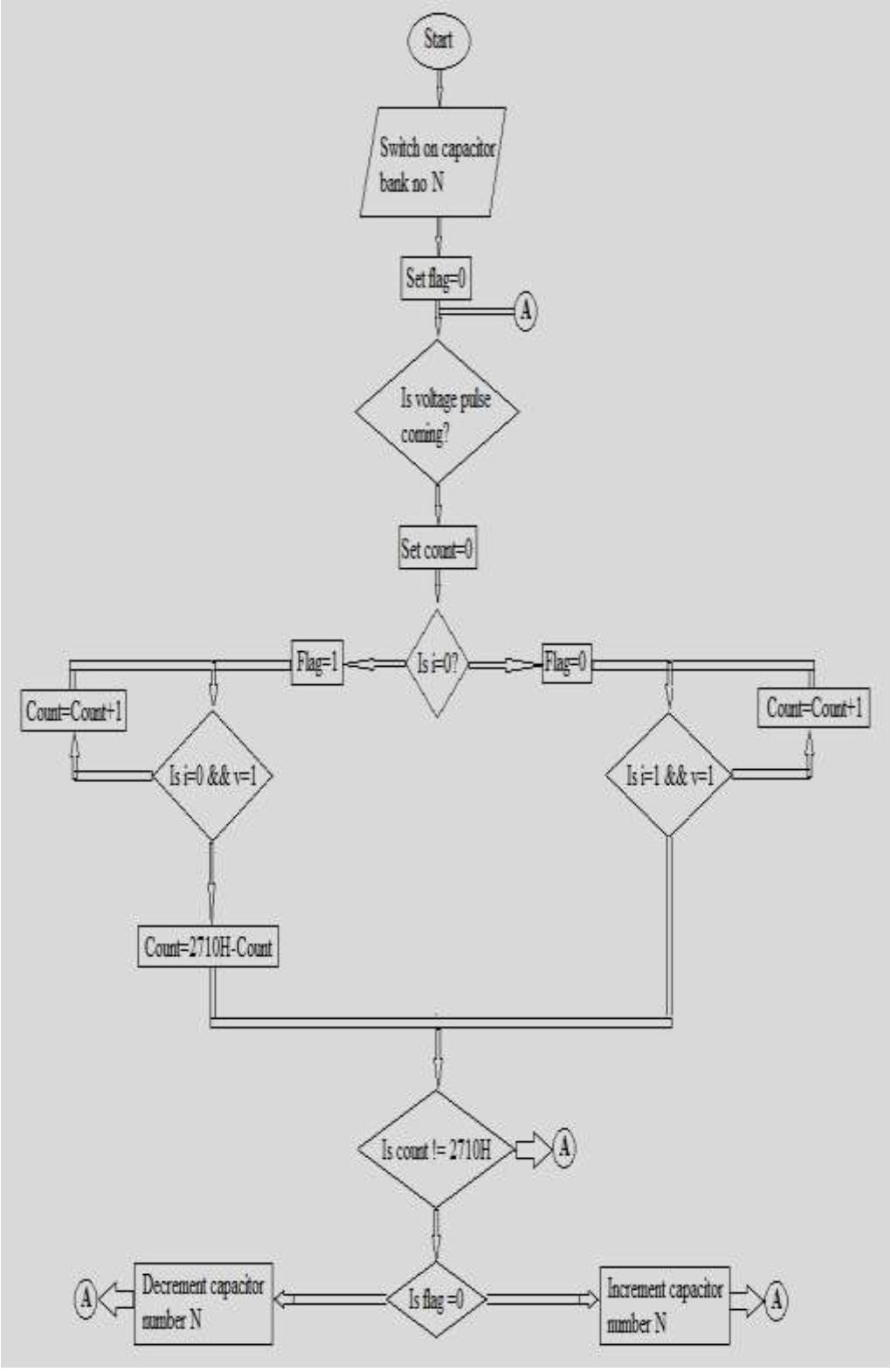

Fig. 6(a) Algorithm of Microcontroller Coding

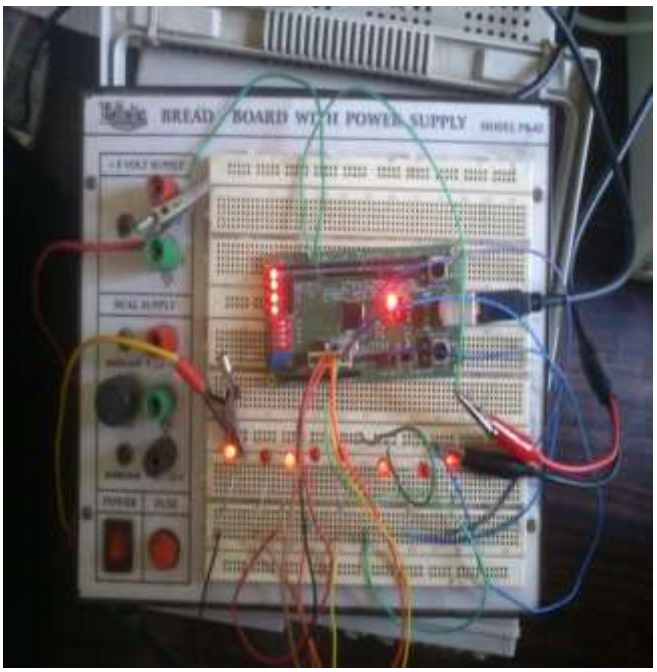

Fig. 6(b) Testing of the Coded Microcontroller

The coded microcontroller is then interfaced with all the binary graded capacitors and the relay driver circuit. The complete assembly along with induction motor is shown in figure 7.The motor is fed from single phase supply and the motor is gradually loaded in steps. The variations in motor parameters are observed and the motor parameters like voltage, current, power and power factor are recorded. These observations are recorded before and after implementation of APFC scheme which is presented in the result section.

Fig. 7 Complete Assembly of Motor Along with APFC

IV. RESULTS

The method was implemented on induction motor as stated in the implementation section. By comparing data of induction motor before implementation of APFC and after implementation of APFC we can observe that PF of IM is improved and for the same value of power, current drawn by an induction motor is reduced. E.g. no load current IM before employing APFC is 2.6A and it is reduced to 1.8A after employing APFC. The results of before and after implementation are shown in Table III and IV respectively. The same data is used to plot the change in variation of power factor and motor current for the same values of motors active power requirements. Figure 8 and 9 show the variation of PF and current with respect to change in active power of motor before and after implementation of APFC.

Table III Data of 0.75HP, 1-ph induction motor before implementation of APFC

Voltage (V)	Current (A)	Power (W)	Active Power (VA)	CosØ
200	2.6	120	520	0.230
198	2.8	260	554.4	0.467
194	3.0	340	582	0.584
194	3.2	400	620.8	0.640
192	3.4	440	652.8	0.670
192	3.7	500	710.4	0.700
192	4.0	550	768	0.716
190	4.3	600	817	0.730

Table IV Data of 0.75HP, 1-ph induction motor after implementation of APFC

Voltage (V)	Current (A)	Power (W)	Reactive Power (VA)	CosØ
200	1.8	120	360	0.27
196	2.1	260	411.6	0.631
196	2.4	340	470.4	0.723
196	2.7	400	529.2	0.756
195	3.0	440	585	0.752
194	3.4	500	659.6	0.758
194	3.6	550	698.4	0.788
193	3.8	600	733.4	0.818

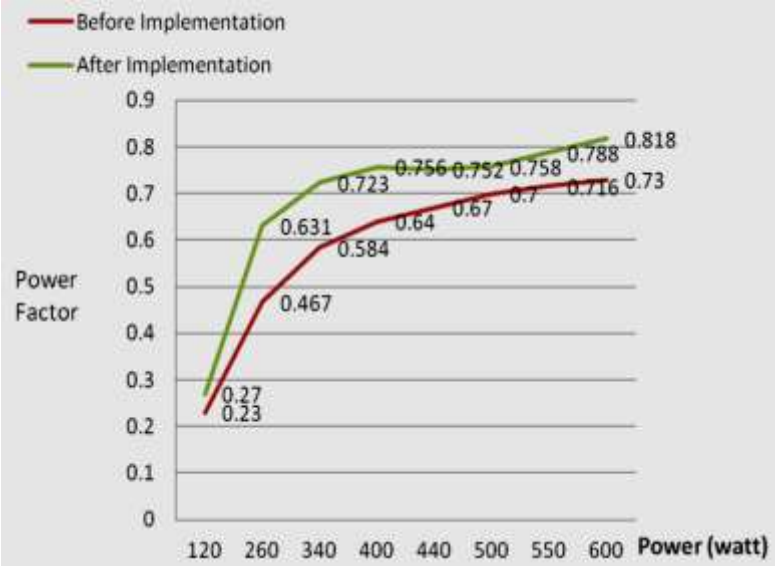

Fig. 8 Comparison of Power Factor Before and after Implementation of APFC with Graded Capacitors

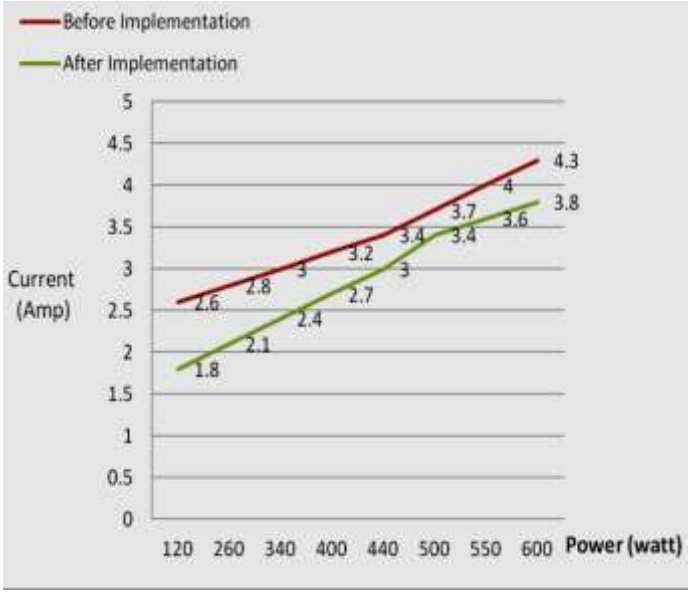

Fig. 9 Comparison of Motor Current before and after Implementation of APFC with Graded Capacitors

V. CONCLUSION

This paper presents a novel methodology for automatic power factor controller. It monitors supply power factor and automatically controls it by switching the graded capacitors. The binary graded capacitor arrangement offers fine tuning of effective capacitance and there by accurate compensation of reactive power to achieve desire power factor. The grading reduces the requirement of high values of capacitances and thus reduces the cost of APFC equipment. The results obtained by application of grading were good and meet the calculated expectations.

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