INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume 3, Issue 6)
Available online at www.ijariit.com

Design and Implementation of Microprocessor Trainer Bus System

Dr. Tin Tin Nwet
Department Computer System and Technology
Computer University, Sittwe, Rakhine, Myanmar
ttnwet@gmail.com

Dr. Phyu Phyu Shein
Department Computer System and Technology
Computer University, Dewai, Rakhine, Myanmar
maphyu.shein79@gmail.com

Abstract: This paper presents a part of a microprocessor trainer system. This paper has six modules. All modules are connected on the bus paths. Control signal such as Direct Memory Access (DMA), I/O Module and memory Modules are attached to the bus. In this paper, the bus has four lines of the bus. They are a line of the address, data, control (Memory Read/ Write and I/O Read/Write) and power. The address bus and data bus are 16 bits. Several Microcontrollers are in this paper. PIC 16f877 is used in a DMA module (direct memory access) and I/O module. PIC 74LS573 is applied as Latch, PIC74LS244 is used as a bus driver and PIC74LS255 is applied as a bus transceiver. PIC18f452 is used in CPU module. Each type of bus has its own requirements and properties.

1. INDRODUCTION

1.1 Basic Computer Architecture

Microprocessors are central components of almost all digit systems because combinations of hardware and software are used to solve design problems. The computer is formed by combining a microprocessor and provides an exile framework that orchestrates the behavior of hardware that has been customized to the application. When many people think about computers, images of desktop PCs and laptops come to their minds. Computers are much more diverse than the stereotypical image and permeate everyday life in increasing numbers. Small computers control microwave ovens, telephones, and CD players. Computer architecture is fundamental to the design of digital systems. Understanding how a microprocessor as a central control element. The microprobe becomes a programmable platform upon which the major components of an algorithm can be implemented. Digital logic can be designed to surround the microprocessor and assist the software in carrying out space's set of tasks. Basic microprocessor operation is presented from a hardware perspective to show how instructions are executed and how interaction with other system components is handled. Interrupts, registers and how interaction with other system components is handled. Interrupts registers and stacks are introduced as well to provide an overall picture of how computers function. Following this basic introduction is a complete example of how an actual eight-bit computer might be designed, with a detailed description of bus operation and address decoding. Once basic computer architecture has been discussed, common techniques for improving and augmenting microprocessor capabilities are covered, including direct memory access and bus expansion. These techniques are not relegated to high-end computing but are found in many smaller digital systems in which it is more economical to add a little extra hardware to achieve feature and performance goals instead of having to achieve feature and performance goals instead of having to use a microprocessor that may be too complex and more expensive than desire.

Design Vs Architecture

Architecture is the art or science of building, a method or style of building. Thus a computer architect develops the performance specifications for various components of the computer system and dense the interconnections between them.

A computer designer, on the other lands, runes this component specification and implements them using hardware, software An architect's capabilities are greatly enhanced if he is also exposed to the design aspects of the computer system. A computer system can be described at the following levels of detail: [12]

- Processor-memory-switch (PMS) level, at which an architect views the system. It is simply a description of system components and their interconnections. The components are species to the block-diagram level.

- Instruction set level, at which level the function of each instruction is described. The emphasis of this description level is on the system rather than the hardware structure of the system.

- Register transfer level, at which the hardware structure is more visible compared to previous levels. The hardware elements at this level are registers that retain the data being processed until the current phase of processing is complete.

- Logic gate level, at which the hardware elements are logic gates and .dips-.ops. The behavior is now less visible, while the hardware structure predominates.

- Circuit level, at which the hardware elements are resistors, transistors, capacitors, and diodes.

- Mask level, at which the silicon structures and their layout that implements the system as an IC are shown.

As one moves from the .rest level of description towards the last, it is evident that the behavior of the machine is transformed into hardware-software structure. A computer architect concentrates on the .rest tow levels described above, while the computer designer takes the system design to the remaining levels. [13]

1.2. Clock Control Signal

One of the most important control signals in any microprocessor-based system is the system clock. This signal provides the timing information for all the system's activities. Clock signals may be generated on the microprocessor chip, or by special IC signal generators. Microprocessors with internal clock generators usually require that an external crystal be connected to their clock input pins. [W10]

2.3 Bus-Based Dynamic Interconnection Networks

2.3.1 Single Bus Systems

A single bus is considered the simplest way to connect multiprocessor system. A system consists of N processors, each having its own cache, connected by a single bus system. [5]

2.3.2 Shared bus

The use of local caches reduces the processor-memory traffics. All processors communicate which a single memory. The typical size of such a system varies between 2 and 50 processors. The actual size is determined by the traffics per processor and the bus bandwidth (denied as the maximum rate at which the bus can propagate data once transmission has started). The single bus network complexity, measured in terms of the number of buses used, is O (1), while the time complexity, measured in terms of the amount of input to output delay is O (1), while the time complexity, measured in terms of the amount of output delay is O (N). Although simple and easy to expand, single bus multiprocessors are inherently limited by the bandwidth of the bus and the fact that only one processor can access the bus, and in turn only one memory access can take place at any given time.

2.4 Multiple Bus Systems

The use of multiple buses to connect multiple processors is a natural extension to the single shared bus system. A multiple bus multiprocessor system uses several parallel buses to interconnect multiple processors and multiple memory modules. A number of connection schemes are possible in this case. Among the possibilities are the multiple buses with full bus-memory connection (MBFBMC), multiple buses with single bus memory connection (MBSBMC), multiple buses with partial bus-memory connection (MBPBMC), and multiple buses with class-based memory connection (MBCBMC). [5]

2.5 Objective

The objectives of the paper are

To design to support a bus system to all module

To operate sufficient current and up to 10MHz clock frequency

To study the signal on the designed bus system

To gain on the experience of designing bus system

2.6 Contribution

A bus is a common electrical pathway between multiple devices uses can be categorized by their function. A bus is a common pathway that connected a number of devices. An example of a bus can be found on the motherboard (the main circuit board that contains the central processing unit) of a personal computer (For a lock at a real motherboard) A typical motherboard contains integrated circuit (ICs) such as the CPU ship and memory chips, board traces that connect the chips and a number of buses for ships or devices that need to communicate with each other.

The main contribution of this paper is to design and implementation of Microprocessor Trainer Bus System. This system is a part of Microprocessor Trainer. This trainer Bus System has six modules and all are connected by the bus. The bus system has address bus, data bus, and control bus. As long as the driver is active in a valid state. No input specification in violated as long as the rise and fall time are within the data sheet limits. However, the driver is in a high impedance state, the receiver input is no longer at a defined level and tends to floats. This situation can worsen when several transceivers shares the same bus.

Many Microcontrollers is used in this paper, PIC 16f877 is used as bus grand (on the direct memory access DMA), PIC 74LS573 is applied as Latch, PIC74LS244 is used as a bus driver and PIC74LS255 is applied as a bus transceiver.

Fig shows that Microprocessors are used in this paper.

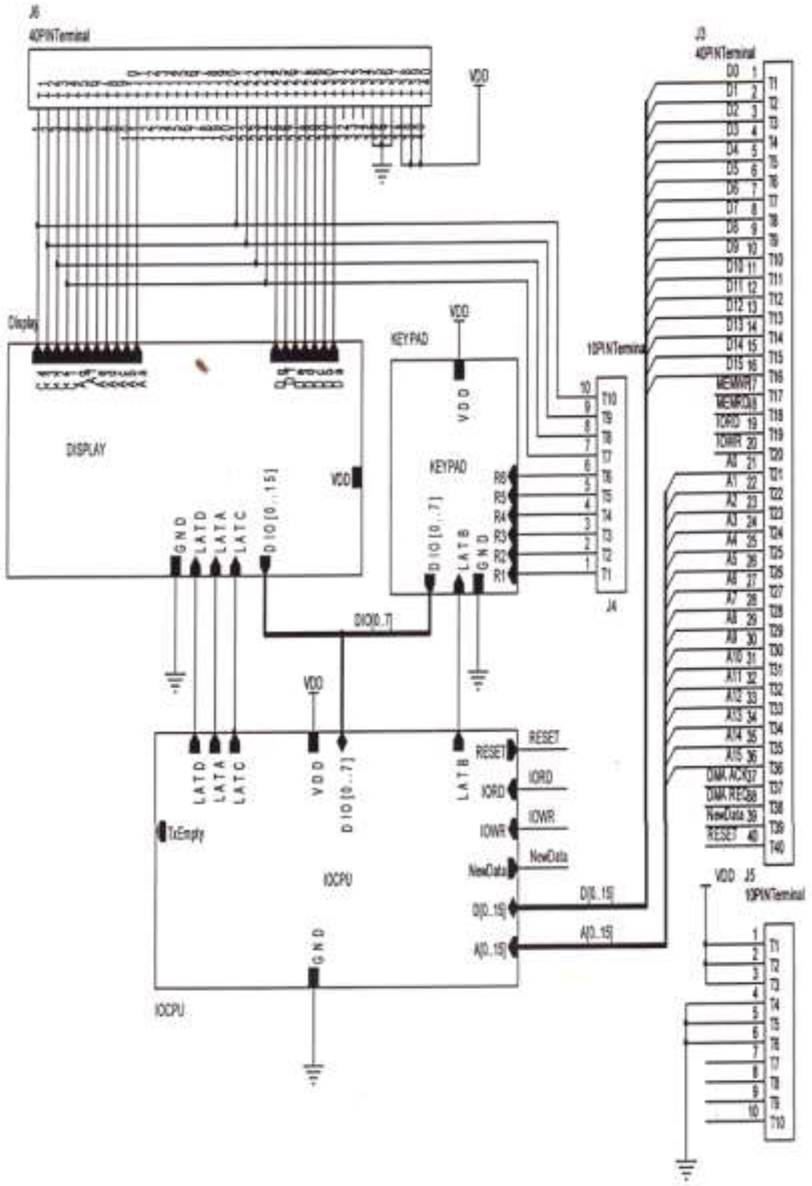

Figure Bus Connection to CPU, Keypad and Display

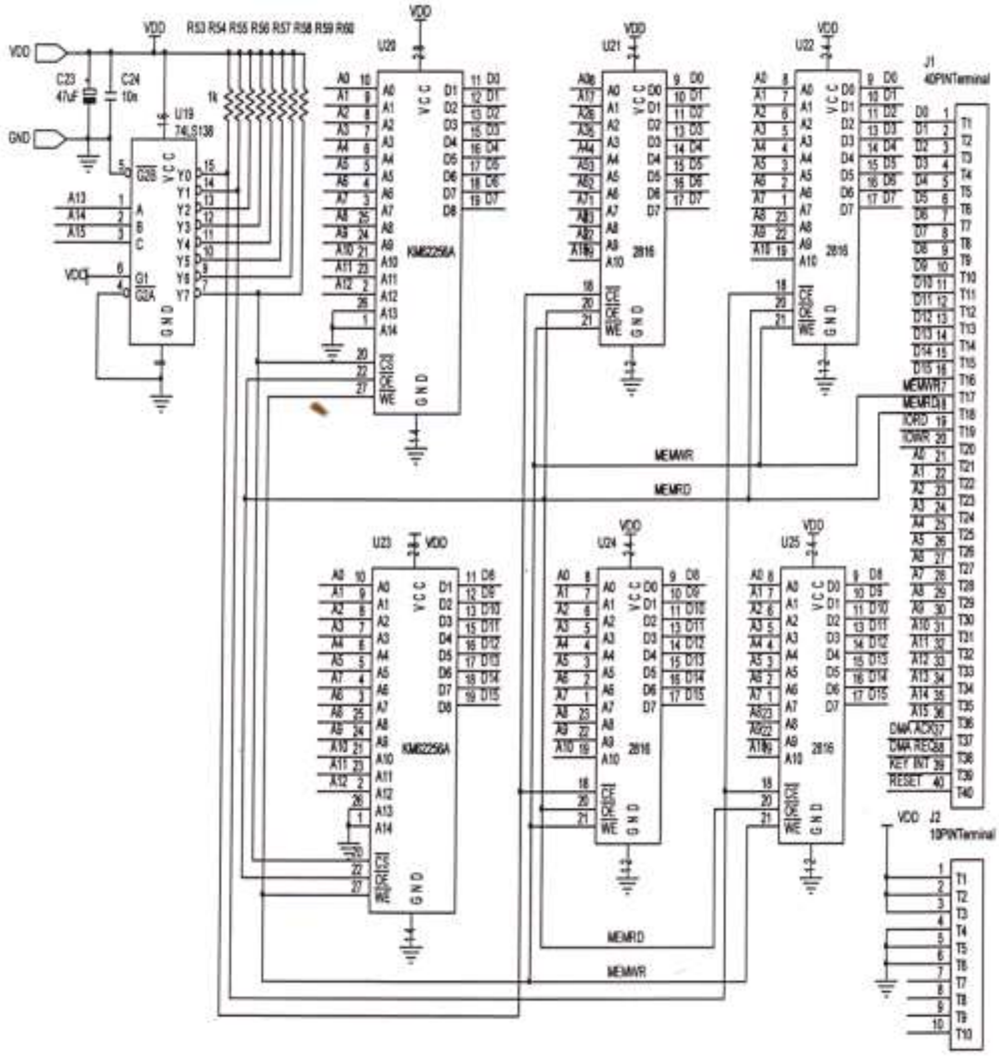

Figure Circuit Diagram of Bus Connection to I/O Read /Write

As long as the driver is active in a transmission path or bus, the receiver's input is always in a valid state. No input specification is violated as long as the rise and fall time are within the data sheet limits. However, when the driver is in a high impedances state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers shares the same bus.

2.6.1 Outline of Paper

This paper is composed of five chapters. Chapter one introduces basis computer Architecture, type of computers and explains the project overview. In Chapter two, Introduction of Bus System and Share Buses are described. Microcomputer Bus Structure and Logic Family Characteristics and Interfacing are explained in chapter three. In chapter four, PIC Microcontrollers and Implementations of the system will be expressed. Finally, it is included with a summary, conclusion, and discussion of this paper, in chapter five.

3. INTRODUCTION OF BUS SYSTEM

A bus is basically a collection of wires which is responsible for interconnection the various components of a microcomputer together in order to allow the exchange of data between these components and to provide power to them. Early microcomputer system possessed relative simple bus system which was often adapted on the basis of their price and availability rather than for any distinguishing technical features. Current state-of-the-art PC bus system is the product of a number of generation of bus technology and represent the end-product of numerous manufacturers' attempts to get it right and establish a particular standard as a common to the industry and PC platform.

Backplane bus system typically consists typically consists of a series of circuit boards mounted perpendicularly onto a motherboard via a series of slot connectors. This design allows for the exchange of bus devices and provides greeted flexibility in the range of devices a system can support. Devices operating on a bus can be divided into two categories, bus masters and bus salves. Bus masters are devices capable of initiating any bus cycle (memory read/write, port addressing, etc) and bus slaves are devices which are not capable of initiating a bus cycle but merely responding to it. A third possible category is intelligent slaves which have their own intelligent controlling devices but do not assert control over the bus. A minimal bus has to feature three types of lines.

- Control Line
- Address Line
- Data Line

3.1 Simple Bus Architectures

A computer system may contain many components that need to communicate with each other. In a worst case scenario, all components need to simultaneously communicate with every other component. The numbers of links become prohibitively large for even small values. A bus is a common pathway that connects a number of devices. An example of a bus can be found on the motherboard (the main circuit board that contains the central processing unit.

An I/O bus is used for a number of cards that plug into the connectors, perpendicular to the motherboard in this example configuration. A bus consists of the physical parts, like connectors and wires and a bus protocol. The wire can be partitioned into separate groups for control, address, data, and power. A single bus may have a few different power lines. The devices share a common set of wire and only one device may send data at any one time. All devices simultaneously listen but normally only one device receives. Only one device can be a bus master and the remaining devices are considered to be salves. The master controls the bus can be either a sender or a receiver. An advantage of using a bus is to eliminate the need for connecting every device to every other device, which avoids the wiring complexity that would quickly dominate the cost of such a system. Disadvantages of using a bus include the slowdown introduced by the master/salve configuration, the time involved in implementing a protocol and the lack of scalability to large sizes due to fan-out and timing constraints. A bus can be classified as one of two types; synchronous or asynchronous. For a synchronous bus, one of the devices that are connected to the bus contains an oscillator (a clock) that sends out a sequence of 1’s and 0’s at time intervals, which corresponds to a clock rate of 100 MHz Ideally , the clock would be a perfect square waves (instantaneous rise and fall times) . In practice, the rise and fall times are approximated by a rounded, trapezoidal shape.

This system has six modules and all are connected data Bus [DO~D15] and address Bus (AO~A15). Control signal such as Memory Read (MEMR), Memory Write (MEMW), Input Output Read (I/ORD), Input Output Write (I/O WR) is used. All modules are connected in 5v (DC) supply. The central processing unit (CPU) is made multiplex in the address and data 16 Lines.

If data is read from external RAM, 16 bits address is generated from PORT D and PORTC.these4 address values are given pulse and cached in PIC 74 LS 573 Latch, Address Latch Enable (ALE). Since address enable (AE) line is law level, Address 16 line is reached on the address bus. Having address value in the DATA bin, another module is disabling. SO, other data are no adulterate,(Bus contention).making Address is Latch PORT C is changed in to Low level. Data from PORT D and PORT C is read. MRMR pin is changed level.

As long as the driver is active in a transmission part or bus, the receivers, the input is always in a valid state. NO input specification is violated as long as the rise and fall time are within the data sheet limits. However, when the driver is in a high impedance states, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus.

When all transceivers are inactive, the bus-line levels are undefined. These devices are controlled by DMA ACK from the main CPU (PIC 18F452) and by ALE from the DMA controller. The enable (E) pin is connected by ALE pin from the transceivers are designed for asynchronous

3.1.2. Microcomputer Bus Structure

One of the misunderstood features of computers today is the bus. Today one hears about the system bus, the local bus, the SCSI bus, the ISA bus, the PIC bus, the VL-bus and now USB. These terms are also confused with other terms for slots, port, connector, etc.

3.2 Bus Definition

Basically, it is a mean of getting data from one point to another, point to point B, one device to another device, or one device to multiple devices.

The bus includes not only the actual capability to transfer data between devices, but also all appropriate signaling information to ensure complete movement of the data between devices, but also all appropriate signaling information to ensure complete movement of the data from point A to point B. To avoid loss of data, a bus must include a mean of controlling the flow of data between two devices, in order to insure that both devices are ready to send and/or received information. Finally, both ends must understand the speed with which data is to be exchanged.

A bus provides for all of these elements, and it includes a port definition to allow physical interfacing or connection of two or more devices. The bus has various component parts of a microcomputer connected by a number of different wires, which usually appear in the form of tracks on a Printed Circuit Board (PCB) these wires can be classified into four functional groups.

3.3 Bus Synchronization

A bus can be classified as synchronous or asynchronous. The time for any transaction over a synchronous bus is known in advance. In accepting and/or generating information over the bus, devices take the transaction time into account. Asynchronous bus, on the other hand, depends on the availability of data and the readiness of devices to initiate bus transactions. In single bus multiprocessor system, bus arbitration is required in order to resolve the bus contention that takes plate when more than one processor completes accessing the bus. In this case, processors that want to use the bus summits their requires busing arbitration logic. The latter decides, using a retain priority scheme, which processor will be granted access to the bus during a certain time interval (bus master). The process of passing bus mastership from one processor to another is called handshaking and required the use of two control signals. Bus request and bus grant. While the second indicates that bus mastership is granted. A third signal, called bus busy, is usually used to indicate whether or not the bus is currently being used. In deciding which processor gains control of the bus, the bus arbitration logic uses a preened priority scheme. Among the priority schemes used are random.

3.3.1 Speed of Data Transfer

3.3.1.1 **Serial Vs Parallel**

One main aspect of a bus is whether the data is transferred in a serial or parallel function. In serial mode, the bits of each character are transmitted one at a time, one another. For example, with each character containing 8 bits, the character is sent between devices, senting the first bit, then the second bit, third bit, and so on until the eighth bit is sent. Contrast this with the parallel transmission, where the bits of a character or data are transferred simultaneously. The parallel interface or transmission contrasts with the serial by allowing the devices to transmit all of a character's bits simultaneously instead of one at a time.

3.2.2 Sustained Vs Burst Throughput

A burst rate is a maximum rate at which data can be continuously sent over the bus. The sustained rate is the rate at which data can be sent over the bus in a consistent manner. It is a better metric than the burst rate for throughput expectations on a bus, as it reflects the typical transmission speed.

3.2.2.1 Speed Buses

The speed of the serial bus is general expressed in bits per second (bps). When a port, bus or interface highlights 56-Kbps capability, the maximum throughput is 56,000 bits per second. For a rough estimate of maximum throughput, one can add the start and stop bits of a typical character, totaling 10 bits per character, and divide the interface speed by the number of bits per character. In the case of a 56-kbps bus or interface, the maximum throughput would be approximately 5600 characters per second. This is only an approximation. Each bus has what is referred to as "overhead" to provide the other highlighted functions of flow control, addressing etc. The simplicity of the bus will dictate the amount of overhead required. Some interfaces, such as those of devices that are locally connected via RS-232, have little overhead. Hence the actual through putting alternatively close to the maximum speed rating. The RS-232 interface is NOT generally referred to as a bus, but it does have the elements of a bus. The keyword here is maximum; most buses are set up electrically to support a maximum throughput rate, as well as a sustained throughput rate. When calculating throughput, use the sustained rate for a closer approximation of speed.

4.1 PIC MICROCONTROLLER AND SYSTEMIMPLEMENTATION

PIC microcontrollers: low-cost computers-in a chip; they allow electronics designer and hobbyists add functions that mimic big computers for almost any electronic product or project.

PIC microcontrollers use von Neunann structure or architecture, which means that they have the separate buses for data and instructions. The ROM holds instructions, and the RAM is used for the data. PIC software is normally written in assembly language. Programming the PIC chip are still using its instruction set, and the assembler program works out the binary codes for providing other help.

In order to program PIC chips we need a suitable development or programming system is a need. It should include an assembler, the programming software, and hardware, plus some form of PIC simulator or emulator.

The program for a PIC chip is stored in its ROM. There is more than one type of ROM and most of the PIC chips are equipped with EPROM (erasable programmable read only memory). It is not difficult to program PIC chips using the systems that are now readily available. Because the contents of the EPROM are erasable, once a chip has been programmed it is possible to re-use it by erasing the contents of EPROM and re-programming the chip.

Some of the PIC processes are non- erasable chips, called OTP (one time programmable) chips. The erasable chips have a life of over 10,000 programming and erasure cycles.

The most basic of the mainstream PIC chips are contained in ordinary 18-pin DIL plastic encapsulations and have two input/output ports. These consist of one 4-bit port and one 8-bit port (i.e. a total of 12 input/ output lines), and they respectively designated port A and port B.

Use a crystal controlled clock where either very fast operation (over 4 MHz) or good timing accuracy is required.There is no lower limit on the on the clock frequency if a C-R clock oscillator or an external type is used. Each line of a PIC port can be set as input or an output via the appropriate control register (TRIS for port A, TRISB for port B, etc.). [W3]

The memory of the PIC microcontrollers is divided into program memory and data memory. The devices also use separated buses to communicate with each memory type. The Harvard Architecture allows for other enhancements. The instructions may be sized differently than 8 bit wide data. The data memory in the PIC microcontrollers can be broken down into general purpose RAM and the special function registers.PIC microcontrollers are becoming ubiquitous in temperature and control applications. The digital/ analog hybrid characteristic provided by the built-in A/D converter provides the end user with great flexibility in how a PIC microcontroller can be used for both data acquisition and control.

In this project, many microcontrollers are used.PIC 16f 877 is used as bus grant (on Direct Memory Access), PIC 74LS573is used as Latch, PIC 74LS244 is used as a bus driver and PIC74LS255is used as a bus transceiver.

4.1.1 Hardware Overview of PIC16f877

The PIC16f877 has 5 digital I/O ports (A-E) each between 3 and 8 bits wide.

Each port is mapped in to the register file space, and many be read/written to like any other register. The circuitry is such that it is no possible to physically input to output from a particular pin simultaneously. For most ports, the I/O pins direction (Input or output) is controlled by the data direction register, called the TRIS register. TRIS<x> controls the direction of PORT<x>.A "1" in the TRIS bits corresponds to that pin being an input, While an "O" corresponds to that pin being and output. An easy way to remember is that a "1" looks like an "I" (input) an an "O" looks like an "O"(output). The PORT register is the latch for the data to be output. When the PORT is ream, the device reads the levels present on the I/O pins (not the latch).this means that care should be taken with reading –modify-write commands on the ports and changing the direction of a pin from an input to an output.

These devices are controlled by DMA ACK from the main CPU (PIC18f452) and by ALE from the DMA controller. The enable (E) pin is connected by the ALE pin from the DMA controller and the output enable (OE) is connected by the DMA ACK pin from the transceivers are designed for asynchronous. The control function implementation minimizes external timing requirements. The devices allow data transmission from the A bus to B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that the buses are effectively isolated. They are used here to latch the output either from the PIC 18f452 or PIC16f877. And G pin can be used to isolate the buses. The DIR pin controls the transmission of data from the bus A to bus B or bus B to bus A. DMA controller uses request (DMA REQ) and acknowledge (DMA ACK) signals to ask the processor (PIC18f452). The processor will finish the present bus cycle (not necessarily the present instruction) and respond to the DMA request by putting low on its DMA ACK pin, thus telling the DMA controller that it can go ahead and use the buses to perform its task, DMA ACK pin must remain active high as long as DMA is performing.[w9]

In the system, the PIC16f877 address and control outputs and data bus pins are basically connected parallel with the system buses.

Buses grant signal is placed on the DMA module. If CPU requests the bus, bus grant on the DMA is enabled and LED is on. If CPU requests the bus, bus grant on the DMA is enabled and LED is on. If CPU is running, bus grant enables and LED is off.

4-2 Hardware Overview of PIC74LS573

The 74LS573Bs in the circuit are octal latches with three-state outputs. It is an octal transparent latch coupled to eight 3-State outputs devices. The two sections of the devices are controlled independently by enable (E) and output enables (OE) control gates. The data on the D inputs is transferred to the latch outputs when the enable (E) input is high. The latch remains transparent to the data input while E is high, stores the data that is present one setup time before the High-to-low enable the transition. It is an 8 bit edge triggered register coupled to eight 3 –state output buffers. The two sections of the device are controlled independently by the clock (CP) and output enable (OE) control gates. The register is fully edge triggered. The state of the D input, one setup time before the low-to-High clock transition is transition is transferred to the corresponding flip-flop's Q output. The active-low output enables (OE) controls all eight 3 State buffers independent of the latch operation. When OE is low, latched or transparent data appears at the output. When OE is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus. [W8]

Pins	description
Do-D7	Data Inputs
E	Latch enables input
CP	Clock pulse

OE Output Enables input (active-low)

Q0-Q7 Data Output

In this project, two 74LS573 are used as a latch.

4.3 **Overview of System**

Most important to the system bus model, The communication among the components are by means of a shared pathway called the system bus, which is made up of the data bus [which carries the information being transmitted], the address bus [which identifies where the information is being sent], and the control bus [which describes aspects of how the information is being sent ant in what manner]. There is also a power bus for electrical power to the components, which is not shown, but its presence is understood. Some architecture may also have a separate I\O bus. Physically, busses are made up of collections of wire that are grouped by function. A 16-bit data bus has 16 individual wires, each of which carries one bit of data [as opposed to address or control information]. In this sense, a system bus is actually a group of individuals' busses classified by their function. The data bus moves data among the system components. Some systems have separate data busses for moving information to and from the CPU, in which case there are a data-in bus and a data – out bus. More often a single data bus moves data in either direction, although never both directions at the same time. If the bus is to be shared among communicating entities, then the entities must have distinguished identities; address. In some computers, all address are assumed to be memory address whether they are in fact part of the computer's memory, or are actually I/O devices, while in others I/O devices have separate I/O addresses.

A bus is a common electrical pathway between multiple devices uses can be categorized by their function. A bus is a common pathway that connects a number of devices. An example of a bus can be found on the motherboard (the main circuit board that contains the central processing unit) of a personal computer, as illustrated in simplified form. A typical motherboard contains an integrated circuit (ICs) such as the CPU chip and memory chips, board traces (wires) that connect the chips, and a number of buses for chips and a number of buses for chips or devices that need to communicate with each other.

CONCLUSION AND FURTHER EXTENSION

Conclusion

In a computer system, the various subsystems must have interfaces to one another. The memory and processor need to communicate, as to the processor and the I/O devices. A bus is a share medication which use one set of wire to connect multiple subsystems.

A bus basically a collection of wires which is responsible for interconnection the various components of a microcomputer together in order to allow the exchange of data between these components and to provide power to them. Early microcomputer systems possessed relatively simple bus systems which were often adapted on the basis of their price and availability rather than for any distinguishing technical features. Current state-of-the-art PC bus systems are the product of numerous manufactures attempts "get it right" and establish a particular standard as common to the industry and PC platform.

A bus is a common electrical pathway between multiple devices. Buses can be categorized by their function. They can be used to transport the internal data of the CPU to enter the ALU and generated out of it. Or data in the other module can be sent into the CPU connection it to memory or I/O devices. Each type of bus has its own requirements and properties.

According to the testing facts, it is found that all the system buses are functioning well. However, it is found that some error occurs when the clock signal is high. This is because of being down to power line voltage and to the quality of some interface IC is fallen. If PCB design is used as the double layer, the buses quality will be better.To know the various operation methods which depend on signal direction, the modules are changed their positions on the board. There will be no change after testing. Because of the scare of instruments, the bus signals are not tested practically. If it can be done so, the quality of the buses can actually be known.

To measure signals on the buses, oscilloscope, impedance meters, logic analyzers, high frequency signal generator and screen capture are required.

If the bus length is short, the value of bus capacitance will be greater and operates quickly.

In the thesis, bus path is because it is used to show demonstration and so sometime error occurs.

If the cards are placed in vertical, bus path is short and it gets less capacitance.

APPENDIX

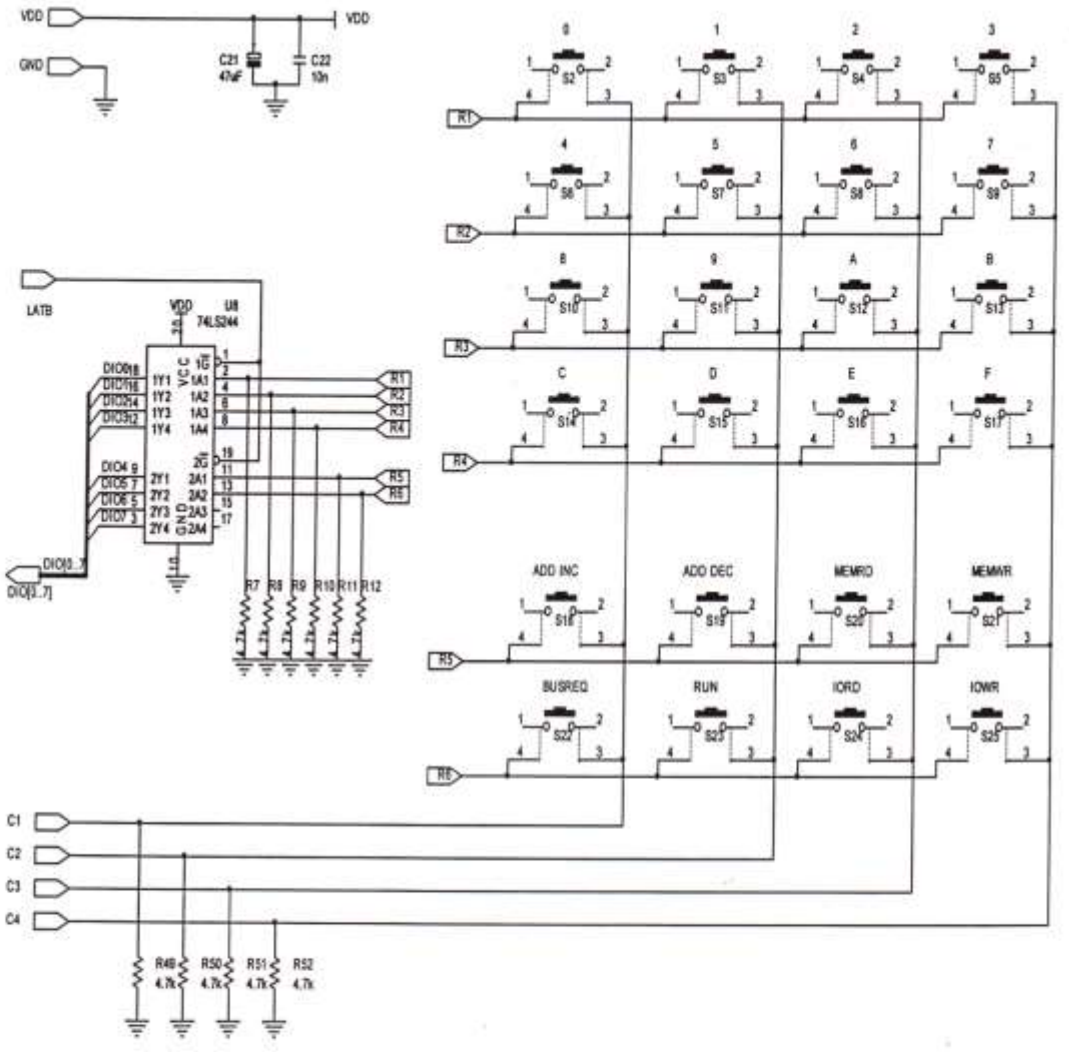

Figure I/O Display

FURTHER EXTENSIONS

This Microprocessor Trainers is 16 bits and then it uses 16 bits address bus and 16 data bus. It can be rebuilt 32 bits Microprocessor Trainer.

If PCB design is used as the double layer, the buses quality will be better. To know the various operation methods which depend on signal direction, the modules are changed their positions on the board. In testing to use instruments, rise/fall time, propagation delay time, setup time, hold time, tri-state enables and disables delays, pulse width, and clock frequency can be calculated.

Furthermore, this paper can be modified and improved bus design such as reflections, crosstalk, ground and supply-line noise and electric interface from pulse-type E.M fields.

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