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Common Mode Voltage Reduction for Three Phase Grid Connected Converters using Multi Level Pulse Width Modulation Techniques

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***Abstract:** This paper investigates the performance of three-phase grid connected multi level (PWM) inverter, with photovoltaic energy conversion system being the main application. The main purpose of this work is to reduce the common mode voltage (CMV) and common mode current (CMC), the performance of the inverter is studied thoroughly. Conventional PWM methods and recently developed reduced common mode voltage PWM (RCMV-PWM) methods are reviewed. The simulation results of CMV, CMC and Total Harmonic Distortion (THD) by applying all the PWM Techniques on a grid connected PV system using a three phase, three-level Multi Level Inverter (MLI) are studied. Amongst all the PWM Techniques, Near State PWM (NSPWM) Technique which is an RCMV-PWM Technique yields the best results.*

***Keywords:** Multi level inverter (MLI), Common-mode current (CMC), Common-mode voltage (CMV), Photovoltaic, Pulse width modulation (PWM).*

I. INTRODUCTION

These days, the usage of renewable sources of energy has increased rapidly due to the spread of awareness about their importance. One such energy is solar energy and Photo Voltaic (PV) technology has become much popular due to its vast advantages [1]. The critical factors evaluated while installation of PV systems is the conversion efficiency, weight, size.

Therefore, transformer fewer converter circuits are often favoured. Nowadays, the usage of grid connected converters integrating PV technology without transformers [2] is a common sight.

But due to, the absence of the transformer lack of isolation between the source and the load occurs which in turn leads to increased leakage currents which are also known as Common mode currents(CMC) and resulting Common mode voltages(CMV).

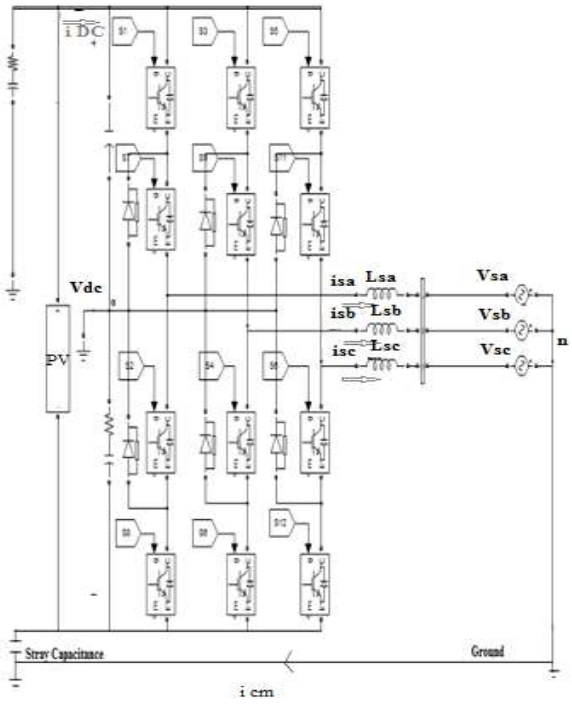


Fig 1: Transformerless grid connected PV system with 3-ϕ, 3-level MLI

The main advantage of using PV is that the global warming issues are taken care of, conversion efficiency is improved and many more factors are improved. So, this paper mainly deals with reducing of common mode current (CMC) and common mode voltages (CMV) using various advanced PWM techniques. Therefore, we are going to review and compare the various advanced PWM techniques applied on the proposed converters.

Fig 1 shows a typical three-phase transformerless grid-connected PV system. The stray capacitance results in the significant common-mode current (CMC) as the grid-connected converter switches at high-frequency pulse width modulation (PWM). In Fig 1, a 3-phase, 3-level multi level inverter(MLI) [3] is shown. There are many added advantages of an MLI. As the number of levels of a multi level inverter increases, the Total Harmonic Distortions(THD), CMV, CMC, DC bus ripples also reduce to a greater extent [5]-[8]. All the PWM techniques proposed in this paper are applied to the grid connected PV system incorporating MLI. The inverter topology consists of totally 12 switches, 4 per each phase. The total number of clamping diodes are 6, 2 per each phase. The principle of operation, mathematical formulas for the calculation of a number of switches, clamping diodes, capacitors are presented in [3],[4].

PWM Techniques play a vital role in minimizing Common-Mode Voltage (CMV), Common-Mode Current (CMC) and Total Harmonic Distortion (THD). In this paper, conventional PWM Techniques [Space Vector Pulae Width Modulation (SVPWM) Technique & Discontinuous Pulse Width Modulation (DPWM) Technique] are compared with Reduced Common-Mode Voltage Pulse Width Modulation Techniques [Active-Zero State Pulse Width Modulation (AZSPWM) Technique & Near State Pulse Width Modulation (NSPWM) Technique]. Reduced Common-Mode PWM Techniques yeilds the better results than Conventional PWM Techniques in terms of CMC, CMV, THD. On the whole NSPWM Technique yeilds the best result.

In Section II, all the PWM techniques are studied in detail. Section III deals with the control techniques of various PWM Techniques. In section IV, the simulation results are presented.

II. PULSE WIDTH MODULATION METHODS

1. Conventional Pwm Method

(a). Space Vector Pulse Width Modulation Method (SVPWM)

The Space Vector PWM is an advanced PWM Method and is the basic method of all vector PWM methods. The concept of this PWM Method can be referred from [20]-[21]. The switching pattern and CMV using SVPWM Method are shown below.

(b) Discontinuous Pulse Width Modulation Technique (DPWM)

By adding a properly selected zero sequence signals, different discontinuous modulating waveforms can be generated. If the augmenting zero-sequence signal is continuous it results in CPWM scheme or if discontinuous it results in DPWM schemes. A carrier based generalized PWM method comprising of all DPWM methods is considered as generalized discontinuous PWM scheme (GDPWM) [22].

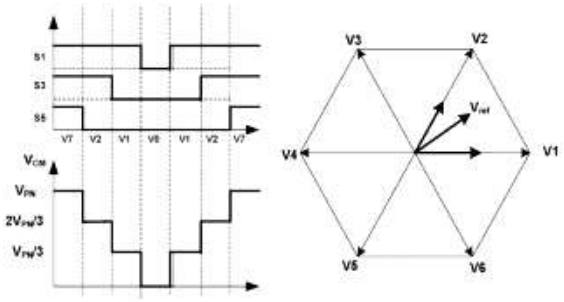


Fig 3: Switching pattern and CMV of SVPWM Technique

2. Reduced Common-Mode PWM Methods

(a) Active Zero State PWM Method (AZSPWM)

Active zero state PWM (AZSPWM) uses two adjacent active vectors in each sector like SVPWM. Instead of zero vectors, this method uses two opposing vectors with equal time to effectively create a zero vector. Further discussion can be referred from [15].

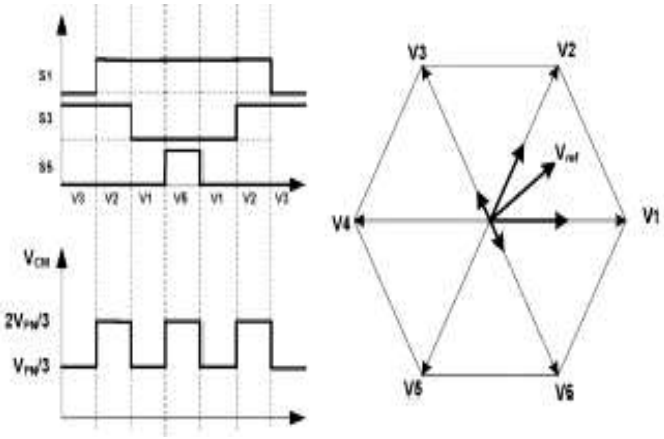


Fig 4: Switching pattern and CMV of AZSPWM Technique

(b) Near State PWM Method (NSPWM)

This method uses the group of three active vectors to produce desired voltage, two classical active vectors like SVPWM and nearest neighbour active vector for the third active vector. [16]-[18] can be referred for further information. The following diagram shows the switching pattern and CMV of this method.

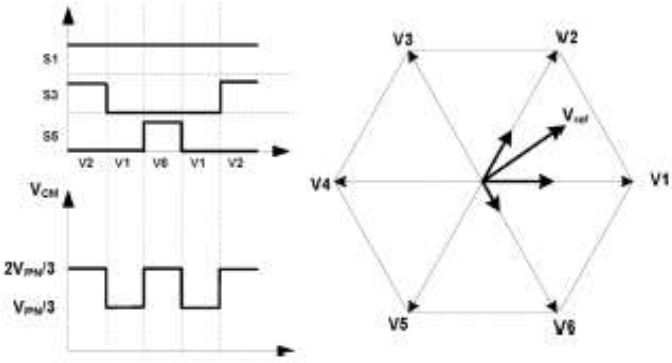


Fig 5: Switching pattern and CMV of NSPWM Technique

III. CONTROL STRATERGIES

The basic control strategy and the basic controller design are discussed in [19]. The control block diagrams of all the four PWM Techniques are given below. The multi level inverter in the figure 1 consists of 12 switches. The control strategy presented below only contains 6 switches. So, while simulation one more such controller block is connected and pulses are given to the remaining 6 switches. Due to the restricted font size, only one controller block is presented here.

(a) SVPWM Method:

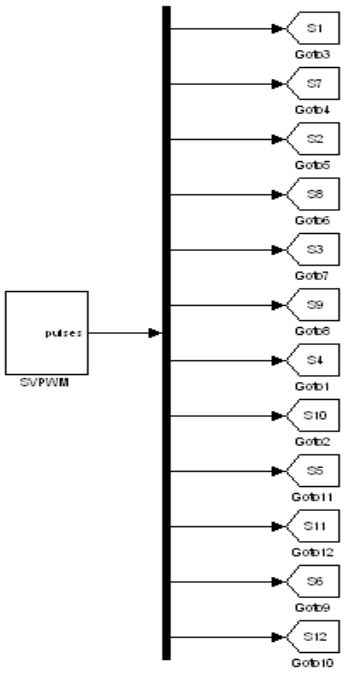


Fig 6: Control Block Diagram of SVPWM Method

In MATLAB Simulation, the Discrete SV PWM Generator block is already inbuilt. The three sine wave signals are given to two function blocks which convert 3-phases to alpha and beta values and are given to Discrete SV PWM generator block. The function in Fcn block is

$$((2/3)*u(1))-((1/3)*(u(2)-u(1))) \text{ --(1)}$$

And Fcn1 block is,

$$(2/\text{sqrt}(3))*(u(2)-u(1)) \qquad \text{--(2)}$$

From this pulses are generated and are given to the switches.

(b) AZSPWM Method:

In AZPWM Method the zero voltage sequence is generated according to the equation mentioned in [1]. Thereby, the zero sequence command is added to the phase voltages to generate the modified phase voltages and are compared with reference signals to generate pulses which feed the switches. A three phase PLL is used to give the angular frequency and is given to the lookup table. The sectors from the lookup table are taken and given to three multi port switches trough a gain according to [9]. This is used to detect where the reference voltage vector lies. The three multiport switches are used for three phases. The outputs from the multi port switches are given to relational operator which is compared with modified phase voltages to generate pulses.

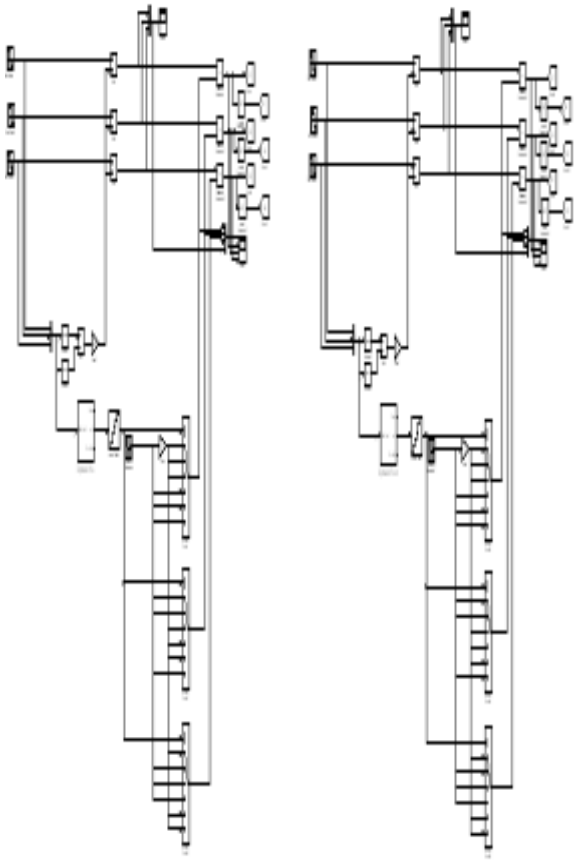


Fig 7: Control Block Diagram of AZSPWM Method

(c) DPWM Method

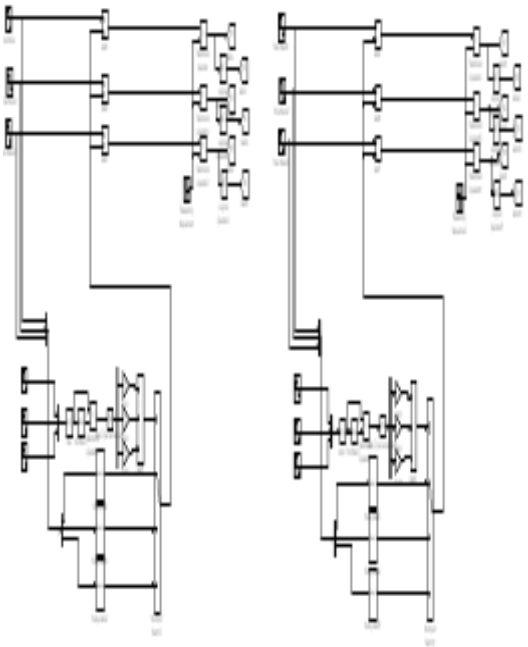


Fig 8: Control Block Diagram of DPWM Method

The DPWM Control Block is fed by three phase sine wave carrier signal. According to the reference equation given for the designing of zero sequence voltage command for DPWM Method, the zero voltage command is generated. The zero voltage command is added to the phase voltages to get the modified phase voltages. The modified phase voltages are then compared with reference repeating sequence to generate the pulses which are thereby fed to the gates of the switches.

(d) NSPWM Method

The control block diagram of NSPWM Method is similar to AZPWM Method except for the design of zero sequence voltage command. The zero sequence voltage command design is shown and explained below.

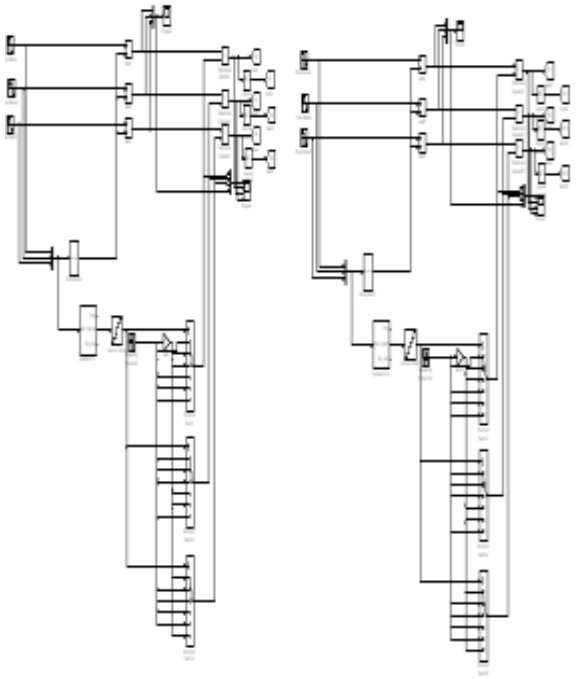


Fig 9: Control Block Diagram of NSPWM Method

The zero voltage sequence command block is designed according to the equation given for NSPWM Method in [1]. The absolute value is calculated by using absolute block of the three phase sine wave signal. Then the maximum of all the three phase voltages using max block is determined. Then the maximum value is sent through data type conversion block to convert it in to Boolean expressions. Then they are sent through gains and are added and sent to the multiport switch. The multiport switch gives the output. The input-output block is also designed as per the requirement of the equation.

IV. SIMULATION RESULTS

The Simulink model of figure 1 is constructed. The simulation results of common mode voltage (CMV), common mode current (CMC) and the spectrum of CMV using all the PWM Techniques discussed are presented in this section. Comparison of CMV's, CMC's, and THD's of all the PWM Techniques is presented in a tabular form.

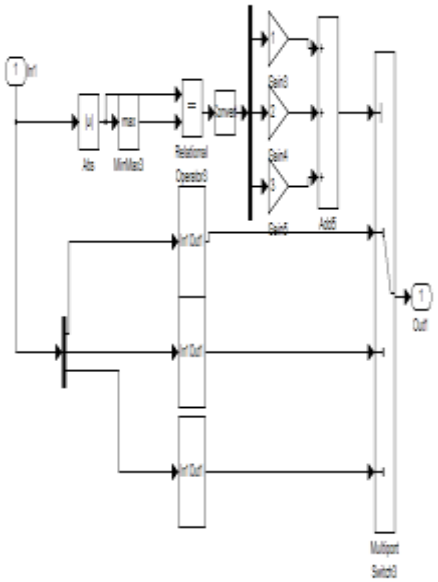


Fig 10: Zero sequence voltage block of NSPWM Method

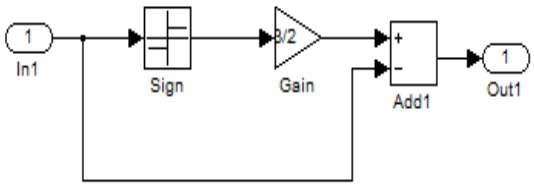
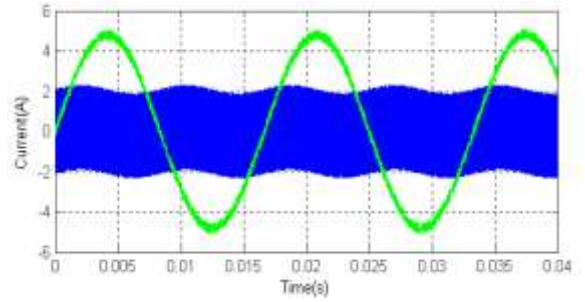
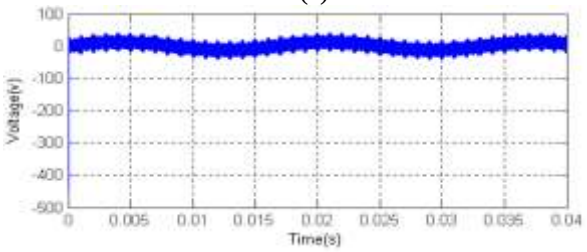


Fig 11: Input-Output block of Control Block Diagram of NSPWM Method

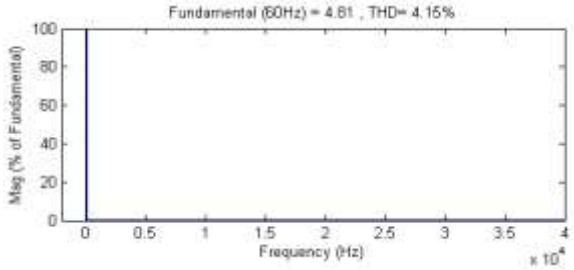
(a) SVPWM Method



(a)



(b)

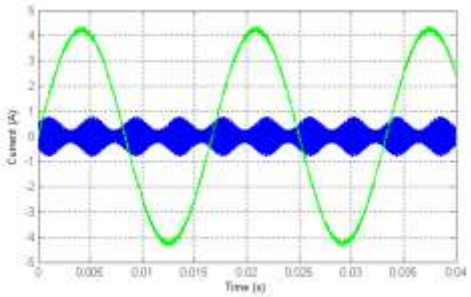


(c)

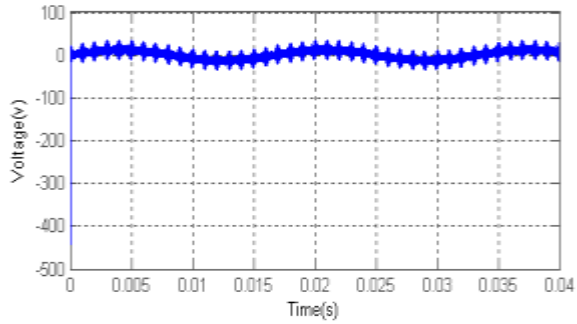
Fig 12: SVPWM at 10 kHz. (a)Phase current and the CMC (b) CMV (c) Spectrum of CMV

Fig 12 (a) shows the common mode current and a phase from three phase currents. It is almost around 1.475 Amps of RMS value. Fig 12 (b) shows common mode voltage which is around 15.93 Volts of RMS value. The spectrum of common mode voltage which is also known as FFT analysis is shown in Fig 12 (c).

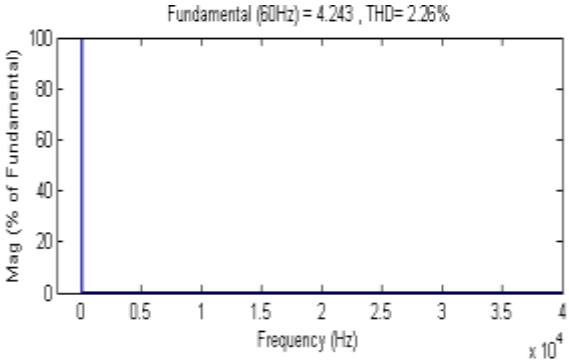
(b) AZSPWM Method



(a)



(b)

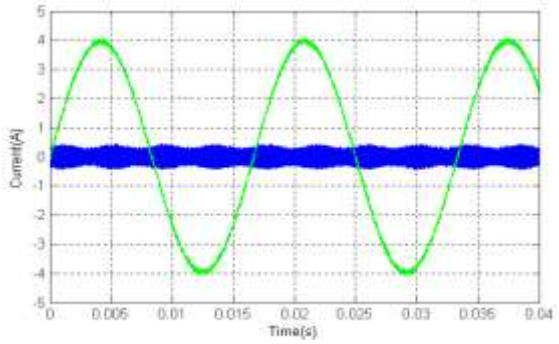


(c)

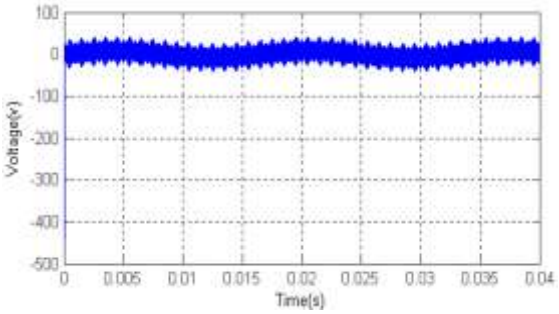
Fig 13: AZSPWM at 10 kHz. (a) Phase current and the CMC (b) CMV (c) Spectrum of CMV

(a) Fig 13 (a) shows the common mode current and a phase from three phase currents. It is almost around 0.385 Amps of RMS value. Fig 13 (b) shows common mode voltage which is around 11.52 Volts of RMS value. The spectrum of common mode voltage which is also known as FFT analysis is shown in Fig 13 (c).

(c) DPWM Method



(a)



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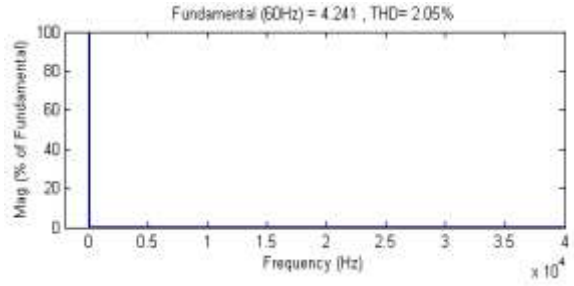
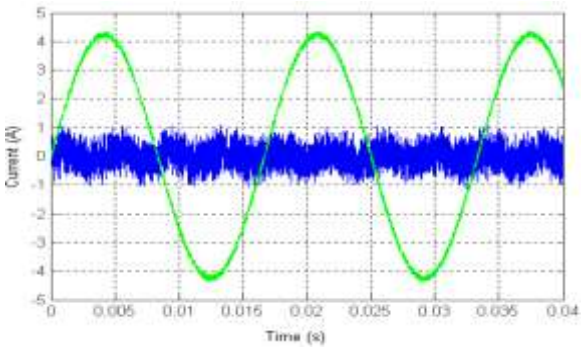


(c)

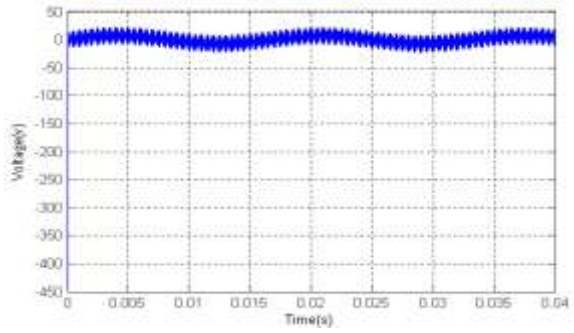
Fig 14: DPWM at 15 kHz. (a)Phase current and the CMC (b) CMV (c) Spectrum of CMV

Fig 14 (a) shows the common mode current and a phase from three phase currents. It is almost around 0.2475 Amps of RMS value. Fig 14 (b) shows common mode voltage which is around 17.12 Volts of RMS value. The spectrum of common mode voltage which is also known as FFT analysis is shown in Fig 14 (c).

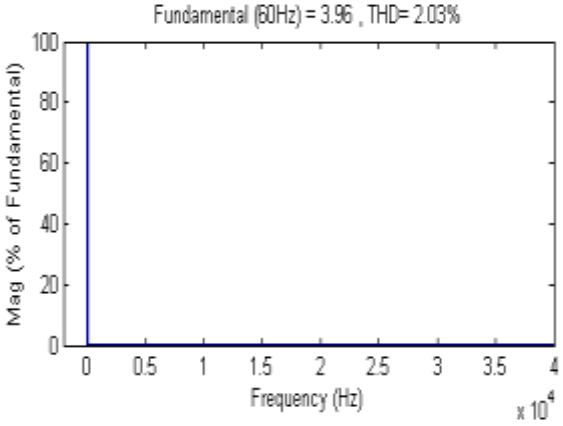
(d) NSPWM Method



(a)



(b)



(c)

Fig 15: NSPWM at 15 kHz. (a)Phase current and the CMC (b) CMV (c) Spectrum of CMV

Fig 15 (a) shows the common mode current and a phase from three phase currents. It is almost around 0.185 Amps of RMS value. Fig 15 (b) shows common mode voltage which is around 8.444 Volts of RMS value. The spectrum of common mode voltage which is also known as FFT analysis is shown in Fig 15 (c).

SIMULATION RESULTS OF NSPWM METHOD WITH STRAY CAPACITANCE 1nf:

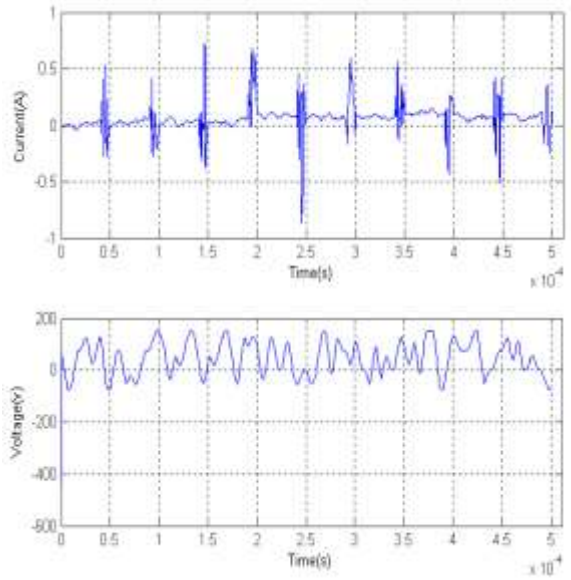


Fig 16 (a): CMC (top: 2 A/div, 50 μs/div) and CMV (bottom: 200 V/div, 50 μs/div) of NSPWM at 15 kHz with different *C*stray. (a) *C*stray = 1nF.

As stated NSPWM is the best available PWM technique in this project, we have studied its performance for various stray capacitance values. For 1 nF we observe that as stray capacitance acts as a filter, more ripples can be noticed. And by using MLI the ripple values reduce more considerably.

SIMULATION RESULTS OF NSPWM METHOD WITH STRAY CAPACITANCE 100nF

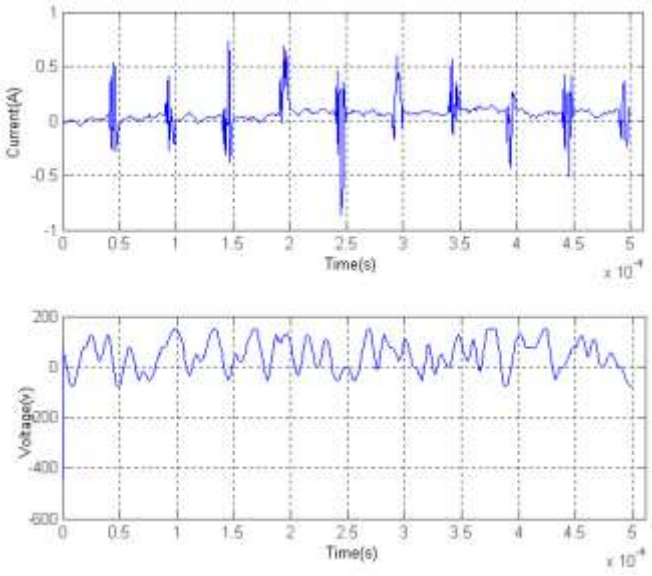


Fig 16 (b): CMC (top: 2 A/div, 50 μs/div) and CMV (bottom: 200 V/div, 50 μs/div) of NSPWM at 15 kHz with different *C*stray. *C*stray = 100 nF

Similarly, for greater values of stray capacitance like 100nF, we can notice that the ripples are considerably reduced and we get a smoother waveform.

Table 1: Comparison of CMV's, CMC's, and THD's of all PWM Methods

	SVPWM	AZPWM	DPWM	NSPWM
Carrier freq (HZ)	10k	10k	15k	15k
CMC (A, RMS)	1.475	0.385	0.2475	0.185
Phase current (A,RMS)	3.4	3.0	2.8	3.0
Phase current THD (%)	2.9	2.3	2.06	2.03
CMV (Volts)	15.93	11.52	17.12	8.444

By studying the above table NSPWM Method yields the best performance in every aspect. The test bench parameters are given in the following table.

Table 2: Test Bench Parameters

AC Utility	220 Vrms (line-line), 60 HZ
AC Side Inductor	Lsa=Lsb=Lsc=5mH
DC Bus Voltage	υDC=370V
DC Bus Capacitor	1000 F
Load	1kW
Stray Capacitance	C_{stray}=0.1µF

V. CONCLUSION

This paper presents a survey of common-mode reduction PWM techniques suitable for grid-connected PV converters. Since the conversion efficiency is the critical factor for grid connected PV systems, transformer less dc/ac converter systems are often favoured. The CMC becomes an even more pronounced issue due to the lack of galvanic isolation. Among all the common-mode reduction PWM techniques, this paper selects AZSPWM1 and NSPWM based on their outstanding performances, in terms of ripples at the ac side (HDF) and at ac side (K_{DC}), especially at high modulation index range. They are tested alongside their "conventional" PWM counterpart, SVPWM and DPWM1, respectively. The outcomes show that by nullifying the zero vector states, AZSPWM1 and NSPWM exhibit superior performance in reducing the CMC. Under the constraint of the same number of switchings per unit time, NSPWM can operate with a carrier wave frequency1.5 times higher than what AZSPWM1 operates with. This explains why NSPWM has the best performance among the examined modulation techniques. The usage of 3-phase, 3-level Neutral Point Clamped Multi Level Inverter also helps in the reduction of CMV, CMC, harmonics.

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