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Novel Low Power Half-Subtractor Using AVL Technique Based On 0.18µm CMOS Technology

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Abstract: ***Now a day's arithmetic circuit plays an important role in designing of any VLSI system. Such as subtractor is one of them. In this paper, half-subtractor is designed by using the adaptive voltage technique (AVL). By using the AVL technique, half subtractor can reduce the power and delay element. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is raised and AVLS (adaptive voltage level at supply) in which the supply potential is increased. The AVL technique shows the significant reduction in power consumption and propagation delay. The circuit is simulated on cadence tool in 180 nanometre CMOS technology.***

Keywords: AVL Technique, VLSI, Low Power, Half-subtractor.

I. INTRODUCTION

The simplest combinational circuit which performs the arithmetic subtraction of two binary digits is called half-Subtracted. The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow). The logic symbol and logic diagram, truth table are shown below.

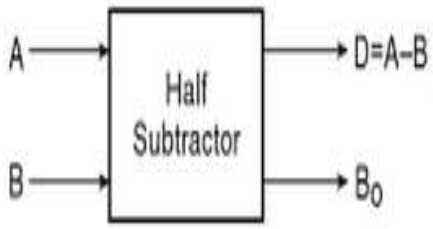

Figure 1.1 logic symbol of half-subtractor

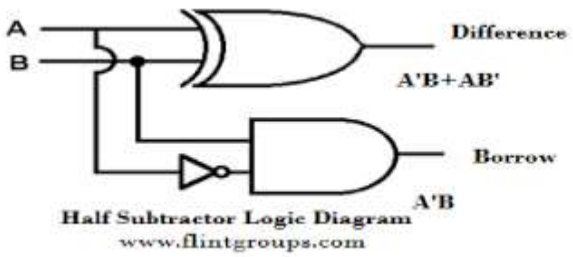

Figure 1.2 logic diagram of half subtractor

Table 1 Truth table of half subtractor

Half Subtractor-Truth Table			
Input		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure 1.2 shows the logic diagram of half-subtractor from table
1.1 logic expression for Difference output and Borrow output can be written in equation 1shown below,

$$Diff = A \oplus B$$
$$Barr = \overline{A}B \qquad (1)$$

II. LITERATURE SURVEY

Leakage reduction technique as high leakage currents in deep submicron regimes is becoming a major contributor to the total power dissipation of CMOS circuits [1]. An adaptive voltage level (AVL) technique can be used to control circuits and it can be used to reduce the heating, the power consumption has to be reduced and this can be achieved by either of the two schemes. One is AVLS (Adaptive Voltage Level at Supply) in which the supply voltage is reduced and the other one is AVLG (Adaptive Voltage Level at Ground) in which the ground potential is increased Leakage current also place a vital role in designing of any system [2-3]. High leakage currents in deep submicron regimes are becoming a major contributor to the total power dissipation of CMOS circuits as the threshold voltage, channel length and gate oxide thickness are scaled. This provides the motivation to explore the design of low leakage SRAM cells. A very small leakage current is flowing in designing using AVLS technique [4].The power consumption of the electronic devices can be reduced by adopting different design styles. The adiabatic logic style is said to be an attractive solution for such low power electronic applications.

Also, power dissipation is very less here [5]. In Deep-Sub-Micron (DSM) technology, it is coming as challenges, e.g., leakage power, performance, data retention, and stability issues. In this work, we have proposed a novel low-stress SRAM cell, called as IP3 SRAM bit-cell, as an integrated cell. It has a separate write sub-cell and read sub-cell, where the write sub-cell has the dual role of data write and data hold. The data read sub-cell is proposed as a PMOS gated ground scheme to further reduce the read power by lowering the gate and sub-threshold leakage currents. The drowsy voltage is applied to the cell when the memory is in the standby mode [6]. Scaling of supply voltage and technology in microprocessors to achieve low power and high performance. The functionality of special circuits in the presence of high leakage, SRAM cell stability, bit line delay scaling, and power consumption in clocks & interconnects, will be the primary design challenges in the future. Soft error rate control and power delivery pose additional challenges [7].

III. PROPOSED SYSTEM

Arithmetic circuits play a vital role in designing of any VLSI system. Subtractor is one of them. In this paper, Half-Subtractor is being designed using Adaptive Voltage Level (AVL) techniques. This design consumed less power as compared to a conventional design. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is raised and AVLS (adaptive voltage level at supply) in which supply potential is increased. The design is much useful in designing the system that consumed less power.

In conventional Half- Subtractor, a simple transistor level circuit is designed. Where all NMOS are connected to the ground terminal and all P-MOS are connected to Source terminal. The circuit is designed using CMOS and the whole circuit consists of 6 transistors. In which 3 NMOS transistors and 3 P-MOS transistors are employed. Leakages current also places a vital role in designing of any system. It should be as low as possible. Power consumption is also an important parameter in system design.

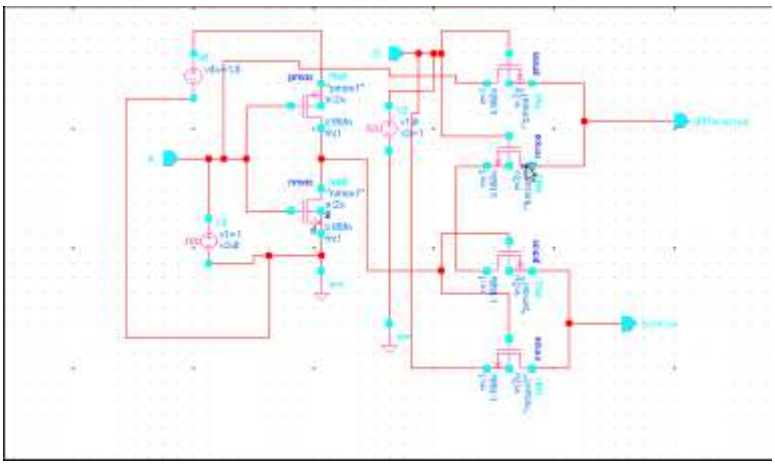

Figure 1.3 Circuit of conventional half-subtractor

An adaptive voltage level technique can be used to control circuits and it can be used either at the upper end of the cell to bring down the supply voltage value, called AVLS scheme or at the lower end of the cell to lift the potential of the ground node, called AVLG scheme. By this technique reduction of power, dissipation occurs. The power dissipation is reduced less than conventional design cell.

In AVLG technique a combination of 1-N-MOS & 2-P-MOS is connected in parallel. So that an input clock pulse is applied at the NMOS circuit of AVLG and rest of all P-MOS are connected to ground. This AVLG circuit is connected at the ground terminal of conventional one by removing ground. This ground terminal is connected to the AVLG circuit.

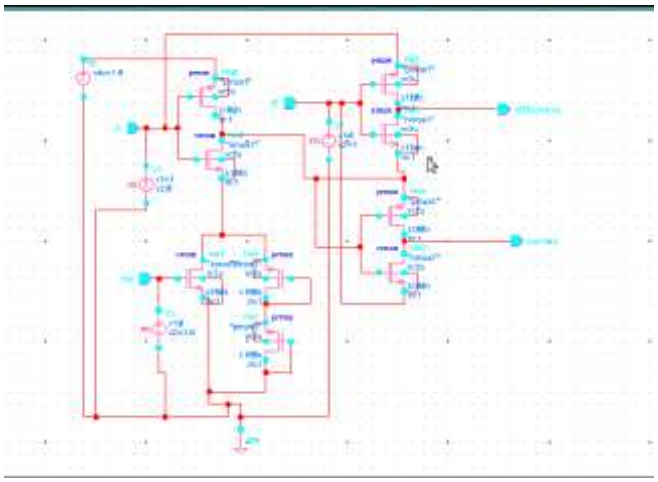

Figure 1.4 Circuit of half-subtractor incorporated with AVLG

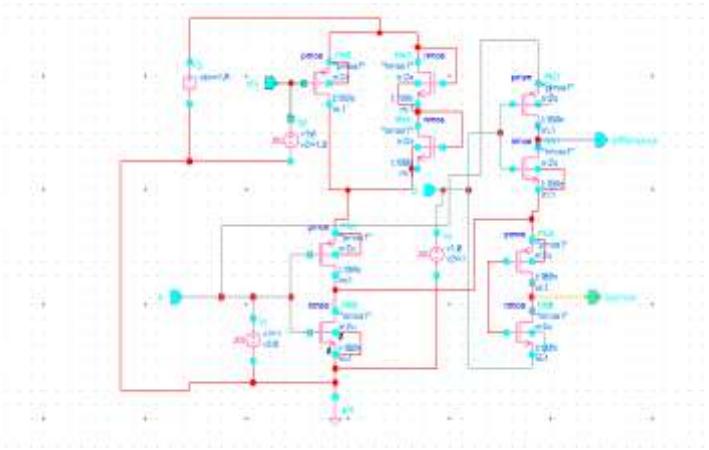

Figure 1.5: Circuit of half-subtractor incorporated with AVLS

In AVLS technique, a combination of 2- N-MOS & 1-P-MOS are connected in parallel. So that an input clock pulse is applied to the P-MOS circuit of AVLS and rest of all N-MOS are connected to drain terminal. This AVLS circuit is connected to the voltage supply source terminal of conventional one by removing voltage supply source. A very small leakage current is flowing in designing using AVLS technique. Also, power dissipation is very less here. By this technique reduction of power, dissipation occurs.

IV. SIMULATION AND RESULT

The simulation result of all the circuit has been placed. Half-subtractor circuit has been implemented. Transient response of the circuit is taken. Transient response is taken due to the analyses the input and output response with power analysis.

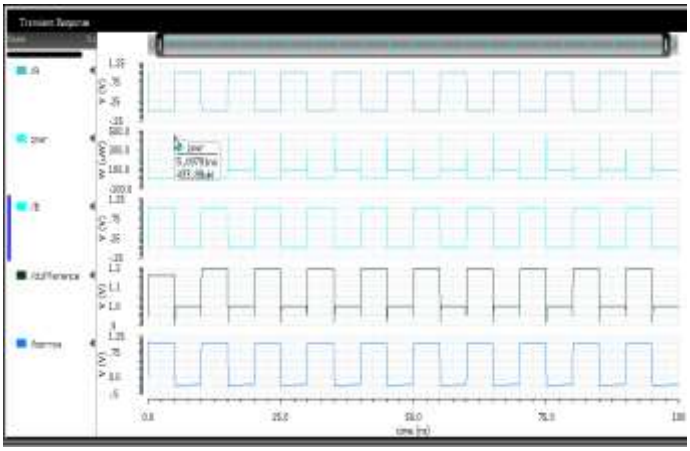

Figure 1.6 Output waveform of conventional half-subtractor

In a conventional half-subtractor circuit which is operated in 1.8v. To implement the half-subtractor circuit the AVLG and AVLS circuits where implemented. The reduction in the power consumption by incorporated with AVL Technique that is either AVLG or AVLS Technique. The half-subtractor is created using the AVL technique and the power analysis is estimated where the power consumption is reduced in AVLS while compared with conventional half-subtractor. On designing AVLS technique based Half-Subtractor using 180 nano meter technologies, we obtain very low power consumption, less propagation delay.

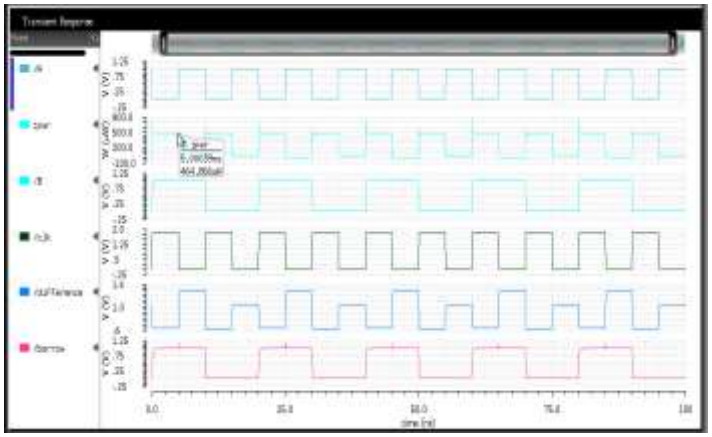

Figure 1.7: Output waveform of half- subtractor incorporated with AVLG

Here the simulation output shows that the power consumption will be reduced lightly when compared with conventional half-subtractor simulation result. Half-subtractor incorporated with AVLS circuit has a power consumption and propagation delay which is less than the half-subtractor incorporated with AVLG circuit.

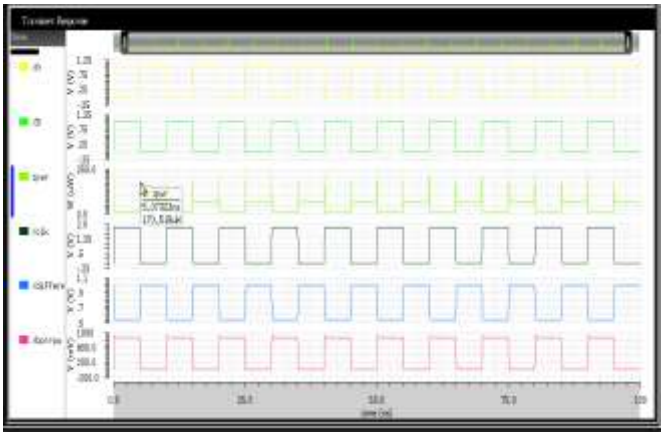

Figure 1.8: Output waveform of half-subtractor incorporated with AVLS

Table 2: Comparison of power and delay

S.No	Circuit	Power reduction	Delay
1	Conventional half sub tractor	433.88µW	5.09 ns
2	Half-subtractor with AVLG	178.86µW	5.07 ns
3	Half-subtractor with AVLS	170.51µW	5.01 ns

The comparison results are shown in the form of graphical view. Here the power consumption is less in AVLS circuit while comparing with other two circuits (ie) AVLG circuit and conventional circuit.

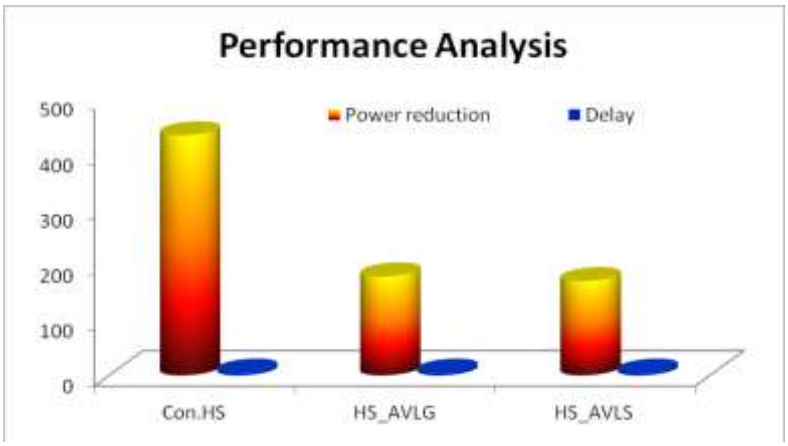

Figure 7: Power and Delay Analysis

The comparison for the conventional half-subtractor and half-subtractor incorporated with AVLG circuit and AVLS circuit using AVL technique are shown in table 2 and the graphical representation of performance analysis shown in figure 7 on both AVLG and AVLS technique.

CONCLUSION

Half-subtractor circuit is implemented using AVL technique. These techniques were employed to reduce the power consumption and propagation delay. The design was implemented in Cadence virtuoso TMSC 180nm CMOS technology and it's obtaining the total power consumption 170.518µW. The entire circuit is operating at 1.8V. Everything has been done in the cadence. This tool it is easy to analysis output of the circuit. For further improvement of power characteristics, new techniques related to the application of half-subtractor can be developed by cadence tool.

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