INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume3, Issue6)
Available online at www.ijariit.com

Implementation of Pull-Up/Pull-Down Network for Energy Optimization in Full Adder Circuit

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Abstract: ***Nowadays the requirements of energy optimized low power circuits in higher-end applications such as communication, IoT, biomedical systems etc., there are several techniques used to implement energy optimization in low power circuits but the static power dissipation need to improve such kind of circuits. The conventional topology has been implemented in basic logical gates but the delay and power much higher in each individual cell. Now we proposed an unbalanced pull-up and pull-down network in full adder circuit using symbols. These techniques were employed to reduce the static power dissipation and switching delay in each individual cell. The design was implemented in Cadence virtuoso TMSC 180nm CMOS technology and it's obtaining the total power dissipation 5.128nW.The pull-up and pull-down network used to reduce the static power dissipation in full adder is used to improve the operating speed of each individual.***

Keywords: CMOS, Logic Gates, Transmission Gates, Pass topology.

I. INTRODUCTION

The energy is reduced while the circuit is operating in the sub-threshold region by using minimum energy point theory [1]. In minimum energy point theory, we determine the optimum supply voltage vdd for threshold voltage. When minimizing the energy, a performance is not a constraint but it shows the dependences of design characteristics and operating condition. The reduced voltages will dramatically worse the device susceptibility in delay and noise margin due to process voltage and temperature variation. By using the device larger than minimum feature size or increasing the supply voltage will compensate the effect of variability [2]. Traditionally a balanced pull-up and pull-down network is preferred in logic cell design. Even though this can be readily achieved by either upsizing the pMOS in the PU network or stacking the nMOS in the PD network [3-4]. A balanced pull-up and pull-down network is achieved using body biasing scheme. Here ultra dynamic voltage scaling is combined with the subthreshold operation so as to operate the circuit under normal vdd at the point of higher throughput [5]. The gate voltage drive of the transistors operating in the sub-threshold domain is small, standard logic cells become more sensitive to process variations; balancing-based sizing method focuses on the statistical distribution of the drain-source current, rather than the current itself [6]. The reverse channel (RSC) effect is used for device optimization by increasing the channel length to have an optimal VT. RSCE behavior where the threshold voltage decreased as the channel length is increased [7]. It will improve the performances and power consumption in subthreshold region. To improve the energy efficiency, the unbalanced PU/PD network, logical effort, and inverse narrow-width (INW) techniques are exploited [8]. The logical effort is an easy way to estimate delay in s CMOS circuit. The method specifies the proper number of logic stages on a path and the best transistor sizes for the logic gates. The method of logical effort is founded on a simple model of the delay through a single MOS logic gate. The delay incurred by a logic gate is comprised of two components; a fixed part called the parasitic delay. The effort delay depends on the load and properties of the logic gate driving the load. The method of logical effort reveals the best number of stages in a multistage network.

The inverse narrow width effect is a reduction in the threshold voltage of a device with decreasing channel width [9]. Circuit noise margin, speed, and required node voltage are an accurate prediction of the threshold voltage. The reduction in the threshold voltage as the width decreases defines the inverse narrow width effect.

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Threshold voltage simulation required a complex multidimensional computer model. Reducing the width of the device increases the threshold voltage; this behavior defines the narrow width effect. The interface charging along both the thin and the field oxide silicon boundary in considered uniform [10].

II. PROPOSED SYSTEM

Logical gates such as AND, OR and EXOR are implemented using the unbalanced pull-up and pull-down network associated with an inverse narrow width technique in pass topology. It reduces the static power dissipation and switching delay in each individual cell. Here the logical gates should be operating in the sub-threshold region because the supply voltage has continually scaled down to the circuit where it reduces the power consumption and switching energy and also it provides high trans conductance gain. By implementing the logical gates using pull-up and pull-down network with inverse narrow width technique, it is one of the power optimization methodologies. Using the narrow width technique the transistor sizing is reduced, within a gate transistor may have a different size to maximize the power saving. Logical gates are implemented using a pass topology, Nmos transistor is an almost perfect switch when passing 0 and thus we say it passing a strong 0. A Pmos transistor again has opposite behavior passing strong 1 but degraded 0. When a Nmos or Pmos has used alone as an imperfect switch it calls as a pass transistor. By combining a Nmos and Pmos transistor in parallel we obtain a switch that turns on when a 1 is applied in which o and 1 are both passed it terms as transmission gate or pass gate. Conventional transistor dimension of a specific logic gate is mainly focused on balancing the driving capability to improve circuit operating speed without much emphasis on the impact of the INW effect it is the technique of circuit optimization. Here with a fixed transistor length L, the threshold voltage is highly dependent on the transistor width W. Static power consumption due to constant current from vdd to gnd in the absence of switching activity. Shrinking transistor geometries causes the different source of leakage current. Subthreshold or weak inversion conduction current between sources and drain in a transistor occurs when the gate voltage is below the threshold voltage. As a consequence, the design margin of the logic cell with higher driving capability is difficult to characterize. To standardizing transistor sizing with increased driving capability to obtain pull-up and pull-down networks propagation delay with respect to the basic logic cell.

Logic gates were implemented using conventional topology and the power analysis is estimated again in logic gates the symbols were created using the conventional transistor. In conventional topology the vpulse and ground are converted as a vss, vdd it assigned as an input for gates to create symbols. By using symbol the gates are analyses where the power is estimated while comparing the conventional gate and symbol based gate the static power is minimized. By implementing these three logic gates we can build a full adder for an application in order to analysis the power estimation. These three gate symbols are used to build the full adder circuit it consists of two xor symbol, two and gate symbol and one or gate symbol.

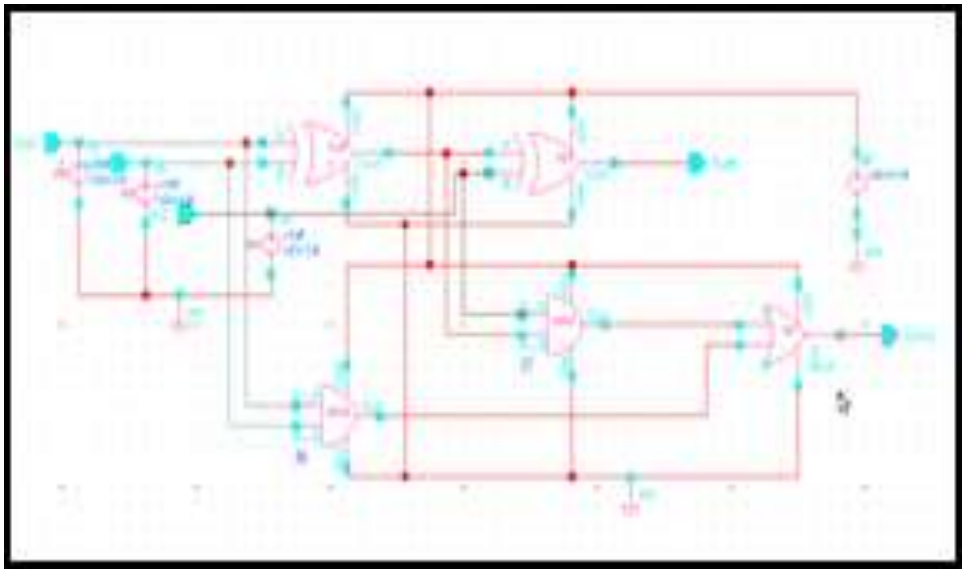

Figure.1 Circuit for Full Adder

A full adder circuit is implemented using the logic gate symbols for the static power reduction in the circuit. When the static power reduction is achieved the energy is utilized to operate the other subcircuit. A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. The full adder circuit is analysed using the pull-up network and pull-down network. The full adder schematic is shown in figure 1. In Figure 2 shows the pull-up network in schematic design and figure 3 shows the pulldown network schematic design. Both technique is used pass transistor topology based pull-up/down network. The utilization of single transistor is reducing the power.

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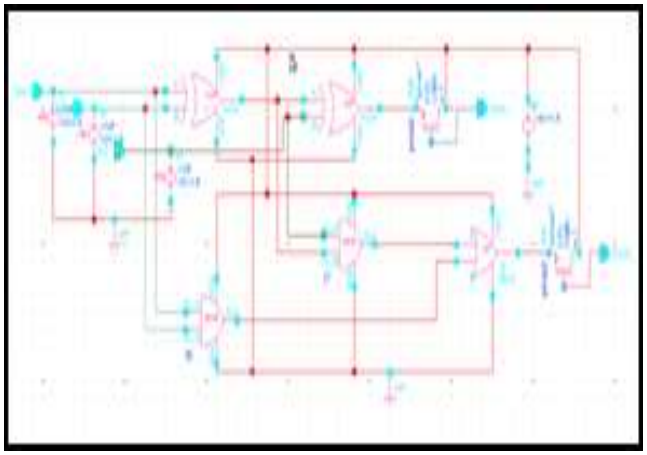

Figure.2 Full adder Using Pullup Network

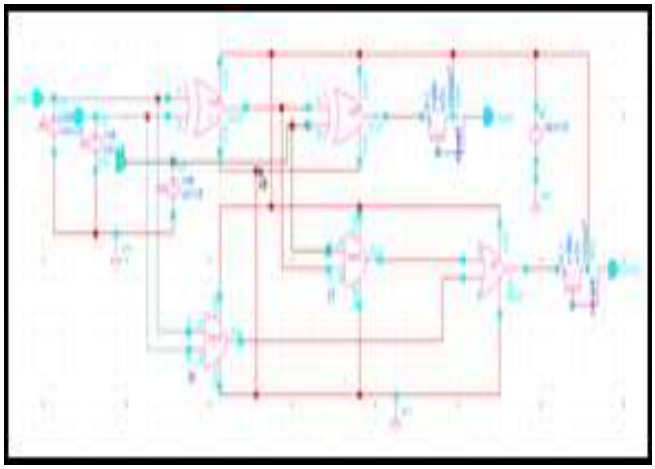

Figure.3 Full adder Using Pulldown Network

III. SIMULATION AND RESULT

The full adder was designed and simulated in Verilog HDL and CMOS design. In figure 4 shows the HDL implementation of 8-bit full adder RTL view and figure 5 contain the circuit utilizing power, area and time in another hand the single bit full adder was implemented in CMOS technique to obtain the transient response and power analysis shown in figure 6. In this analysis, the entire circuit consuming the power has been reduced when compared to HDL design.

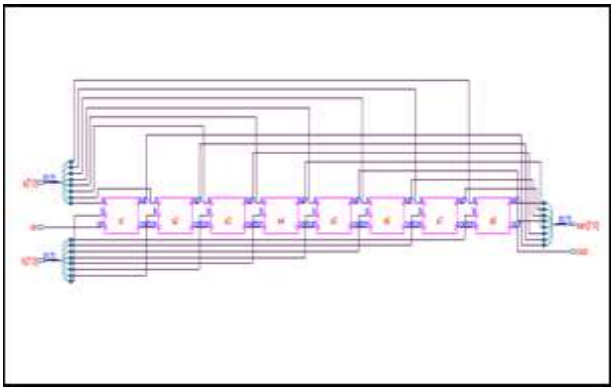

Figure.4 8 Bit Full Adder RTL View

Table.1 RTL Report

Gate	8
Power	6942.391 nW
Time	2057 ps

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In table shows the utilization of gates, power and time in verilog HDL design obtained cadence encounter 90nm. Transient response of the circuit is taken. Transient response is taken due to the analyses the input and output response with power analysis. The output of the full adder is shown in figure 5.

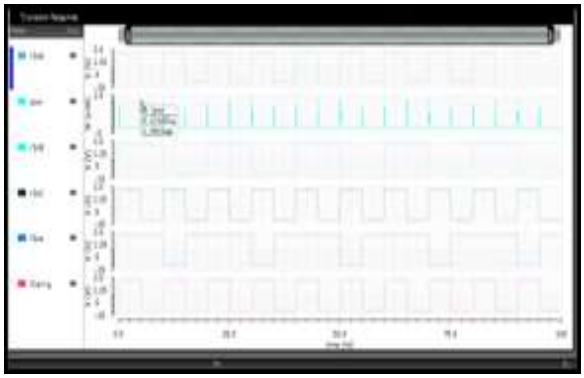

Figure.5 Conventional Full Adder Output

In conventional full adder circuit which is operated in 1.8 v. The power is estimated for the circuit which consists of 5.000nm.This symbol creation is applied in the application as a full adder. The full adder is created using the AND, OR, EXOR symbols and the power analysis is estimated where the static power is reduced in full adder while compared with conventional logic gates. To implement the full adder circuit the AND, OR and EXOR gates where implemented. The pull-up network is added with the adder circuit in order to reduce the static power of the circuit. Here the pull-up network is acted as a high value which utilizes the power leaked by the full adder circuit. Likewise, the pull-down network is added with adder circuit which is low value.

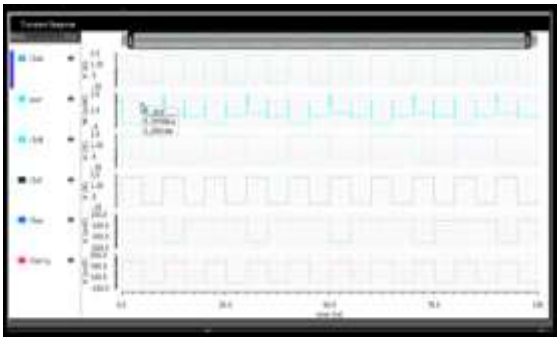

Figure.6 Full Adder Output using Pull-up Network

In this work, we obtain the simulation output shows that the static power will be reduced slightly when compared with conventional full adder simulation result. Pull down network has a static power reduction which is less than the pull-up network of the circuit. The output of full adder with pullup and pulldown network are shown in figure 6 and figure 7.

Figure.7 Full Adder Output Using Pulldown Network

The comparison for the conventional full adder and full adder circuit using pull-up network and pull-down network are shown in table 2.

Table.2 Comparison of Power Analysis

S: no	Circuit	Power reduction
1	Conventional full adder	5.12187
2	Pull up network	5.09128
3	Pull down network	5.09128

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The comparison of the results is shown in the form of graphical view. When the power reduction will be more in full adder circuit while comparing with simple logic gate power estimation which is shown in the graph 1

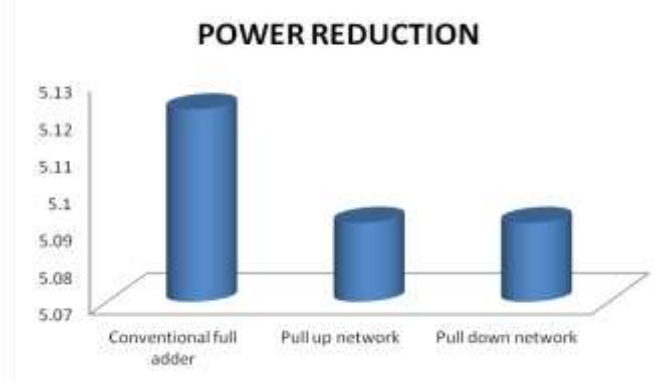

Figure.8 Power Analysis

Now the 8-bit full adder is designed where the power analysis is compared between the one-bit full adder and 8-bit full adder it consists of 5.12187 NW for one-bit adder and 6942.391 nW for the 8-bit adder.

CONCLUSION

A full adder circuit is implemented using symbols with pull-up and pull-down network. These techniques were employed to reduce the static power dissipation and switching delay in each individual cell. The design was implemented in Cadence virtuoso TMSC 180nm CMOS technology and it's obtaining the total power dissipation 5.128nW.The pull-up and pull-down network used to reduce the static power dissipation in full adder is used to improve the operating speed of each individual. The requirements of energy-optimized low power circuits are used in higher-end applications such as communication, IoT, biomedical systems etc., the entire circuit is operating at 1.8V. Everything has been done in the cadence. This tool it is easy to analysis output of the circuit. For further improvement of power characteristics of logic family, new techniques related to the application of ladder can be developed.

REFERENCES

[1] B.H. Calhoun and A.Chandrakasan (2004) "Characterizing and modeling minimum energy operation for subthreshold circuits" in Proc Symp Low Power Electron Design PP: 90-95.

[2] A.Tajalli and Y.Leblebici (2011) "Design trade-offs in ultra-low power digital nanoscale CMOS" IEEE Trans Circuits Syst. Vol No: 58[9] PP: 2189-2200.

[3] N.Reynders and W.Dehaene (2012) "Variation resilient building blocks for ultra-low energy sub-threshold design" IEEE Trans Circuit Syst. Vol No: 59[12] PP:898-902.

[4] M.Alioto (2010) "Understanding Dc behavior of sub threshold CMOS logic through closed-form analysis" IEEE Trans Circuit system. Vol No: 57[7] PP: 1597-1607.

[5] M.E.Hwang, A.Raychowdhury, K.Kim, and K.Roy (2007) "An 85 mV 40nW process- tolerant sub-threshold 8x8 FIR filter in 130nM technology" in Proc IEEE Symp VLSI Circuit. PP:154-155.

[6] B.Liu, J.P.de Gyvez and M.ashouei (2013) "Subthreshold standard cell sizing methodology and library comparison" J.Low Power Electron. Vol No:3[3] PP:233-249.

[7] T.H.Kim, H.Kim, J.Keane and C.Kim (2006) "Utilizing reverse short channel effect for optimal subthreshold circuit design" in Proc Int Symp Low Power Electron. PP:127-130.

[8] F.Frustaci, P. Corsonello and S.Perri (2012) "Analytical delay model considering variability effects in subthreshold domain" IEEE Trans Circuit yet. Vol No:59[3] PP:168-172.

[9] I.S.Sutherland, R.Sproull, and D.Harris (1999) Logical effort: Designing fast CMOS circuits, Son Francisco CA, USA.

[10] L.A.Akers (1986) "The Inverse Narrow Width Effect" IEEE Electron Device Lett, Vol No:7[7] PP:419-421.

[11] J.Zhou, S.Jayapal, B.Busze, L.Huang and J.Stuyl (2012) "A 40nM dual width standard cell library for near/subthreshold operation" IEEE Trans Circuit Syst. Vol No:59[11] PP:2569-2577.

[12] A.Klinefelter, Y.Zhang, B.otis and B.H.Calhoun (2012) "A Programmable 34nW/channel sub-threshold signal band power extractor on a body sensor node SOC" IEEE Trans Circuit System Vol No:59[12] PP:937-941.

[13] J.Kwong and A.P.Chandrakasan (2006) "Variation driven device sizing for minimum energy subthreshold circuits" in Proc Int Symp Low Power Electron Design.PP:8-13.

[14] J.M.Wang, S.C.Fang and W.S.Fang (1994) "New efficient design for XOR and XNOR function in the transistor level" IEEE J.Solid State Circuit. Vol No:29[7] PP:780-786.

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