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Efficient Implementation of Full Adder for Power Analysis in CMOS Technology

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Abstract: In recent days, the real-time application and fast arithmetic operations require highly efficient arithmetic hardware architecture to improve the system performances. The adder plays a vital role in digital circuits, the earlier hardware architecture using conventional CMOS and transmission logic gate based full adder design. Moreover, the techniques using more number of transistors and consume larger power and delay so we proposed the techniques pass-transistor logic and transmission gate based hybrid pass logic. The hybrid technique is used to reduce the number of the transistor, so the delay and power consumption will be reduced when compared with the earlier techniques. The proposed technique design was implemented using 16 transistors in 180nm CMOS technology and it consumes 8.2075nW power and the delay reduced to 5.0146ns.

Keyword: CMOS. Transmission gate, Pass-Transistor Logic, Adder.

I. INTRODUCTION

A full adder is one of the most fundamental building blocks of all the circuit application. Standard static CMOS, dynamic CMOS logic, complementary pass transistor logic (CPL) and transmission gate full adder are the most logic styles in the conventional domain [1]. In general, one bit full adder core has three inputs (A, B and carry in Ci) and two outputs (sum S and carry out Co).The adder performance may improve the power and speed with driving capability. The performance of full adder can significantly affect the system performance [2]. At the circuit level, the optimized design is used to avoid degradation in the output voltage, and it consumes less power and delay in the critical path [5]. Using the complementary pass transistor logic (CPL) the adder circuit will operate at low supply voltage with signal integrity [6]. From the gate logic design, the full adder can be implemented using exclusive-OR gates, since the sum can be expressed as an XOR function and output can be expressed as a multiplexer function [7].

The power dissipation characteristics are compared qualitatively and quantitatively with gate implementation. Lowering supply voltage also increases the circuit delay and degrades the drivability of the cells [8]. Clustered voltage scaling (CVS) and Dual voltage supply (dual-VS) have been proposed to maintain the chip throughput by selectively lowering the supply voltage.The critical path traverses from the carry-in to the carry-out of the full adders. To optimize and analyze the performance of different full adders, a tree-structured setup is proposed. Each of these modules is implemented, optimized and tested separately [6]. Several full-adder cells are composed by connecting these modules. Adders are an extensively used component in data paths and the design and analysis are required for these units to obtain optimum performance.

To execute an arithmetic operation a circuit can consume very low power by clocking at low frequency to complete the operation.GDI techniques are used to reduce power consumption, propagation delay [9]-[14]. The major sources of power consumption in CMOS circuits are switching power, short circuit power and leakage power [15]. The performance and complexity at the transistor level directly influence the overall performance of the system. The gate-based Full adders with conventional methods result in a higher number of transistors and consequently more power consumption, delay, and area wastage [17] –[19]. Lowering the supply voltage appears to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles [20]-[23]. The power-delay product (PDP) represents a tradeoff to be optimized between two conflicting criteria of power dissipation and circuit latency. In VLSI the adders are basic components for an ALU. There is N number of adders their own advantage and disadvantages.

When two numbers are to be added and if each of them is of N bits than we can add in two ways they are serial and parallel. In serial addition, the LSBs are added first then the carry created are propagated to the next higher bits. In parallel addition, it added in parallel without waiting for carrying and different algorithms are used to compensate for the carry.

In CMOS the adders are classified based on the propagation of carry between the stages they are Ripple Carry Adder (RCA), Carry Skip Adder (CSKA), Carry Increment Adder (CIA), Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSLA) and Carry Bypass Adder (CBA). RCA contains the series structure of Full Adders each full adder is used to add two bits along with carrying bit. The carry generated from each full adder is given to next full adder and the delay is more as the number of bits is increased. CSA uses skip logic in the propagation of carrying. It is used to speed up the operation by adding a propagation of carrying bit around a portion of the entire adder.

Carry increment adder (CIA) consists of ripple carry adder and incremental circuitry. The addition operation is done by dividing a total number of bits into a group of 4- bits and addition operation is done using several 4-bit ripples carry adder. Carry look Ahead (CLA) is based on the principle of looking at lower adder bits of argument and added if higher orders carry generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal propagates. Carry save adder (CSA) three bits are added parallel, in this carry is not propagated to the stages. The delay due to the carrier is reduced. Carry select adder (CSLA) architecture consists of the independent generation of sum and carry i.e., cin=1 and cout=0 are executed parallel. Carry Bypass adder (CBA), ripple carry adder is used to add 4-bits at a time and the carry generated will be propagated to next stage.

II. PROPOSED SYSTEM

The simulation of the proposed full adder was carried out using 180 nm technologies and compared with the other adder techniques like conventional CMOS (C-CMOS), Transmission gate adder (TGA), Transmission full adder (TFA) and 10T transistor design. The proposed techniques consist of pass transistor logic and transmission gate based hybrid pass logic. The pass transistor logic is driven by periodic signal and it reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages and this reduces the number of active devices. The power consumption is minimized mainly by sizing the transistors in inverter circuits while the carry propagation delay will be improved by sizing the transistor between the paths from cin to court. The power consumption may be classified into static and dynamic power. The static power is mainly due to biasing, leakage currents and sub-threshold conduction. To minimize the static power the inverters should have a large channel width. The difference in static and dynamic power consumption is large because of increases in subthreshold conduction current and the leakage.

The proposed hybrid adder requires only 16 transistors whereas the other hybrid technique requires more than 16 transistors. The average power consumed by the proposed full adder is significantly lower than that of the other hybrid full adders. Figure 2 shows the detail diagram of the proposed full adder. The sum output of the full adder is implemented XNOR modules. The inverter comprised of pmos and nmos transistors which generate the input B. Output of the controlled inverter is basically the XNOR of A and B. The performances analysis of proposed full adder was performed with 1.8v supply voltage with 180nm technology. The uses of less number of transistors in proposed full adder also improve the speed. The table1 represents a detailed comparison of the proposed full adder with other hybrid full adders in 180nm technology which is discussed below.

Table1: Simulation result for full adders in 180 nm technology

Design	**Avg. Power(nw)**	**Delay (ns)**	**Transistor count**
C-CMOS	22.473	28.14	28
TGA	8.3741	5.0595	20
TFA	24.504	9.7605	16
10T	24.44	4.75496	10
Proposed	8.2075	5.0146	16

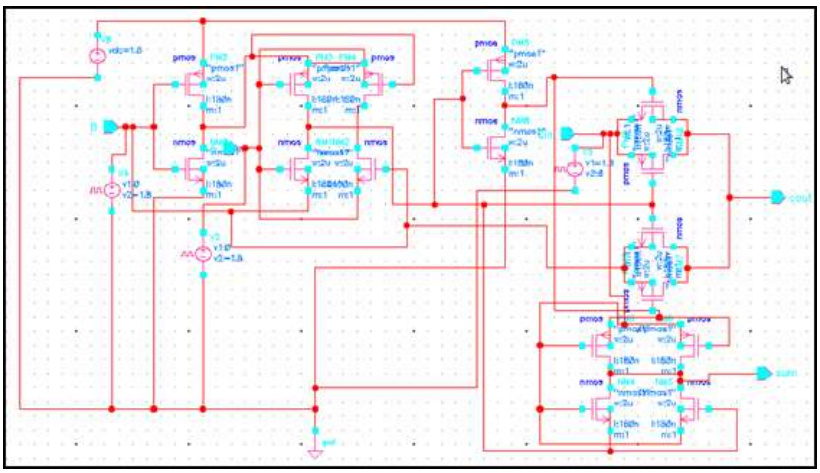

Figure1: Circuit for proposed full adder

III. SIMULATION AND RESULT

The analysis which includes different circuits like C-CMOS, TGA, TFA, 10T and proposed adder has been based on simulation runs on cadence using 180nm technology. By optimizing the number of the transistor of a full adder, it is possible to reduce the delay of all adders without increasing the power consumption. Buffers are attached to TFA, TGA and 10T circuits to enhance driving capability. Figure 2 represents the output of proposed full adder circuit in which the delay and power will be calculated.

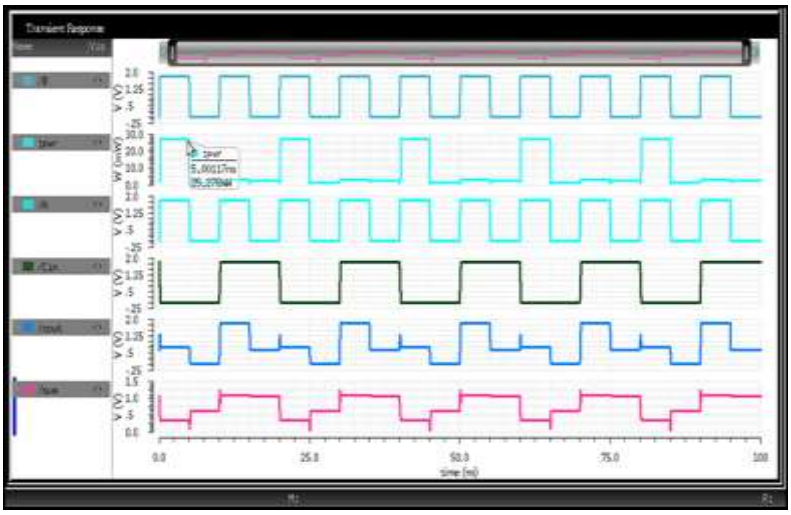

Figure 2: Output of proposed full adder

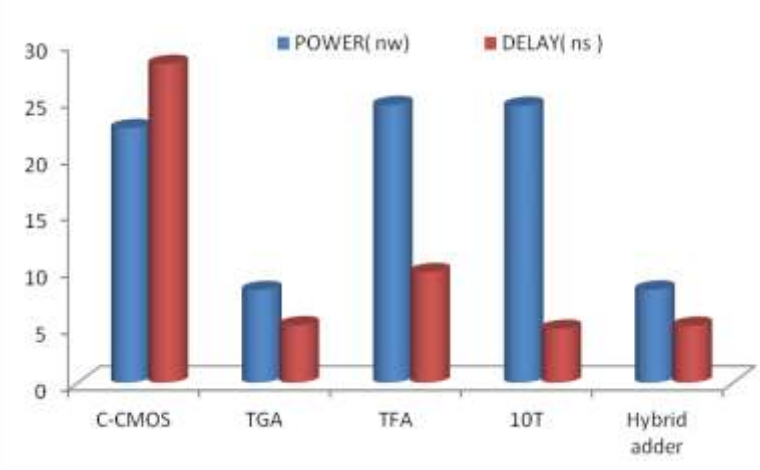

Figure 3. Comparison of delay and power

The performance of the proposed full adder in terms of average power and delay with supply voltage and comparison with other existing design is shown in above figure 3.

CONCLUSION

In this paper, we proposed a low power hybrid 1-bit full adder in CMOS design. The simulation was carried out using cadence virtuoso tool 180 nm technologies and compared with other designs like C-CMOS, TFA, TGA, and 10T. The simulation result offered that the established proposed adder reduces the power compared with earlier designs. The hybrid technique is used to reduce the no of the transistor, so the delay and power consumption will be reduced when compared with the earlier techniques. The proposed technique design was implemented using 16 transistors in 180nm CMOS technology and it consumes 8.2075nW power and the delay reduced to 5.0146ns.

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