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Power Quality Improvement by Diode Clamped Multilevel Inverter

Rahul Kumar Sahu
Department of Electrical & Electronics Engineering
Bhopal Institute of Technology, Bhopal
sahurahul636@gmail.com

Dr. V. K Jain
Department of Electrical & Electronics Engineering
Bhopal Institute of Technology, Bhopal
principalbit@gmail.com

Vinay Pathak
Department of Electrical & Electronics Engineering
Bhopal Institute of Technology, Bhopal
hodbit@gmail.com

Ankush Yadav
Department of Electrical & Electronics Engineering
Oriental University
ankushvac@gmail.com

Abstract: ***The solution of power quality problem employ improved performance converters. Pulse width modulation converter has become an integral part of these improved performance converters, require high voltage, high-frequency switching devices. Recently multilevel inverters are being emerged as a viable solution of the conventional 2-level inverter for medium and high voltage applications with improved power quality. In this Paper a single phase five level diode clamped inverter is designed, developed and investigated for improve voltage quality in terms of harmonic distortion with reducing switching losses.***

Keywords: Power Quality.

INTRODUCTION

The multilevel inverter includes an array of power semiconductor devices and capacitors voltage sources, the output of which generates voltages with stepped waveforms. The computation of the switches permits the addition of the capacitors voltages to obtain high-voltage at the output, while the power semiconductors have to withstand only reduced voltages. We can observe a two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor. While three and level inverter generates three voltages, and a nine-level inverter generates a nine-level output voltages. In all these cases devices are not arranged in series but they are arranged in such way that, they gain the capability to generate such kind of voltages. Herein, we should remember one important thing i.e. as the number of steps increases in the output waveforms; harmonic content comes down. Thus power quality of such waveforms will increase drastically. However, in order to generate step kind of waveforms in the output side, different Multilevel based archetypes are successfully built and verified. But the general principle of multilevel inverters is the synthesis of the AC voltage from several different voltage levels on the DC bus. As the number of voltage levels on the input DC side increases, the output voltage adds more steps which approach the sinusoidal wave research work.

Diode Clamped Multilevel Inverter (DCMLI)

Values of various parameters used in this model are given in Fig. 1 shows a schematic diagram of Basic Diode Clamped Multilevel Inverter. In a 3-level DCMLI total of 8 IGBTs, 7 clamping diodes, and 4 V_{cc} supply. The DC voltage source may be a battery or rectified voltage through uncontrolled/controlled bridge rectifier known as passive/active front end converter, respectively. To obtain $+V_{dc/2}$ voltage at inverter pole.

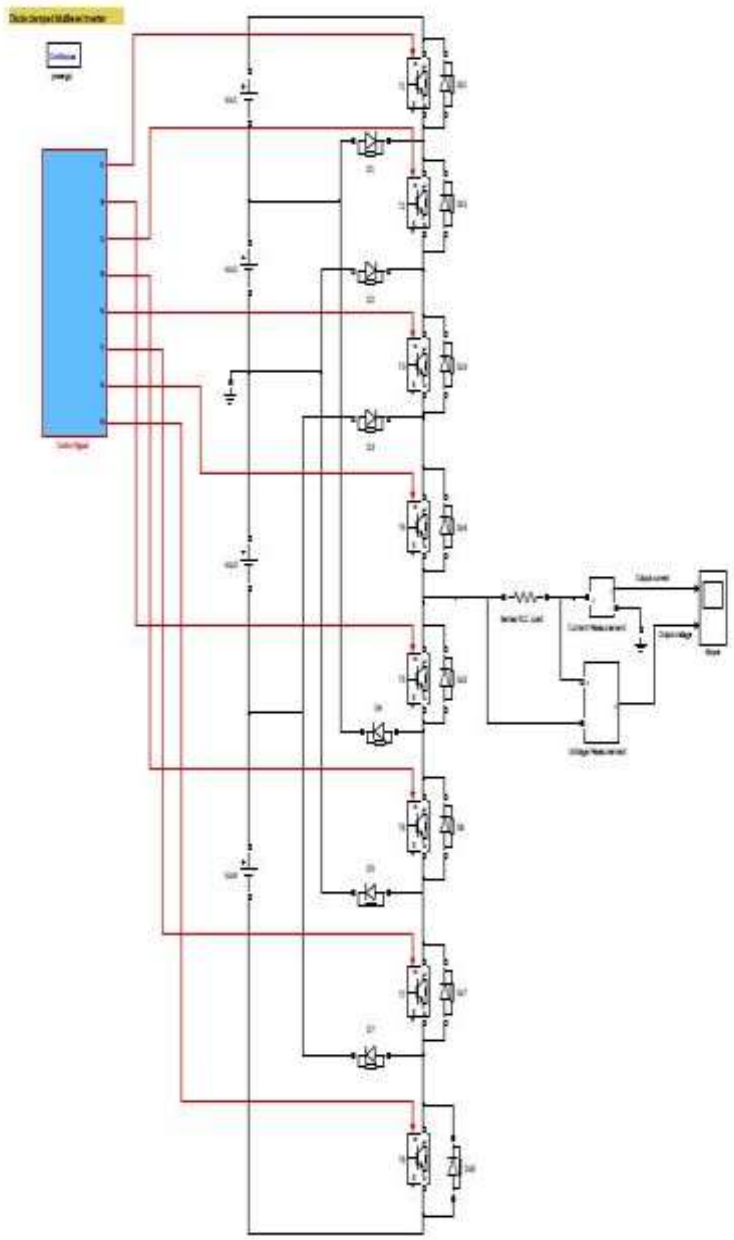

Figure 1 Diode Clamped Multilevel Inverter

SIMULATION RESULT AND ANALYSIS

The proposed converter synthesizes a single-phase multilevel waveform from the calculated switching angles. The converter thus generates the variable-amplitude, variable frequency voltage waveforms to DC. The MATLAB-Simulink is used to simulate 3 and 5-level Diode Clamped Multilevel Inverter. In this research area, we are investigating the nine different modulation schemes of Diode Clamped Multilevel Inverter. We are analysing the difference of THD in all the schemes of line voltage and phase voltage and clearly shown in table 2.1 and 2.2.

The first experimentation is carried out to investigate the performance of three-phase, five-level diode-clamped multilevel inverter SPWM control validates the simulation results with Sinusoidal PWM schemes. Further, the inverter is tested with PD SPWM,

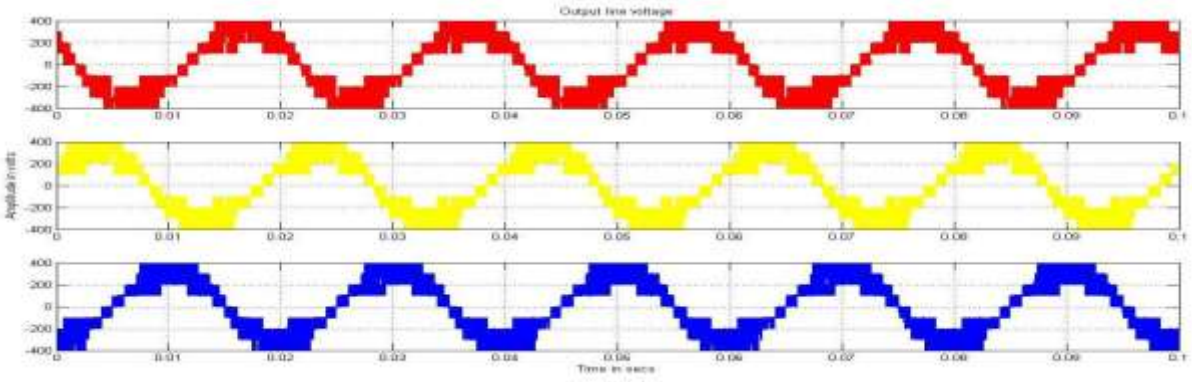

Figure2.1Line voltages of the proposed three-phase inverter

VAPD SPWM, POD SPWM, VAPOD SPWM, APOD SPWM, VAAPOD SPWM, VF SPWM, CO SPWM – A, CO SPWM – B and their modified forms with the addition of off-set signal. It indicates the unequal voltage stresses on the devices in the same phase leg of the inverter. Inverter line voltages with PD SPWM scheme, POD SPWM scheme, PD with off-set signal and POD SPWM with off-set signal technique. The frequency spectrum of line voltage $V_{ab}$with these different SPWM schemes is discussed in the last chapter. The lowest harmonic distortion is 16.97%. Line voltage contains increased magnitude of harmonics around the switching frequency and THD contents are 20.08 % in POD SPWM and POD SPWM with off-set signal respectively.

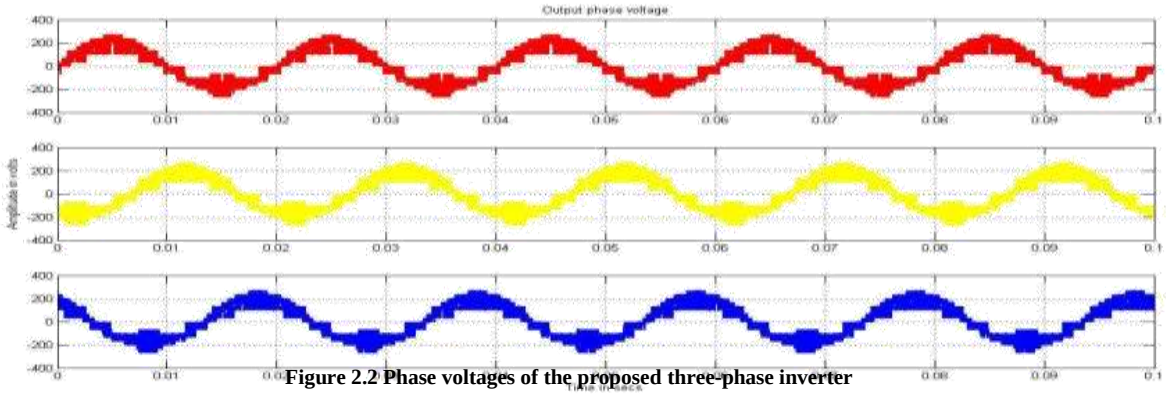

Figure 2.2 Phase voltages of the proposed three-phase inverter

Table 2.1 Fundamental Frequency and %THD of line voltage

Different Modulation schemes	Fundamental frequency – line Voltage	Total harmonic distortion (THD) - line voltage
DPWM	348.1	16.95
VAPDPWM	377.0	17.39
PODPWM	377.0	20.16
VAPODPWM	367.1	20.15
APODPWM	346.9	25.15
VAAPODPWM	376.9	21.23
VFPWM	346.8	18.78
COPWM-A	364.1	21.21
COPWM-B	364.1	23.87

Table 2.1 and 2.2 compare the performance of DCMLI with different SPWM schemes on no-load and on-load conditions on the basis of %THD, amount of DC link unbalance and fundamental voltage output. The THD content in inverter voltage in minimum

in PD SPWM investigation in chapter 4. This schemes also gives minimum DC link unbalance without using any controller. It is clear that phase voltage contains 3rd order harmonic due to the inherent problem of capacitor voltage unbalancing. These results confirm the correctness of the developed inverter and its controller experimentally. The best techniques in my research work are PDPWM which has been providing minimum harmonics 16.95% and APOPWM techniques have maximum 25.15% harmonics.

The valuable data of bar frequency we are showing here FFT calculation and we getting to compare maximum harmonics in all that schemes order with sinusoidal waveform and her frequency analysis tool and maximum harmonic of 81 i.e. 9.06% and value of frequency is 4050 Hz.

Table 2.2 Fundamental Frequency and %THD of phase voltage

Different Modulation schemes	Fundamental frequency- phase Voltage	Total harmonic distortion (THD) - phase voltage
DPWM	201.3	16.97
VAPDPWM	217.7	17.42
PODPWM	217.7	20.08
VAPODPWM	216.1	20.04
APODPWM	200.3	25.13
VAAPODPWM	217.7	21.09
s VFPWM	200.3	18.76
COPWM-A	210.3	21.21
COPWM-B	210.4	23.80

CONCLUSION

Recent development in this technology enables to achieve high efficiency, energy savings, improved performance, and compactness in almost all domestic, commercial, industrial and utility based applications. The solution of this power quality problem again employs improved performance converters. Pulse width modulation converter has become an integral part of these improved performance converters, require high voltage, high-frequency switching devices. Recently multilevel inverters are being emerged as a viable solution of the conventional 2-level inverter for medium and high voltage applications with improved power quality. In this dissertation, a single phase five level diode clamped inverter is designed, developed and investigated for improve voltage quality in terms of harmonic distortion with reducing switching losses. An exhaustive literature survey is carried out on the different multilevel inverter to review the state of art of multilevel inverter technologies based on topologies, modulation schemes, and application techniques. A three-level diode clamped inverter is then investigated through simulation using different multilevel modulation schemes such as sinusoidal pulse width modulation (SPWM). An improved performance of the inverter is obtained with SPWM and their modified forms

(PD SPWM, VAPD SPWM, POD SPWM, VAPOD SPWM, APOD SPWM, VAAPOD SPWM, VF SPWM, CO SPWM – A, CO SPWM –B) in terms of load side power quality

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