Reduction of VR using Pi and FLC in a buck-boost converter by SR buck – KY boost converter

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Abstract: In this paper, an analyze and describe step by step process of designing, feedback control and MATLAB simulation of a voltage bucking-boosting converter by combining KY and Synchronous Buck converter for power battery applications. Unlike the traditional buck–boost converter [1, 2, 10, 11], this converter has only the positive output voltage, different from the negative output voltage of the traditional inverting buck–boost converter. This converter operates only in continuous conduction mode. The output current is the non-pulsating waveform thereby not only the current stress on the output capacitor is reduced but also reducing the output voltage ripples. By Combining the KY converter with the synchronous buck converter, a positive buck–boost converter is obtained and uses the same power switches with no right-half-plane zero. So that the circuit is made to be compact and the corresponding cost to below.

Keywords: KY converter, Output Voltage Ripples, Voltage Conversion Ratios, Right-Half Plane Zero, and Synchronously Rectified (SR) buck Converter.

I   INTRODUCTION

Nowadays the use of low voltage portable devices and growing requirements of functionalities embedded into such devices is increased. Thus, the techniques of efficient power management are needed for longer battery life for them. A buck-boost switching converter is most efficiently generated because it gives the highly variable nature of batteries systems often require supply voltages to be both higher and lower than the battery. But here the converter efficiency is decreased since the power loss occurs in the storage devices. Over the years the portable electronics industry progressed widely. A lot requirement evolved such as increased battery life, small and cheap systems, coloured increased battery life, small and cheap systems, colored phones. The introduction of the new field has offered challenges owing to the unique combination of three major fields of electrical engineering: electronics, power, and control.

DC-DC converters are the devices that are used to convert and control the DC electrical power efficiently and effectively from one voltage level to another. The DC-DC converter is a device for converting one DC voltage level to another DC voltage level with a minimal loss of energy.

Here the KY Converter [5-8] recently invented by K. I. Hwu and Y. U. Yau operates in Continuous Conduction mode with non-pulsating output current across the output capacitor results in low output voltage ripples. Several types of non-isolated voltage-bucking/boosting converters such as buck-boost converter, Cuk converter, SEPIC converter, Zeta converter, etc., operating in continuous conduction mode (CCM) and possess right–half plane, thereby causing the system stability to be low, load transient responses to be slow about several milliseconds and hence corresponding design for accelerating transient responses to be difficult [12]. These problems can be rectified by the KY –buck Converters. Generally, for the reduction of the ripple content the techniques preferred are Equivalent Series Resistant (ESR) capacitor [7] or by adding an inductance-capacitance (LC) filter [8] in KY Converter.

Furthermore, since the proposed converter comes from the KY converter, the detailed comparisons between the proposed buck–boost converter and the KY converter are described as follows.

1) Both converters always operate in CCM. That is, the negative current can be allowed at light load, but the corresponding average current must be positive.

2) Both converters have individual output inductors, thereby causing the output currents to be pulsating.

3) The proposed converter has one additional inductor and one additional capacitor so as to execute voltage bucking/ boosting as compared with the KY converter. Therefore, the proposed converter has the voltage conversion ratio of 2D, and hence possesses voltage bucking with the duty cycle locating between 0 and 0.5 and voltage boosting with the duty cycle locating between 0.5 and 1. On the other hand, the KY converter has the voltage conversion ratio of 1 + D, and hence only possesses voltage boosting with the duty cycle locating between 0 and 1. In addition, the maximum voltage conversion ratios for both are identical, equal to 2.

4) Both these converters can operate bidirectionally. The proposed converter works with the backward voltage conversion ratio of $0.5/(1-D)$, whereas the KY converter works with the backward voltage conversion ratio of $1/(2-D)$.

II A PROPOSED BUCK BOOST CONVERTER COMBINING KY AND BUCK CONVERTERS
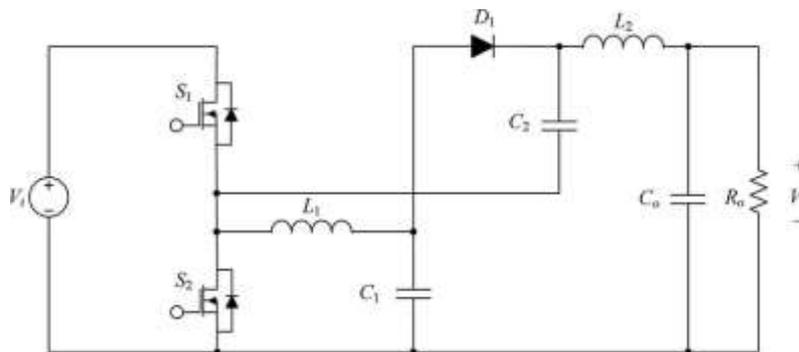

Fig. 1. A KY Buck–boost converter.

Fig. 1 shows a novel buck–boost converter, which combines two converters using the same power switches. One is the SR buck converter, which is built up by two power switches S1 and S2 , one inductor $L1$, one energy-transferring capacitor $C1$,

whereas the other is the KY converter, which is constructed by two power switches S1 and S2 , one power diode D1 which is disconnected from the input voltage source and connected to the output of the SR buck converter, one energy-transferring capacitor $C2$, one output inductor $L2$, and one output capacitor Co. The output load is signified by Ro . Furthermore, during the magnetization period, the input voltage of the KY converter comes from the input voltage source, whereas during the demagnetization period, the input voltage of the KY converter comes from the output voltage of the SR buck converter. In addition, during the startup period with S1 being ON and S2 being OFF, $L1$ and $L2$ are both magnetized. At the same time, $C1$ is charged, and hence, the voltage across $C1$ is positive, whereas $C2$ is reverse charged, and hence, the voltage across $C2$ is negative. Sequentially, during the startup period with S1being OFF and S2 being ON, $L1$ and $L2$ are both demagnetized. At the same time, $C1$ is discharged. Since $C2$ is connected in parallel with $C1$, $C2$ is reverse charged with the voltage across $C2$ being from negative to positive, and finally, the voltage across $C2$ is the same as the voltage across $C1$.

III BASIC OPERATING PRINCIPLE

There are some assumptions and symbols that are given as follows: 1) All the components are ideal; 2) the blanking times between S_1 and S_2 are omitted;3) the voltage drops across the switches and diode during the turn-on period are negligible; 4) the values of C_1 and C_2 are large enough to keep V_{C1} and V_{C2} almost constant, that is, variations in V_{C1} and V_{C1} are quite small during the charging and discharging period; 5) the dc input voltage is signified by V_i , the dc output voltage is represented by V_o , the dc output current is expressed by I_o , the gate driving signals for S_1 and S_2 are indicated by M_1 and M_2, respectively, the voltages on S_1 and S_2 are represented by v_{S1} and v_{S2} , respectively, the voltages on L_1 and L_2 are denoted by v_{L1} and v_{L2}, respectively, the currents in L_1 and L_2 are signified by i_{L1} and i_{L2} , respectively and 6) the currents flowing through L_1 and L_2 are both positive.

This converter always operates in CCM inherently, the turn-on type is $(D, 1-D)$, where D is the duty cycle of the gate driving signal for S_1 and $1-D$ is the duty cycle of the gate driving signal for S_2.
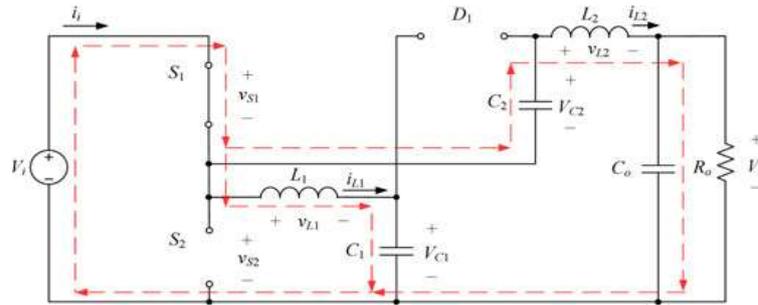
Fig. 2. Current flow in state 1.

There are two operating states to be described.

State 1: As shown in Fig. 2, S1 is turned ON but S2 is turned OFF. During this state, the input voltage provides energy for *L*1 and *C*1 . Hence, the voltage across *L*1 is *Vi* minus *VC* 1 , thereby causing L_1 to be magnetized, and *C*1 is charged. At the same time, the input voltage, together with *C*2 , provides the energy
for *L*2 and the output. Hence, the voltage across *L*2 is *Vi* plus *VC* 2 minus *Vo,* thereby causing *L*2 to be magnetized, and *C*2 is discharged. Therefore, the related equations are depicted as follows:

$$V_{L1} = V_i - V_{C1} \qquad (1)$$
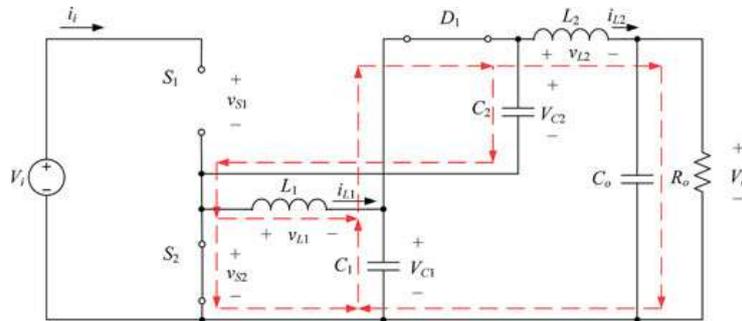$$V_{L2} = V_i + V_{C2} - V_o \qquad (2)$$

Fig. 4. Current flow in state 2.

State 2: As shown As shown in Fig. 4, S1 is turned OFF but S2 is turned ON. During this state, the energy stored in *L*1 and *C*1 is released to *C*2 and the output via *L*2 . Hence, the voltage across *L*1 is minus *VC* 1 , thereby causing *L*1 to be demagnetized, and *C*1 is discharged. At the same time, the voltage across *L*2 is *VC* 2 minus *Vo* , thereby causing *L*2 to be demagnetized, and *C*2 is charged. Therefore, the associated equations are described as follows:

$$V_{L1} = -V_{C1} \qquad (3)$$
$$V_{L2} = V_{C2} - V_o \qquad (4)$$
$$V_{C2} = V_{C1} \qquad (5)$$

By applying the voltage-second balance to (1) and (3), the following equation can be obtained as

$$(V_i - V_{C1}).D.T_s + (-V_{C1}).(1 - D).T_s = 0 \quad (6)$$

Sequentially, by applying the voltage-second balance to (2) and (4), the following equation can be obtained as

$$V_{C1} = D.V_i \qquad (7)$$
$$(V_i + V_{C2} - V_o).D.T_s + (V_{c2} - V_o).(1 - D).T_s = 0 (8)$$

Hence, by substituting (5) and (7) into (8), the voltage conversion ratio of the proposed converter can be obtained as

$$\frac{Vo}{Vin} = 2D \qquad (9)$$

Therefore, such a converter can operate in the buck mode as the duty cycle *D* is smaller than 0.5, whereas it can operate in the boost mode as *D* is larger than 0.5.

IV KEY DESIGN PARAMETER CONSIDERATIONS

In this section, the design of inductors and capacitors are mainly taken into account. Before this section is taken up, there are some specifications to be given as follows: 1) the dc input voltage *Vi* is from 10V to 16V; 2) the dc output voltage *Vo* is 12V; 3) the rated dc load current *Io*−rated is 3A; 4) the switching frequency *fs* is 200 kHz; and 5) the product name of S1 and S2 is APM3109 and the product name of D1 is STP30L45; and 6) the product name of the control IC is ICA7W716.

1. Inductor Design

From an industrial point of view, the inductor is designed under the condition that no negative current in the inductor exists above 25% of the rated dc load current. Therefore, in this letter, the critical point between positive current and negative current in the inductor is assumed at 25% of the rated dc load current. Therefore, the peak-to-peak values of $iL1$ and $iL2$ are expressed by $\Delta iL1$ and $\Delta iL2$, respectively, and can be obtained according to the following equation:

$$\Delta i_{L1} = \Delta i_{L2} = 0.5 I_{o-rated} \quad (10)$$

Therefore, $\Delta iL1$ and $\Delta iL2$ are 1.5 A.

Since the high input voltage makes the inductor not easier to escape from the negative current than the low input voltage, the inductor design is mainly determined by the high input voltage, namely, 16V. Hence, the corresponding minimum duty cycle Dmin is 0.375. Moreover, based on (10), $VC1$ and $VC2$ are both $0.5Vo$, namely, 6V. Also, the values of $L1$ and $L2$ can be obtained according to the following equations:

$$L_1 \geq \frac{D_{min} \cdot (V_i - V_{C1})}{\Delta i_{L1} \cdot f_s} \quad (11)$$

$$L_2 \geq \frac{D_{min} \cdot (V_{C2} + V_i - V_o)}{\Delta i_{L2} \cdot f_s} \quad (12)$$

Therefore, the values of $L1$ and $L2$ both are calculated to be not less than 12.5 μH, and finally, $L1$ and $L2$ have individual PC47RM5Z ferrite cores with turns of 10.5, corresponding to 14 μH.

2. Capacitor Design

(i) Output Capacitor Design: Prior to designing Co, it is assumed that the output voltage ripple Δvo is smaller than 1% of the dc output voltage, that is, Δvo is smaller than 120 mV. Hence, the equivalent series resistance of the output capacitor ESR can be represented by

$$ESR \leq \frac{\Delta V_o}{\Delta i_{L2}} \quad (13)$$

Accordingly, ESR is calculated to be smaller than 80 mΩ, and eventually, one Nippon Chemi-Con (NCC) KY series capacitor of 470 μF with ESR equal to 46 mΩ is chosen for Co.

(ii) Energy-Transferring Capacitor Design: Prior to designing the energy-transferring capacitors $C1$ and $C2$, it is assumed that the values of $C1$ and $C2$ are large enough to keep $VC1$ and $VC2$ almost at 6V, and hence, variations in $VC1$ and $VC1$ are quite small and are defined to be $\Delta VC1$ and $\Delta VC2$, respectively.

Based on this assumption, $\Delta VC1$ and $\Delta VC2$ are both set to smaller than 1% of $VC1$ and $VC2$, respectively, namely, both are smaller than 60 mV. Also, in State 1, $C1$ is charged whereas $C2$ is discharged. Therefore, the values of $C1$ and $C2$ must satisfy the following equations:

$$C_1 \geq \frac{I_{o-rated} \cdot D_{max}}{\Delta V_{C1} \cdot f_s} \quad (14)$$

$$C_2 \geq \frac{I_{o-rated} \cdot D_{max}}{\Delta V_{C1} \cdot f_s} \quad (15)$$

Since the maximum duty cycle, Dmax occurs at the input voltage of 10V, namely, 0.6, both the values of $C1$ and $C2$ are not less than 150 μF. Finally, $C1$ and $C2$ have individual NCC KY series capacitors of 470 μF.

V EXPERIMENTAL RESULTS

The proposed buck boost converter has the voltage conversion ratio of 2D and hence the duty cycle of voltage bucking locate between 0 and 0.5 and the duty cycle of the voltage boosting locate between 0.5 and 1. By calculation with system working equations, we get the proposed converter voltage conversion ratio as 2D. Here an input of 10-16V dc supply is given. The converter works in a linear mode by giving the output of 12V. Normally many applications working in a voltage range of 12V.

Here the output voltage ripple is reduced, PID controller is designed. Here the output voltage ripple reduces to 100mV when the switching frequency is 200 KHz. The proposed system of this KY Converter has much more reduction in the output voltage ripple by Fuzzy logic Controller [14-18].
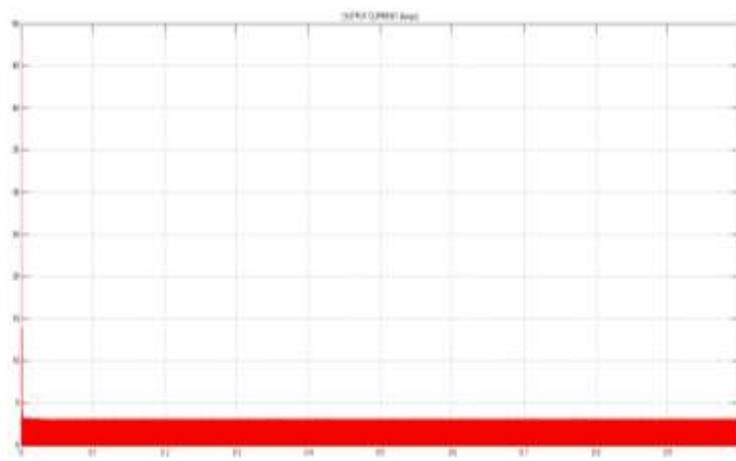
Transient Regions:

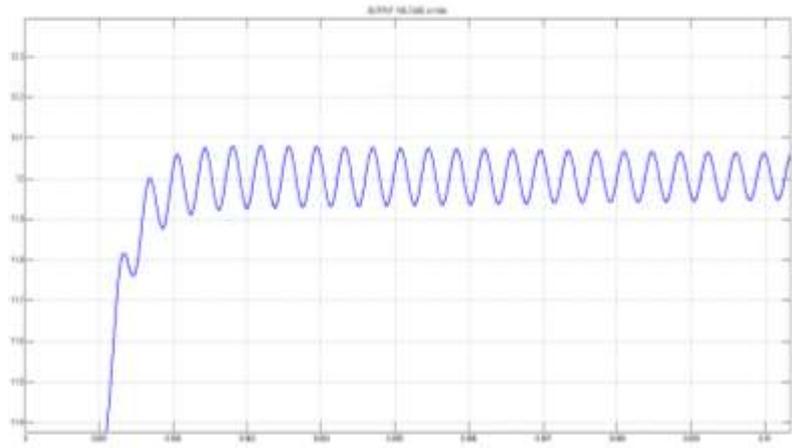Performance characteristics (buck mode).
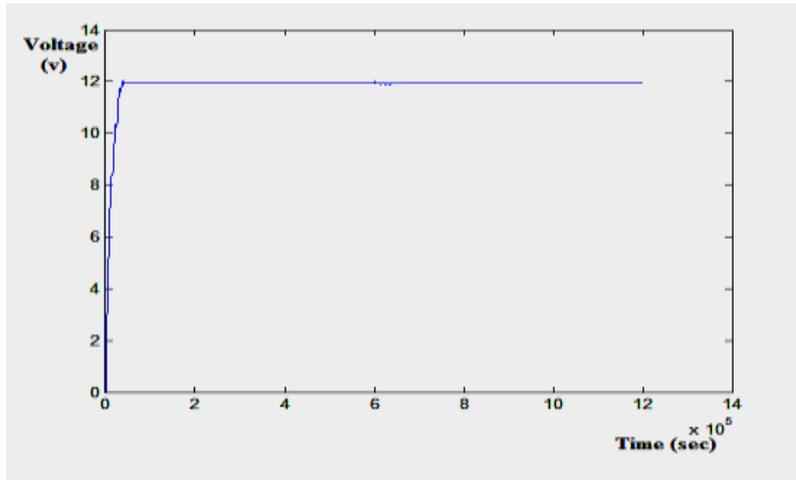
Performance characteristics (boost mode).
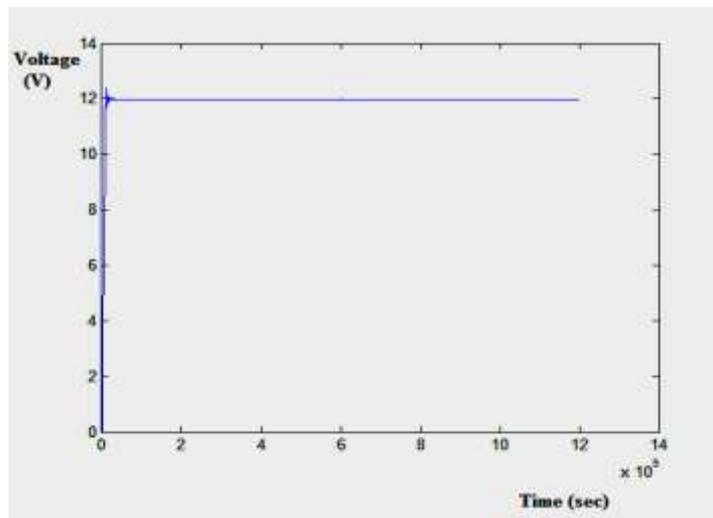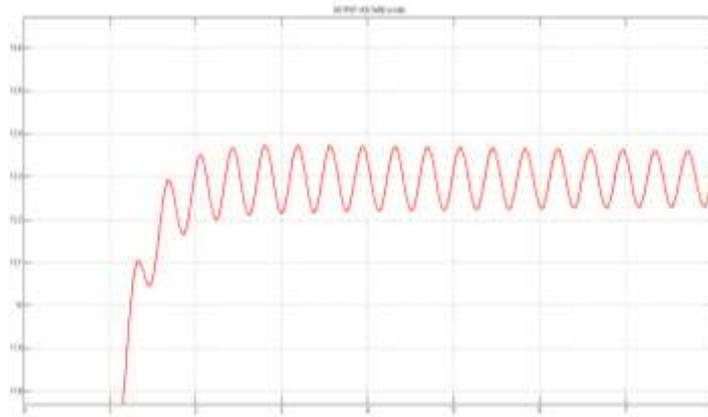

Output inductor current Vs Time

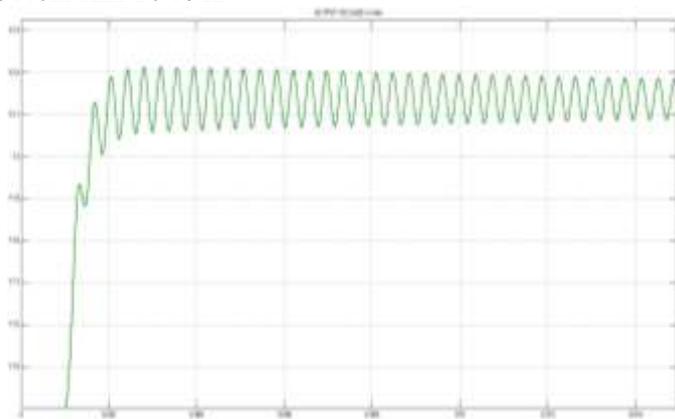**Output Voltage Vs Time with Settling Time**

Settling Time = .0025 sec

Line Variations:
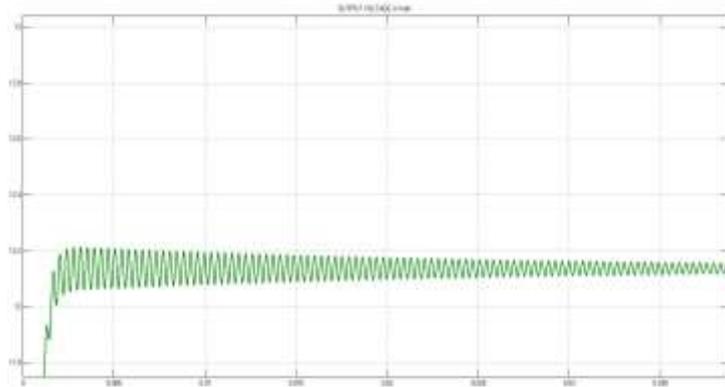A step change in input voltage from 9V to 12V
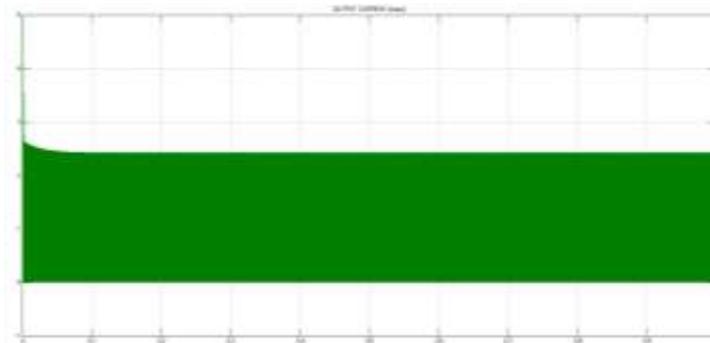

Settling Time=.0022 sec

Load Variations:
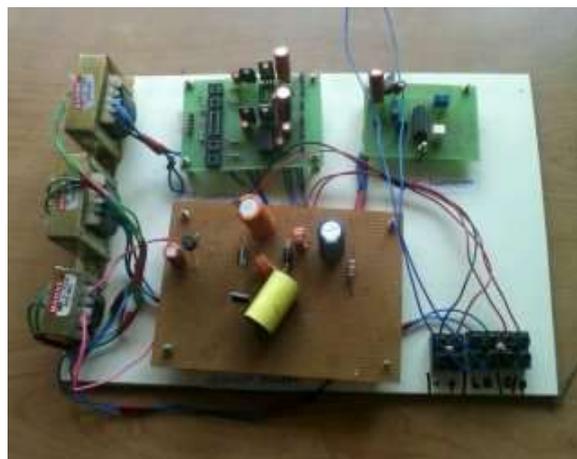Output Voltage At Load Changes From 12Ω To 18 Ω

Steady State Region
Output Voltage

Output Current

Hardware Implementation:

CONCLUSION

By combining the KY converter and the traditional SR buck, a buck-boost converter is introduced with the same power switches and having a positive output voltage and no right-half-plane zero. Furthermore, this converter always operates in Continuous Conduction Mode inherently, thereby causing variations in duty cycle all over the load range not to be so much, and hence, the

control of the converter to be easy. The output current is the non-pulsating waveform thereby not only the current stress on the output capacitor is reduced but also reducing the output voltage ripples. By means of experimental results, it can be seen that for any input voltage, the proposed converter can stably work for any dc load current; the positive buck boost converter widely used in many applications such as better power. We can use the modified non-inverting buck-boost converter in a combination of different modes as required by the application. Thus, a micro system has developed a solution for a buck-boost converter in which the efficiency is maximized, ripple noise is minimized on input and output and minimizes external component requirements and associated cost.

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