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Design and Implementation of HDLC Controller Using VHDL Code

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Abstract: High-Level Data Link Control (HDLC) is a bit oriented full duplex data link layer transceiver. HDLC controller has a Flag register with an 8-bit pattern of 01111110 which generates the state of HDLC protocol. This paper describes the HDLC controller design using VHDL code consists of 16-bit cyclic redundancy checker (CRC) and FIFO. FIFO used for transmits the data. HDLC controller implements on Spartan 6 Xilinx FPGA.

Keywords: CRC, HDLC, Full Duplex, FIFO, Flag Register.

I. INTRODUCTION

HDLC transceiver used for transmits and receives of high-level data link layer protocol in layer 2 (data link layer) of OSI model. International Standards Organization (ISO) builds the HDLC controller which is a bit-oriented full duplex data link layer protocol. HDLC determine a data encapsulation method on synchronous serial links using frame characters and checksums and based on IBM Corporation's Synchronous Data Link Control (SDLC) protocol. HDLC protocol is a frame structure unit, which consists of the flag, info, control bits, CRC and terminates with the same flag bits. It has been widely used throughout the world because it supports the both mode of (half duplex and full duplex) communication lines, point to point and multipoint networks, and switched and non-switched channels [1].

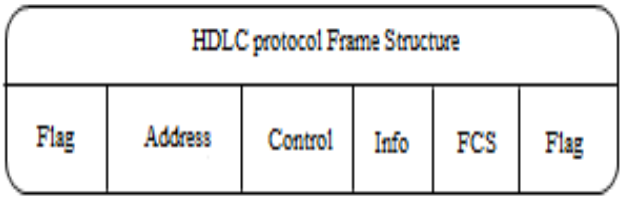

Fig. 1. HDLC protocol frame structure

II. PREVIOUS WORK

The multi-channel design consists a programmable number of HDLC channels which is used the synchronization pulse for divided time division multiplexing (TDM) data stream into a set of 8-bit time slot [2]. HDLC transmit and receive the data over data link layer, data link layer lies between the physical layer and network layer. A packet of data passing through the internetwork in the network layer which can consider many of local area network (LAN) and wide area network (WAN). The physical layer is responsible for the transmission of the bits [3]. HDLC controller has the number of features such as received and transmits control, 8- bit parallel to serial and serial to parallel conversion, synchronous operation, SRAM interface and CRC error detection [4]. CRC-16 removes the error and transmits the data, CRC works on modulo 2 division concept and add the reminder data [5]. HDLC controllers added the information in each data block and detect the error and organize the retransmission of data [6].

HDLC controller used the zero insertion technique and ensures the transparency of data stream [7]. The basic difference between single channel and multi-channel HDLC controller is used a number of multiplexer and de-multiplexer. The flexibility of HDLC controller is very high because it also supports the ISDN frame format [8]. Fig. 1 shows the block diagram of HDLC controller.

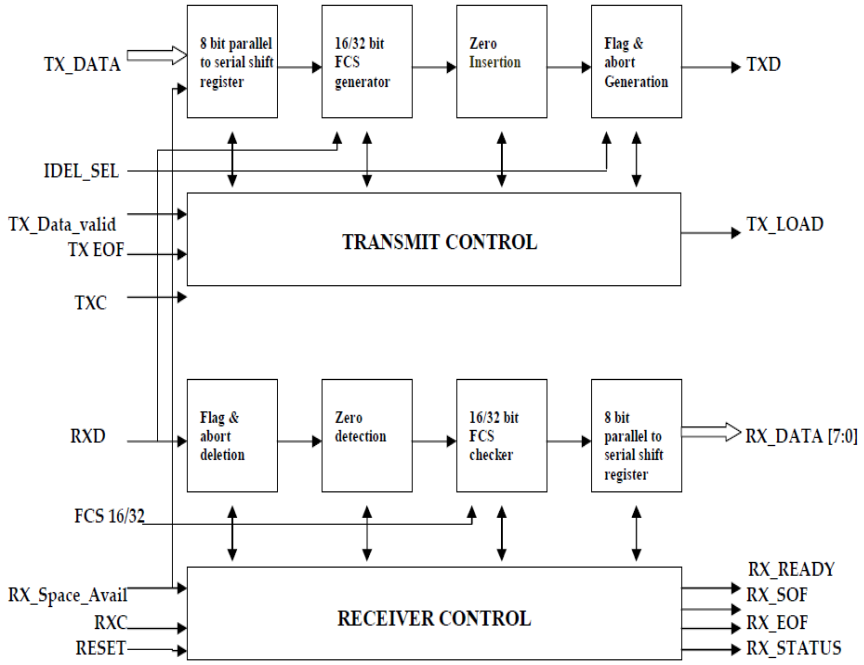

Fig. 2. Block diagram of HDLC controller

III.DESIGN OF HDLC CONTROLLER

Proposed HDLC architecture consists of Transmit module and receiver module. HDLC controller has following features:

1. Flag insertion and detection
2. Abort generation and detection
3. Zero bit stuffing and deletion
4. 16-bit CRC generation and checking
5. CRC-16 can be separately enabled and disabled for transmit
6. Automatic insertion of 1 to 255 IDLE Characters between frames
7. Enable and data valid signals for flow control
8. Operates up to 155.52Mbit/s (STS-3) data rates
9. Full-duplex operation.

A. Transmit Module

HDLC transmitter consists the 8-bit parallel to serial shift register, 16-bit CRC checker, zero insertion, and flag generation. The first packet of data stream converted into a serial signal, then zero insertion used for transparency in the data stream. 16-bit CRC checker detects and remove the error of signal and retransmit the error free signal. CRC checker based on module 2 division concepts generate the polynomial and recording the remainder. The remainder is CRC. Polynomial used in CRC-16:

$$CRC = x16+x15+x2+1 \quad (1)$$

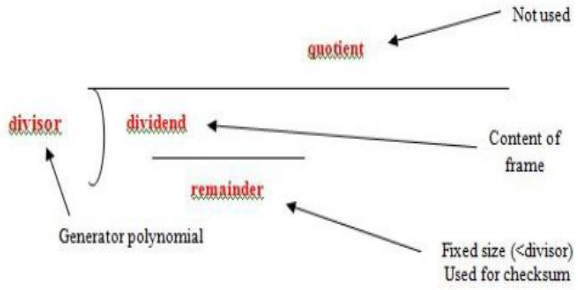

Fig. 3. CRC-16 module division

Flag generation is a bit pattern "01111110" generate the state of the flag and added the information with the data stream and transmit via transmit control in data link layer. The state diagram of transmit module shown in Fig. 4.

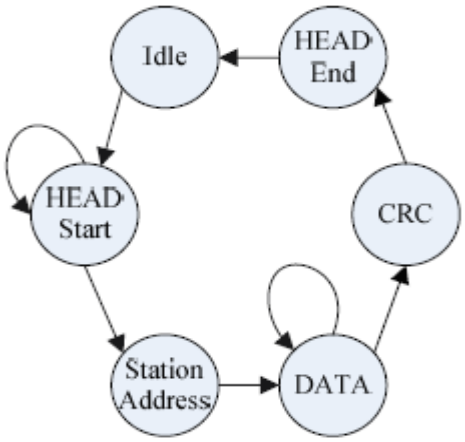

Fig. 4. State diagram of Transmit module

B. Receive Module

HDLC receiver received the data from transmit control and detect the status of flag register then detect the zero insertion. CRC checker checks the generated polynomial the produced the output to the serial to the parallel shift register and finally received the error-free data or information via data link layer. Sate diagram of receive module shown in Fig. 5.

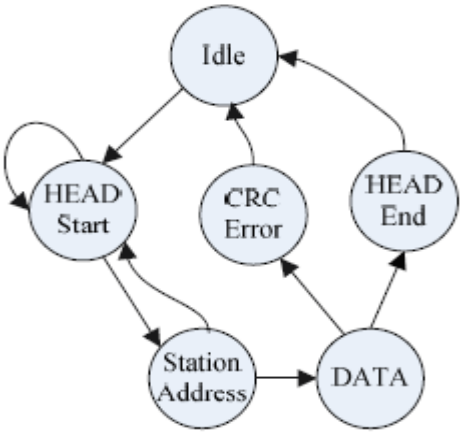

Fig. 5. State diagram of Receive module

IV. IMPLEMENTATION AND SIMULATION OF HDLC CONTROLLER

HDLC controller implements on Spartan 6 FPGA and simulates on Xilinx I sim simulator. Transmission of the data depends on the tenable signal and txc clock signal when both are high data start to transmission and received the signal when reenable and rxc clock signal is high. Fig. 6 and Fig. 7 show the RTL and waveform of HDLC controller.

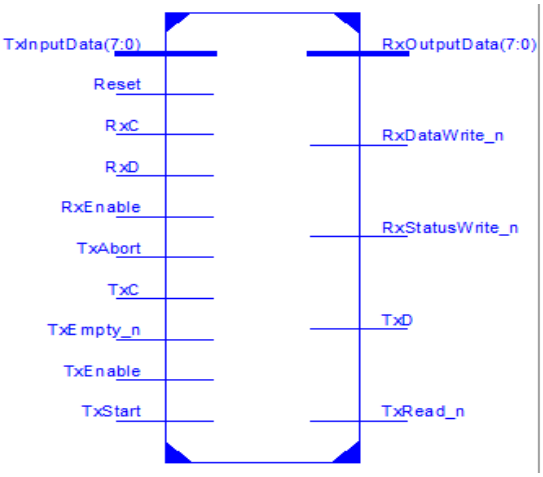

Fig. 6. RTL of HDLC controller

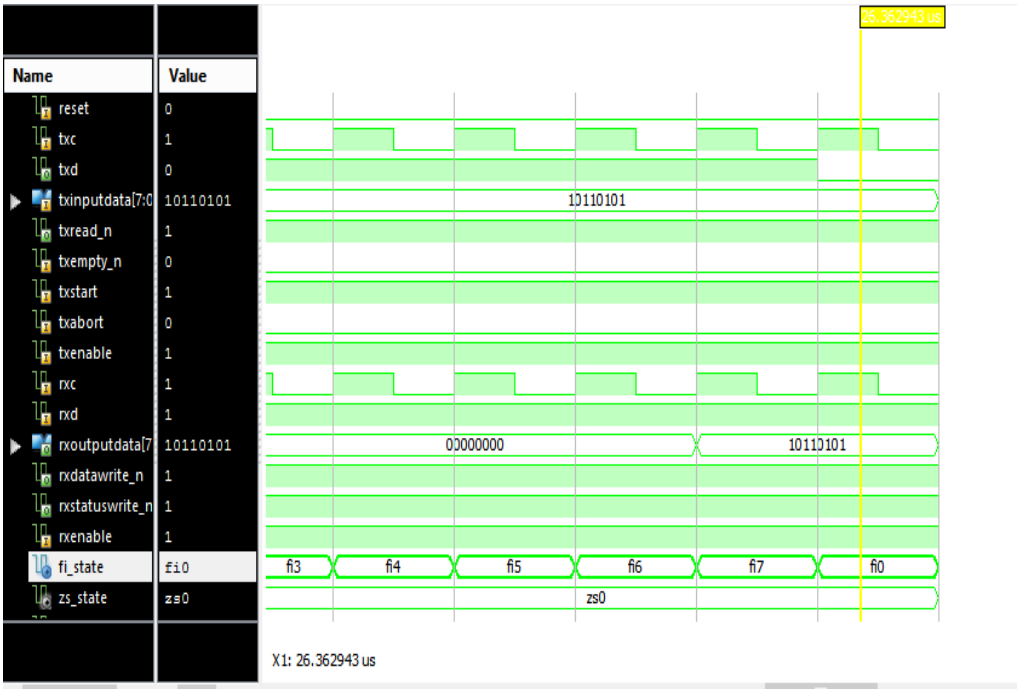

Fig. 7. Waveform of HDLC controller

Proposed HDLC controller design in behavioral modeling using VHDL code and reduced the slices and LUTs as compare to previous work. Table 1 shows the comparison between previous work and purposed work in terms of LUTs and slices.

TABLE: COMPARISION OF DIFFERENT HDLC CONTROLLER

Parameters	**Ref. [3]**	**This work**
No. of LUTs	451	84
No. of Slices	313	41
No. of Slice Flip-Flops	274	108
Number of BUFG/BUFGCTRLs	4	2
Number of FIFO16/RAMB16s:	2	0

HDLC controller implements on different FPGA board in terms of power dissipation. In Spartan 6 HDLC consumes low power but perform faster in Virtex5. Table 3 shows the analysis of power at different FPGA board2

TABLE: POWER ANALYSIS AT DIFFERENT FPGA BOARD

FPGA	**Power**
Spartan 6	15mW
Virtex4	187mW
Virtex5	324mW

CONCLUSION

.In this paper, HDLC controller design using VHDL code behavioral modeling and consists less LUTs and slices. HDLC controller is widely used where the high data rate is required thus HDLC implement on FPGA board and consumes less power and perform more faster as compared to previous Technique such as clock gating technique etc. Finally, HDLC controller performs better as compared to the previous design.

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