INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume3, Issue3)
Available online at www.ijariit.com

Variation Tolerant Sram Cell for Low Power Applications

Dineshkumar .C
Vellalar College of Engineering and Technology Tamil Nadu
dineshkumar0694@gmail.com

M. Parimala Devi
Vellalar College of Engineering and Technology Tamil Nadu
parimaladevim@velalarengg.ac.in

Abstract: ***Static Random Access Memory (SRAM) is the important component across a wide range of microelectronics applications like high-performance server processors, multimedia, and System on Chip (SoC). The lower power consumption, static noise margin (SNM), read and write stability are the major design metrics for designing a SRAM cell. It is difficult to achieve that conventional 6 T SRAM cell in scaled technology, particularly in the deep-subthreshold region. In this paper, the impact of process parameters variations on various design metrics of the proposed cell is presented and compared with conventional 6T and 8T.The proposed 9T cell utilizes a scheme with separate read and writes word lines it is shown that the 9T cell achieves improvements in power dissipation, performance and stability compared with previous designs (that require 6T and 8T) for low-power operation. The 9T scheme is amenable to small feature sizes as encountered in the deep submicron/nano ranges of CMOS technology. The proposed 9T SRAM cell designed in 130 nm Complementary Metal Oxide Semiconductor (CMOS) technology in the power supply voltage of 1.8 V. The simulation is done by using AARON 9.03 tool to achieve the power consumption of 91.55% lesser than existing method, then the read and write delay of proposed 9T SRAM cell is reduced by 8.3% and 23.0% lesser than conventional 6T and 8T.***

Keywords: SOCs, SRAM, Low Power, Static Noise Margin (SNM), Deep Sub-Micron.

I. INTRODUCTION

Static random access memories (SRAMs) are used as a cache memory which is embedded in a microprocessor, system-on-chip, and network-on-chip products. This is due to the fact that they are fast compared to dynamic random access memory (DRAM) and main memory [1]. The 90% of the processor's chip area is occupied by SRAM. The design of a power efficient SRAM cell is one of the most important factors while trying to achieve better chip performances. More than 40% of the active energy is consumed because of leakage currents in modern high-performance processors [2], [19]. An array of SRAM cells is a prime source of leakage currents in modern high-performance processors because a large number of transistors are used in today's on-chip cache memory. Therefore, it is imperative to design a low-leakage SRAM cell [3], [16].

By reducing the supply voltage (*V*DD), dynamic power decreases quadratically and first order leakage power decreases linearly [4]. Therefore, by operating the cell in sub-threshold region (lowering the supply voltage below threshold voltage) [19], it is possible to achieve low-power SRAM cell. To overcome the problem of reading stability, several SRAM cells are proposed which have some additional helpful peripherals circuits. These cells can be classified into two categories are single-ended SRAM cells [11]–[14] and differential SRAM cells [17], [18], [20]. Generally, a single-ended SRAM cell is not that much robust as a differential one. Therefore, it needs some additional compensation technique like separates the read and write path and exhibits read decoupling to maintain reliability.

II. RELATED WORK

Moreover, as the technology node is scaling down, threshold voltage, leakage current and another process, voltage, and temperature (PVT) variations are of great concern [7],[2]. It is more challenging to have the successful operation of a SRAM cell in such low voltage because of RSNM reduction. Furthermore, static noise margin (SNM) has an exponential relationship with the threshold voltage and it degrades linearly as the supply voltage is scaled down [5]. Therefore, the design of highly stable with low power consumption SRAM cell has been the central theme in the past decade. The conventional 6-transistor SRAM cell (hereafter called 6 T cell) depicts weak write-ability or poor read stability in the sub-threshold region [1], [10]. For 6 T cell read stability and writeability are two conflicting design metrics. Therefore, it is extremely difficult to use the 6 T cell in the sub-threshold region [3], [6].

To address these issues, several SRAM cells other than 6 T-cell-like 8T and 9T, have been proposed in the recent to mitigate the issue related to read stability problem, write ability problem and static noise margin [8], [15], And also compare these area to be utilized for the design of 6T, 8T and 9T.

III. PROPOSED 9T SRAM CELL

In this paper, a SRAM cell 9T is proposed in order to achieve improved performance and density. The proposed cell is very similar to the conventional 6T, except the two extra buffer transistors (M6/2), one tail-transistor (M9). The proposed architecture is shown in Fig.1.1.

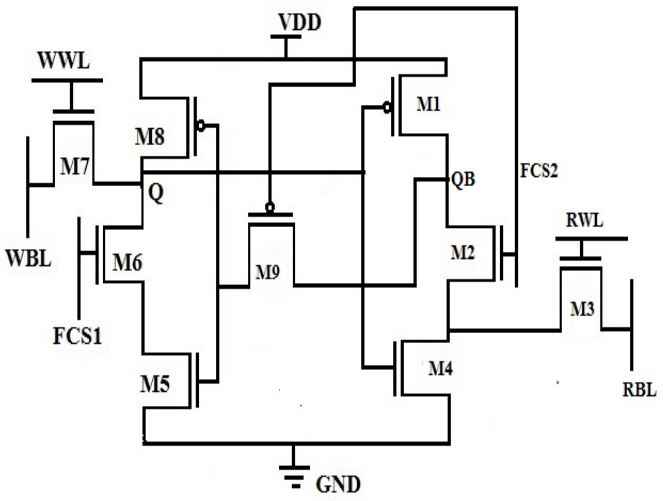

Fig.1.1 9T SRAM cell Design

The proposed 9T has one cross-coupled inverter pair, in which each inverter is made up of three cascaded transistors. These two packed cross-coupled inverters (M1–M2–M4 and M8–M6–M5) retain the data during hold mode. The write word line (WWL) controls by only one nMOS transistor M7, used to transfer the data from single write bit line (WBL) to SRAM cell. A separate read bit line (RBL) controls by only one nMOS transistor M3, used to transfer the data from SRAM cell to the output when read word line (RWL) is activated. Two columns biased feedback control signals FCS1 and FCS2 lines are controlled by the feedback cutting transistors (M6 and M2), respectively. The M9 transistor is used to avoid the negative feedback signal flow from one inverter pair to another inverter pair.

A. Hold Operation

During hold mode, WWL and RWL are kept low and FSC1 and FSC2 is disabled. Both the bit lines BL and BLB remain precharged during hold mode. When the cell is in hold mode, tail transistors M9 is kept OFF as RWL is kept low and output of the SRAM cell is low (because both WL and RWL are low) respectively. This helps to reduce the standby power consumption.

B. Write Operation

During write operation all read control signal to be made low. For write 1 operation FCS1 is made low which turn OFF M6 transistor. When the RWL is made low which turn OFF the M3 transistor and FCS2 high, switch OFF M9 and M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to WBL is 1 and WWL is activated, then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1– M2–M4) changes the state of QB from 1 to 0 in existing method there is an drawback of reverse flow of current from QB to inverter (M5-M6-M8) change the state of Q so its affect the data stored in the cell .So we introduced one extra PMOS for this proposed method its break the reverse flow current from QB to the inverter (M5-M6-M8).

Write a 0 at Q, All read control signal and the feedback control signal to be made low, WWL is made high, FCS1 & FCS2 made low. Then WBL is pulled to the ground or otherwise apply logic '0'. The low going FCS2 turn OFF M2 its avoid QB to the ground. And a logic'0' on the Q turn ON the M1 transistor so QB charged through VDD, make QB change its state from 0 to 1 and Q change its state from 1 to 0 .The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other. The simulations for WT were performed at all process corners. During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS process corner dominated by the fast switching activities. As write 0 operation is faster than writing 1, the write 0 power consumption during write 0 is more as compared with that of write 1 operation.

C. Read operation

The read operation is performed by charging the RBL and activating RWL, at the same time writes signal and feedback control signal made low. If 1 is stored at node *Q* then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to the ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation, therefore, there is no direct disturbance on true storing node QB during

reading the cell. The low going FCS2 leaves QB floating and turn ON M9 transistor, which goes to a negative value then comes back to its original 0 value after the successful read operation.

During read 0 operation, if FCS1/FCS2 turns 1 before RWL is turned 0 then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and *Q*, and transistor M9 turn OFF so any disturbance in QB will not affect *Q*. if Q is 0 and RBL hold pre-charged high value and the inverter sense amplifier gives 0 at the output. After that, if RWL goes low, the positive feedback will restore the respective states (*Q* = 1 and QB = 0).

Transistors	Write 0	Write 1	Read 0	Read 1
M1	ON	OFF	ON	OFF
M2	OFF	ON	ON	OFF
M3	OFF	OFF	ON	ON
M4	ON	ON	ON	ON
M5	ON	OFF	ON	OFF
M6	OFF	OFF	ON	OFF
M7	ON	ON	OFF	OFF
M8	ON	OFF	ON	ON
M9	ON	OFF	OFF	ON

Table.1.1 Read and write operation of 9T SRAM cell

The Table.1.1 shows the corresponding ON/OFF state of each transistor in reading and write operation of proposed 9T SRAM cell.

RESULTS AND DISCUSSIONS

The schematic diagram of the proposed 9T SRAM cell is shown in Fig.1.2.The data storage is performed by an asymmetrical cross-coupled inverter pair.

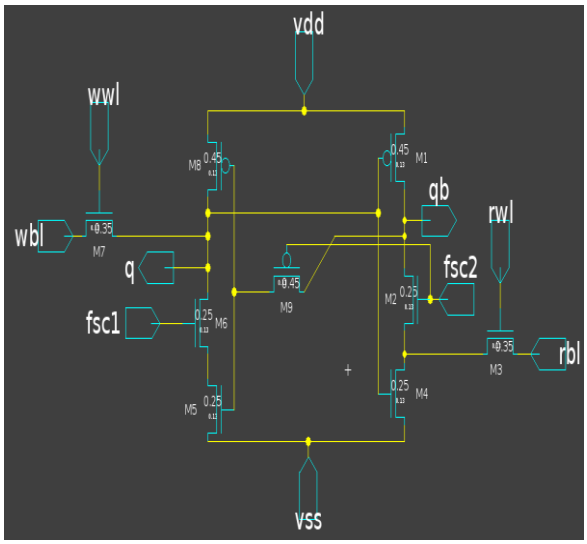

Fig.1.2 Schematic of proposed 9T SRAM cell

Were write Bit Line (WBL) and Read Bit Line (RBL) are used to perform the write and read operation, respectively. Write Word Line (WWL) is activated only in the write mode, and the read operation is performed by enabling the Read Word Line (RBL) signal.

A. Transistor Width Modulation Effect

The cell ratio and pull up ratio affects the stability of SRAM Cell during reading and write operation. The read noise margin increases with increasing the cell ratio, so keep cell area within reasonable values.

a) Cell Ratio

Cell ratio is defined as ratio between the sizes of the driver (pull down) transistor to the size of access transistor as shown in Eq. (1)

$$CR(r) = \frac{\text{the size of pull-down transistor}}{\text{size of the access transistor}} \quad (1)$$

b) Pull up Ratio

Pull up ratio is nothing but a ratio between sizes of the load transistor (pull up) to the size of access transistor as shown in Eq.(2)

$$PR\ (q) = \frac{\text{the size of the pull-up transistor}}{\text{the size of the access transistor}} \quad (2)$$

The transient waveform shows the read delay, write delay of both read and write operation. The write 1 and read 1 waveform of the proposed 9T SRAM cell is shown in Fig.1.3 and Fig 1.4.

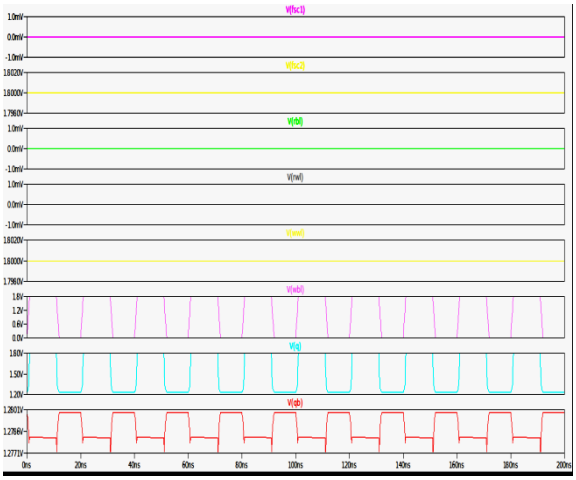

Fig.1.3 Write 1waveform of proposed 9T SRAM cell

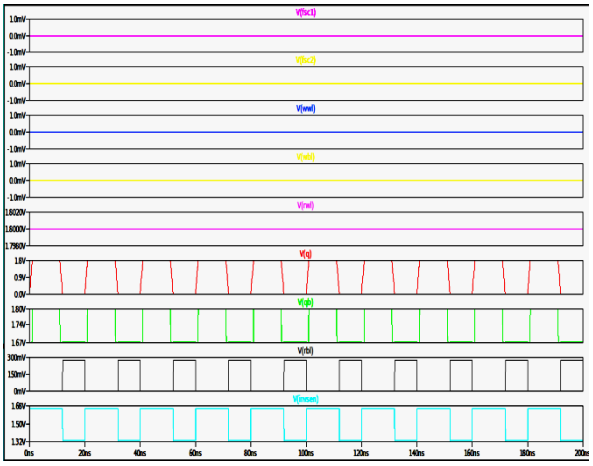

Fig.1.4 Read 1 waveform of proposed 9T SRAM cell

B. SPICE Code

SPICE code is a program used in the integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

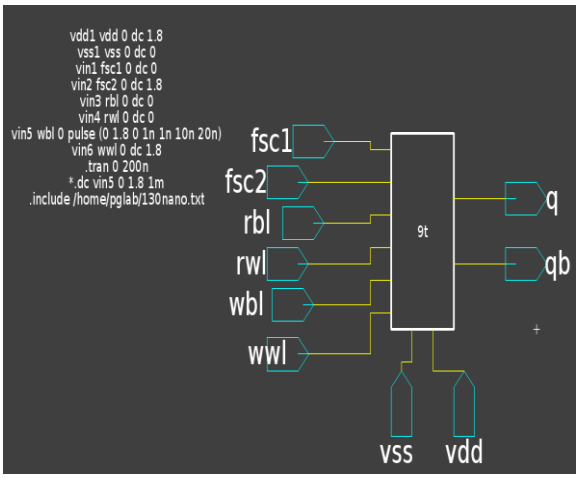

Fig.1.5 Write 1 spice code for 9T SRAM cell

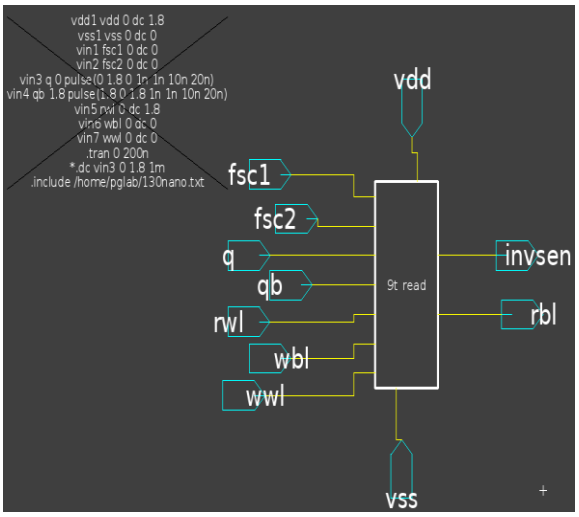

Fig.1.6 Read 1 spice code for 9T SRAM cell

The proposed 9T SRAM cell has separate read and writes operation and its corresponding spice code is shown in Fig.1.5 and Fig 1.6.

C. Cell Layout

The area layout of proposed 9T is drawn in 130-nm CMOS technology, as shown in Fig.1.7. The 9T occupies a 1.3× area as compared with that of 6T. Due to the design constraints and the contact area between M2, M3, M4, and M8 for proposed 9T, there is 2× area overhead as compared with the 6T cell. Even though it has 2× area of 6T, but its better built-in process tolerance and dynamic voltage applicability.

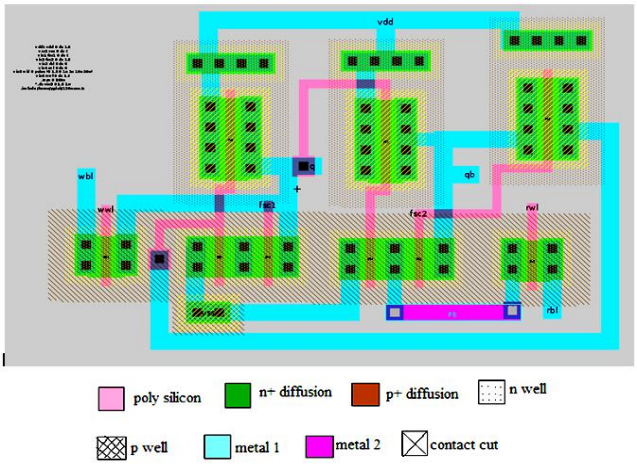

Fig.1.7 Layout of proposed 9T SRAM cell

The comparison of 8T subthreshold SRAM cell and 9T SRAM cell in different process parameter variation like write delay, read delay, supply voltage, technology, power consumption, resistance value, capacitance value, temperature, MOS models, wire delay and gate delay is shown in Table 1.2.

Parameters	8T Sub-threshold SRAM cell	9T SRAM cell
Power consumption	32.401mW	1.428mW
Temperature	27°C	27°C
MOS models	Level 3	Level 3
Supply voltage	1.2V	1.2V
Write delay	50.0ns simulation in 13s	50.0ns simulation in 11s
Read delay	200.0ns simulation in 40s	200.0ns simulation in 25s
wire delay	0.100ns	0.070ns
Gate delay	0.030ns	0.030ns
Resistance value	1545ohm	1507ohm
Capacitance value	31.08fF	32.45fF

Table 1.2. Comparison of 8T subthreshold SRAM cell and 9T SRAM cell

CONCLUSION

A 9T SRAM cell is accessible in this paper for high read stability and low energetic power consumption. For low leakage and high-speed circuits, the concern should be on both the factors speed and power. The proposed 9T SRAM cell provides two separate data access mechanisms for reading and writes operations. During the read operation, the data storage nodes are completely isolated from the bit lines, thereby improving the read SNM by twice as compared to the read SNM of the conventional 6T SRAM cell. During the write operation, the SRAM cell utilizes the charging & discharging by only one bit line (BL), resulting in a reduction of dynamic power consumption as compared to conventional 6T SRAM cell. Different techniques have been analyzed to reduce the standby leakage current & dynamic power dissipation of the SRAM cell. In the proposed 130nm technologies are analyzed using the AARON EDA software and is used to analyze parameters such as power consumption, delay time and operating frequency. Based on the results obtained when compared with the existing methods, by utilizing the above-proposed method it is clearly observed that there is a 91.55% decrease in power consumption and stability improvement of the memory cells.

REFERENCES

[1] Hassanzadeh S., Zamani M., Hajsadeghi K., and Saeidi R. (2013),'A novel low power 8T-cell sub-threshold SRAM with improved read-SNM', in Proc. 8th Int. Conf. Design Technol. Integr. Syst. Nanoscale Era (DTIS), pp. 35–38.

[2] Kushwah C. B. and Vishvakarma S. K. (2016),'A single-ended with dynamic feedback control 8T subthreshold SRAM cell', IEEE transactions on very large scale integration systems, Vol.24, No.1, pp. 373 - 377.

[3] Pasandi G. and Fakhraie S.M. (2014),'An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs', IEEE transactions on very large scale integration (VLSI) systems, Vol. 61, No. 7, pp. 1-9.

[4] Saeidi R., Sharifkhani M. and Hajsadeghi K. (2014), 'A subthreshold asymmetric SRAM cell with high read stability', IEEE Transactions on Circuits System II, Vol. 61, No. 1, pp. 26–30.

[5] Sayeed Ahmad, Mohit Kumar Gupta, Naushad Alam and Mohd Hasan (2016), 'Single-ended schmitt-trigger-based robust low-power SRAM cell', IEEE transactions on very large scale integration systems, Vol.24, No.8, pp. 2634-2642.

[6] Soumitra Pal and Aminil Islam (2016),'Variation tolerant differential 8T SRAM cell for ultralow power applications', IEEE transactions on computer-aided design of integrated circuits and systems, Vol.35, No.4, pp.549-558.

[7] Wen L., Li Z., and Li Y. (2014), 'Analysis of a read disturb-free 9T SRAM cell with bit-interleaving capability', Microelectronics journal, Vol. 45, pp. 815-824.

[8] Younghwi Yang, Juhyun Park, Seung Chul Song, Joseph Wang, Geoffrey Yeap and Seong-Ook Jung (2015),'Single-ended 9T SRAM cell near-threshold voltage operation with enhanced read performance in 22-nm FinFET technology', IEEE transactions on VLSI systems, Vol. 23, No. 11, pp.2748-2752.

[9] Kushwah C and Vishvakarma S. K.(2012), 'Ultra-low power subthreshold SRAM cell design to improve read static noise margin', in Progress in VLSI Design and Test (Lecture Notes in Computer Science), vol. 7373. Berlin, Germany: Springer-Verlag, pp. 139–146.

[10] Yang B.D and Kim L.S. (2005), 'A low-power SRAM using hierarchical bit line and local sense amplifiers', IEEE J. Solid-State Circuits, vol. 40, no. 6, pp. 1366–1376.

[11] Chang L., et al.(2008), 'An 8T-SRAM for variability tolerance and low-voltage operation in high-performance caches', IEEE J. Solid-State Circuits, vol. 43, no. 4, pp. 956–963.

[12] Tu M.H., et al.(2102), 'A single-ended disturb-free 9T subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing', IEEE J. Solid-State Circuits, vol. 47, no. 6, pp. 1469–1482.

[13] Pasandi G and Fakhraie S. M.(2015), 'A 256-kb 9T near-threshold SRAM with 1 k cells per bit line and enhanced write and read operations', IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 11, pp. 2438–2446.

[14] Zhai B., Hanson S., Blaauw D. and Sylvester D. (2008), 'A variation-tolerant sub-200 mV 6-T subthreshold SRAM', IEEE J. Solid-State Circuits, vol. 43, no. 10, pp. 2338–2348.

[15] Liu Z and Kursun V. (2008), 'Characterization of a novel nine-transistor SRAM cell', IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 4, pp. 488–492.

[16] Islam A and Hasan M. (2012), 'A technique to mitigate the impact of the process, voltage and temperature variations on design metrics of SRAM cell', Microelectron. Rel., vol. 52, no. 2, pp. 405–411.

[17] Do A. T., et al. (2011), 'An 8 T differential SRAM with improved noise margin for bit-interleaving in 65 nm CMOS', IEEE Trans. Circuits Syst. I, Reg. Paper, vol. 58, no. 6, pp. 1252–1263.

[18] Benton H. Calhaun, Anantha P. Chandrakasan (2006), 'Static Noise Margin Variation for Sub-threshold SRAM in 65 nm CMOS', IEEE Journal of Solid-State Circuits, vol.41, pp.1673-1679.

[19] Wen L., Li Z., and Li Y. (2013), 'Single-ended, robust 8T SRAM cell for low-voltage operation', Microelectron. J., vol. 44, no. 8, pp. 718–728.

[20] Takeda K., et al. (2006), 'A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications', IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 113–121.

