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Low Power Full Adder Circuit Design Using Two Phase Adiabatic Static CMOS Logic

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Abstract: Adiabatic logic is used to minimize the energy loss during operation of the circuit. Using two-phase adiabatic static CMOS logic (2PASCL) the power consumption can be reduced. This paper compares the power consumption of Static Energy Recovery Full Adder(SERF) and the proposed full adder using two phase adiabatic static CMOS logic(2PASCL). The average power consumption of proposed full adder is 4.8pW which is very less in a comparative study with SERF. The result of this work focuses on the reduction of power consumption with the scaling down technology.

Keywords- Adiabatic Logic, 2pascl, Low Power, Full Adder, Static Energy Recovery Logic.

I. INTRODUCTION

In fast growing technology in mobile computation and communication, it is necessary to design low power VLSI system. VLSI system-on-chip (SOC) designs the address by increasing the clock frequency and incorporating more components on the chip, supported by scaling of the processing technology. Increasing clocks, logic speeds, and complexity of high performances results in increasing power consumption and turns out to be major hindrance adding on the cooling cost and battery life of portable devices [1]. In earlier studies, it is observed that adiabatic circuits have less energy dissipation in comparison to CMOS circuits. Hence low power adiabatic circuit can be operated on frequency range in which the signals are digitally processed. In diode based adiabatic logic families, there is disadvantage power dissipation in charges across the diodes [2].

The energy dissipation can be reduced by using 2PASCL (two phase clocked adiabatic static CMOS logic) is different from other diode families in which high amplitude and reduced energy dissipation can be achieved. In 2PASCL technique, we use split level sinusoidal driving voltage to reduce the dynamic power consumption.

II. ADIABATIC LOGICS CIRCUITS

Less power is dissipated in adiabatic logic compared to static CMOS circuits. Adiabatic logic circuits minimize the energy loss during charging/discharging. A constant current is used to reduce the power dissipation. It uses the time varying voltage to reduce the switching activity hence AC supply is used to specific phase to recover the supplied charge. Therefore if I am considered as the average current flowing to CL, so the overall energy dissipated during the transition.

$$^{2}R \quad = (\quad)^{2}R \quad =(\quad / \quad) \qquad . \ ^{2} \qquad (1)$$

Theoretically, during adiabatic charging, when Tp, the time for the driving voltage φ to change from 0 V to Vdd is long, energy dissipation is nearly zero.

III. STATIC ENERGY RECOVERY FULL ADDER

In this type of adder shown in Figure 1(c), the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The circuit consists of two XNORs accomplished by 4 transistors. The sum is generated from the output of the second stage XNOR circuit. The Cout can be calculated by multiplexing and Cin controlled by (a ⊗ b). The circuit produces full-swing at the output nodes [4]. But it fails to provide so for the internal nodes. As the power consumption by the circuit demotes and it becomes slower.

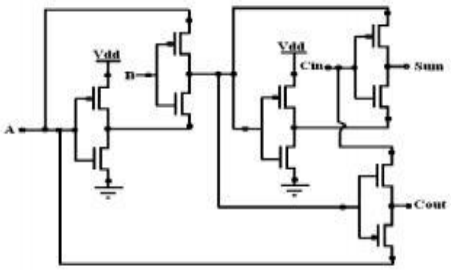

Fig.1. Static Energy Recovery Full Adder

IV. **2PASCL**

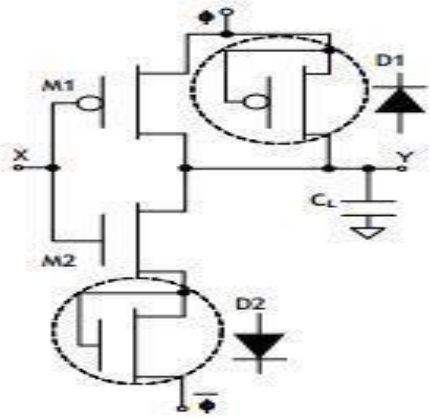

Fig.2. 2PASCL

In this circuit of two phase adiabatic static CMOS logic (2PASCL).two diodes are used as shown placed between the output node and the power clock and the second diode is adjacent to the nMOS logic circuit and connected to another power source used for improving the discharging speed of internal nodes.

The system uses a two-phase clocking split-level sinusoidal power supply, wherein φ and φ replace Vdd and Vss, respectively. One clock is in phase and the other is inverted. By using these two split-level Sinusoidal waveforms, the voltage difference between the current-carrying electrodes can be minimized, and consequently, power consumption can be suppressed. The substrates of the pMOS and nMOS transistors are connected to φ and GND respectively. From the previous design of complementary sinusoidal voltage driver clocks of each Vp−p being 0.9 V [7]. The values are at evaluation phase.

IV**. FULL ADDER USING TWO-PHASE ADIABATIC STATIC CMOS LOGIC**

This full adder is being designed using two phase adiabatic static CMOS logic which uses the Split level technology to reduce the power consumption and high amplitude [6]. The system uses a two-phase clocking split-level sinusoidal power supply, wherein clock (CLK) and clock bar (clkbar) replace Vdd and Vss, respectively. One clock is in phase and the other is inverted.

The main aim is to reduce the power consumption which is useful in the upcoming technology.

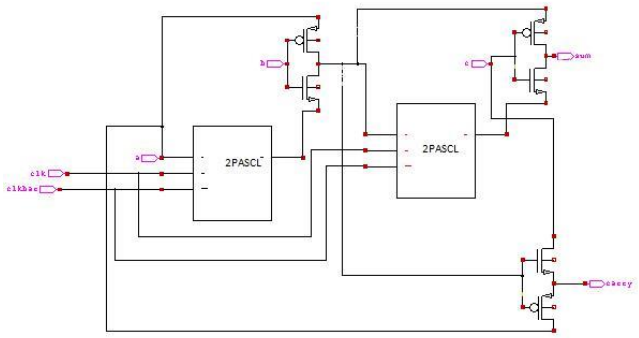

Fig.3. 2PASCL full adder

This proposed full adder is designed using two phase adiabatic static CMOS logic (2PASCL) as mentioned to reduce the power consumption.

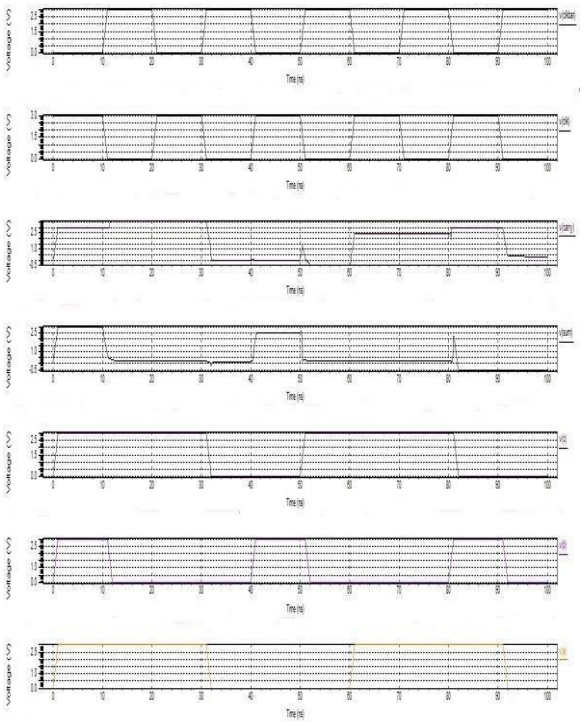

Fig 4. Simulated waveforms

V. SIMULATION AND RESULTS

Fig. 3 is the waveform of a full adder using 2PASCL. The simulation was performed on SPICE circuit simulation with 180nm. The symmetrical clock is studied where the results are observed at the evaluation phase (clk= high and clkbar= low). The frequency of the clock is being changed and studied. The average power consumption of fuller adder using 2PASCL IS 4.8pW and for static energy recovery full adder is 3.18mW.

It is clearly observed that the average power consumption of full adder using 2PASCL comparatively very less as compared to static energy recovery.

CONCLUSION

From the results, it is concluded that the proposed circuit i.e. full adder design using two phase adiabatic static CMOS logic (2PASCL) have less average power consumption on caparison with a static energy recovery full adder. The motive is to reduce the power consumption of the circuit in fast growing technology.

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