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ASIC Implementation of 64 -Bit Comparator Using Reversible Logic

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Abstract: A need for low power ICs arises to keep the power density of ICs within tolerable limits. While the power dissipation increases linearly with advanced version processors, the power density also increases exponentially, because of the ever-shrinking size of the integrated circuits. Reversible logic is emerging as an important research area in the recent years due to its ability to reduce power dissipation, which is the main requirement in low power digital design. In our proposed method reversible comparator based on CMOS logic circuit is designed using reversible gates. In this design, we try to reduce optimization parameters like a number of constant inputs, garbage outputs, and quantum cost. The experimental results obtained for implementation in CADENCE EDA 180nm technology shows the considerable reduction in terms of Power Delay Product in comparison with the comparator designed using conventional gates.

Keywords: Low Power digital Design, Reversible Logic, Power Delay Products.

INTRODUCTION

Digital or Binary Comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs. For example, along with being able to add and subtract binary numbers, we need to be able to compare them and determine whether the value of input A is greater than, smaller than or equal to the value at input B etc.

Currently, Reversible logic is one of the most promising Logic in different areas of application like low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication & computer Graphics. Rolf Landauer's [14] research has proved that "the amount of energy dissipated for every irreversible bit operation = $KT \ln 2$ joules"

Where,

- $K=1.3806505 \times 10^{-23} \text{m}^2 \text{kg}^{-2} \text{K}^{-1}$ (joule/Kelvin) is the Boltzmann's constant
- T is the temperature at which the operation is Performed.

This means that information loss is a physical phenomenon. The heat generated due to the loss of one bit of information is very small at room temperature. However, when the number of bits is more, (as in the case of high-speed computational works) the heat dissipated by them will be so large that it affects the performance and results in the reduction of the lifetime of the components. Fortunately, in 1973, [12] Bennett showed that $KT \ln 2$ energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs. Reversible logic supports the process of running the system both forward and backward.

Comparators already available are added based comparator, priority encoder based comparator, Bit-wise Competition Logic comparator etc. As always happens in the design of digital circuits, achieving high speed is not the only concern. Low power consumption and reduced silicon area are equally important design goals. C.-C. Wang et al [1] the power dissipation and area used

by the design is relatively large and also not suitable for single cycle operation. Huang and Wang et al. [2] is based on priority encoding algorithm and it increases the operating speed and eliminates the long dynamic chains. But due to more execution steps, the energy dissipation is high. Hierarchical prefix tree structure [3] J. E. Stine et al used reduces delay and improves the scalability for the 2-bit comparator. While increasing the bit level its cascaded structure increases its area and delay.

The method adopted by H.-M. Lam and C.-Y. Tsui, [4] is parallel MSB checking algorithm. It introduces priority encoding algorithm. H.-M. Lam and C.-Y. Tsui [5] proposed a comparator based on MUX architecture for MSB checking algorithm. But hardware complexity and delay penalty increased here. Kim and Yoo [6] follow bitwise computation logic after pre-encoding, to find out the first '1' away from MSB. In [7] and [8] tree structure based comparator is followed. Computation speed increased here but it not suitable for static logic implementation. In these designs, add/vt ratio is less. Comparator using redundant binary signed digit number [9] improved the speed and is efficient for comparison within larger operand. But each bit. For this comparison, the number representation depends on polarities. Comparator utilizing hybrid PTL/CMOS logic style [10] shows low power design as compared to CMOS and pass transistor logic design. In [11] proposed scalable high-speed low power comparator using regular digital hardware structure. But these structure increases the leakage power and delay. All the designs considered are implemented using conventional gates

In the proposed design the reversible gates are used in the design of comparator logic and its performance is compared with the convention gate design comparators. The organization of the paper is such that Section II explains the development of 64-bit comparator using the conventional gates. Section III uses the same concept but the gates used are reversible gates.

II. CONVENTIONAL COMPARATORS

The conventional comparator uses standard gates like AND gate, OR gate, NOR gate, EX-NOR gate, NOT gate etc., The combinational blocks contain the AND Gate, OR Gate, and NOR Gate. The block diagram of the 4-bit comparator is given in figure 1. The cascade logic is used to convert the 4-bit comparator to 8 Bit and then 64-bit comparator. The block Diagram of 64-bit comparator is shown in figure 2.

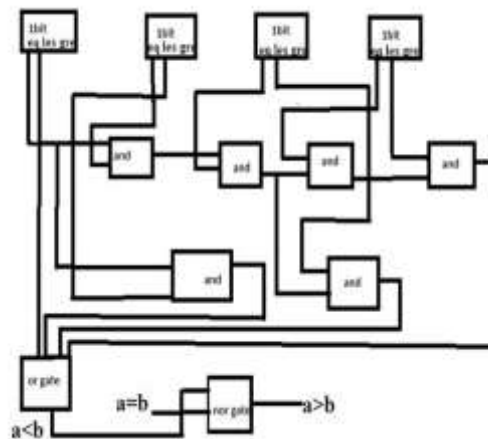


Figure.1 Block Diagram of Cascade Logic 4-bit Comparator

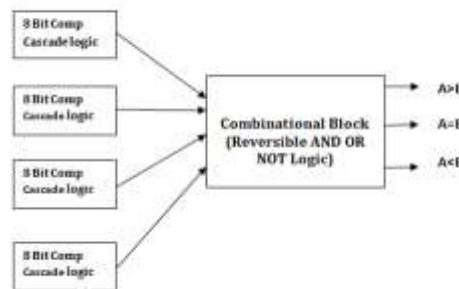


Figure.2 Block Diagram of Cascade Logic 64-bit Comparator

i. Equality Condition

When all the AND gates produce the High Output then the condition is equal.

ii. Less Than Condition:

If the equality condition fails the second level AND gate used checks for "less than" condition and finally the output of AND gate is given to OR gate along with equality condition to obtain the lesser condition

iii. Greater Than Condition:

Simple NOR logic is used to find the greater than the condition. The same logic is used for the implementation of 64-bit comparator also.

III. REVERSIBLE COMPARATORS

Reversible one-bit comparator is implemented with Feynman gate and TR gate and BVF gate. The number of garbage outputs is one and represented as G1, it uses two constant inputs, logic 0 and logic 1 and its quantum cost is 7. If A=1, B=1 the F gate driving the output1 is 1 given to TR second input. The output2 of FG gate is 0 given to BVF gate input2. These two gates output is fed to the input of BVF gate. Therefore the output of the AXOR is 1 which gives the equal condition. The block diagram of 1 Bit reversible comparator is shown in figure 3.

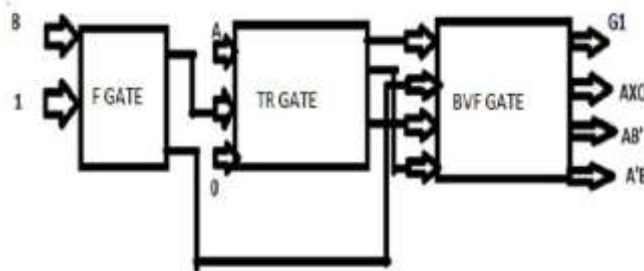


Figure3 Single bit Reversible Comparator

The reversible four-bit comparator implemented using single bit comparator blocks designed using reversible gates. Reversible AND gate is designed by reversible Peres gate. Reversible OR and NOR gate is designed by Modified Toffoli gate.

The cascading logic of 4-bit reversible comparator is used to construct the reversible 8-bit comparator. Similarly, the 64-bit comparator is also constructed. The logic flow is same as the conventional 1-bit comparator. The reversible AND, OR, NOR Gates are done Peres and Toffoli gate.

IV. Results and Discussion:

The Schematic implementation of the 64-bit comparator in CADENCE EDA tool in 180nm technology is shown in the figure below.

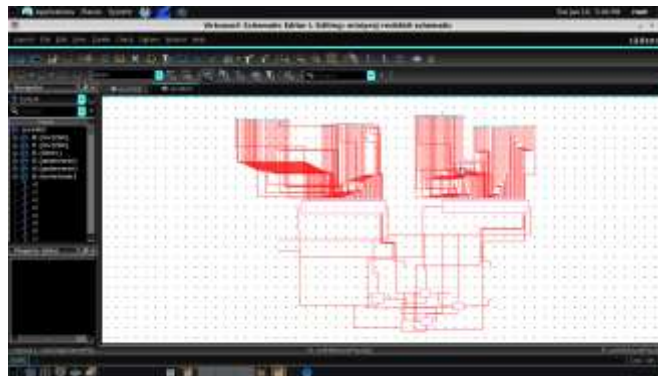


Figure4: Reversible Implementation Cascade Logic 64-bit Comparator

The major advantage in reversible logic implementation is the reduction of consumed power and the heat dissipation is less. The static and dynamic power consumption for single, 8 bit, 16 bit, 64-bit comparator designed using conventional AND OR NOT gates and reversible gates are tabulated in Table 1.

Table 1. Comparison of power Consumption of Conventional and Reversible Comparator

Single bit comparator					
S.NO	FREQUENC Y	CONVENTIONA L		REVERSIBLE	
1	3.4GHz	2.88nw	928nw	96mw	286nw
2	100KHz	2.88nw	484mw	96mw	200uw
3	10KHz	2.88nw	928uw	96mw	90uw
4 Bit Comparator					
1	3.4GHz	2.88nw	928nw	2.88mw	1mw
2	100KHz	2.88nw	484mw	2.88mw	1.4mw
3	10KHz	2.88nw	928uw	2.88mw	1.45mw
8-bit comparator					
1	3.4GHz	51.99n	4.51mw	2.84mw	1.15mw
2	100KHz	51.99n	4.1mw	2.84mw	1.16mw
3	10KHz	51.99n	4.1mw	2.84mw	1.16mw

16-bit comparator					
1	3.4GHz	106.1nW	20.9mw	147mw	4.4mw
2	100KHz	106.1nw	19.9mw	147mw	4.5mw
3	10KHz	106.1nw	20.94mw	147mw	4.48mw
64 Bit Comparator					
1	3.4GHz	203nw	34.6mw	198mw	5.414mw
2	100KHz	203nw	32.7mw	198mw	5.412mw
3	10KHz	203nw	33.6mw	198mw	5.414mw

CONCLUSION

The proposed reversible binary comparator based on cascade logic approach having less power consumption. The design is based on the useful properties of the reversible gates suitable for mapping the comparator Boolean equations. The design presented has shown better results than the existing conventional design of reversible binary comparator in terms of power consumption and the propagation delay. Due to these logics, the proposed design achieves reduction of dynamic power from 34.6mW to 5.414mw compared to the conventional design of 64-bit binary reversible comparator. The comparator designs proposed can be used for realizing the hardware design of the quantum algorithms.

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