INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume3, Issue2)
Available online at www.ijariit.com

A Review of Low Power Consumption Clock Gating Techniques

Priyanka Saraswat
Electronics and Communication engineering
IEC College of engineering and technology, Dr. A.P.J Abdul Kalam Universiity
Saraswatp59@yahoo.com

Abstract: This paper represents a review of some existing clock gating techniques for low power dissipation in digital circuitry designs. In this paper, the clock gating techniques are used which reduces the power consumption from the normal implementation of the same design. The 16 bit ALU (arithmetic logical unit) is used for reducing the dynamic power consumption through gating techniques by shutting down the clock at a given instant of time when it is not needed for work to prevent the unnecessary power consumption of the system. These designs are implemented on RTL level at VIVADO 2016.4 platform for synthesis and simulation by different gating techniques.

Keywords: RTL, ALU, ISE, Clock Gating, Glitch.

1. INTRODUCTION

Power consumption is the main issue of today's world which drains out the battery of compact devices faster. The maximum of the dynamic power is consumed in the clock signal. Clock signals have a high frequency and consume up to 70% of total power [1]. This signal doesn't carry any information but continues processing the functionality. Hence, by using functional blocks which contain logic gates and flip-flops is connected to the main module design to reduce the power consumption of the system. This functional block is clock gated which shutting down the clock signals at a given time for reducing the power consumption. The power is directly proportional to the given supply voltage and clock frequency [2].

Power= C_L . F . V_{DD}^2

2. REVIEW OF CLOCK GATING TECHNIQUES ON 16 BIT ALU

A. AND Gate Clock Gating

The implementation of AND gate is also known as latch free technology [3][4][5]. In this technique, AND gate is used with the enable signal and clock as an input and its output is connected to the main module of 16 bit ALU. When the enable signally is high with the clock signal the ALU operations occurs and when enable signal is OFF the clock of ALU is also OFF.

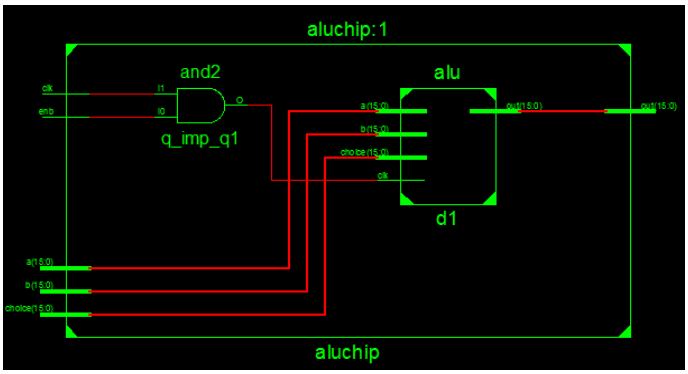

Figure1. And gate or latch free clock gating implementation on 16-bit alu

DISADVANTAGE OF AND GATING

When the enable signal goes low before the clock pulse falling edge the gated pulse is automatically terminated before the actual termination[2] [3] as shown in figure (3).

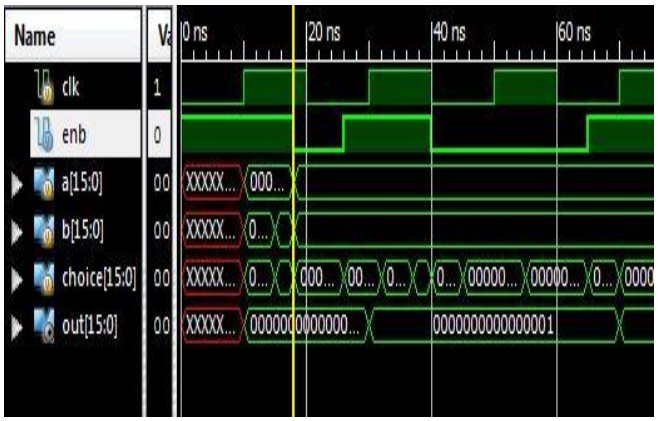

Figure 2. Simulation of and clock gating

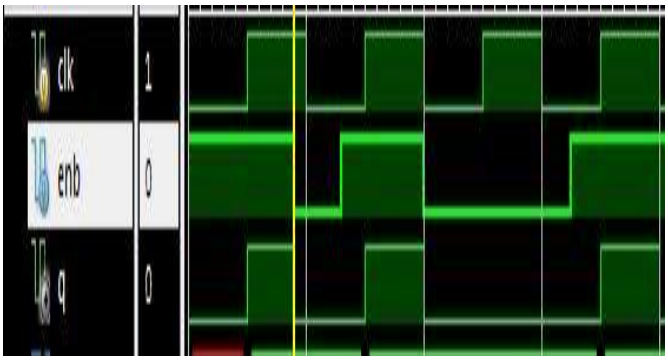

Figure 3. Auto termination of gated pulse before clock

B. LATCH-BASED CLOCK GATING

The latch-based clock gating technique is implemented to avoid the glitches in the above design module [1][3][4][5]. In this technique, the enable and the clock signal is taken as an input of the latch and the output of latch and clock is taken to an input of AND gate. The output of AND gate is 'GCLK'. This clock is taken as a global clock for ALU which avoids the problem of glitches occurs in the simulation as shown in figure (6). The RTL module is shown figure (4) and its simulation in figure (5)

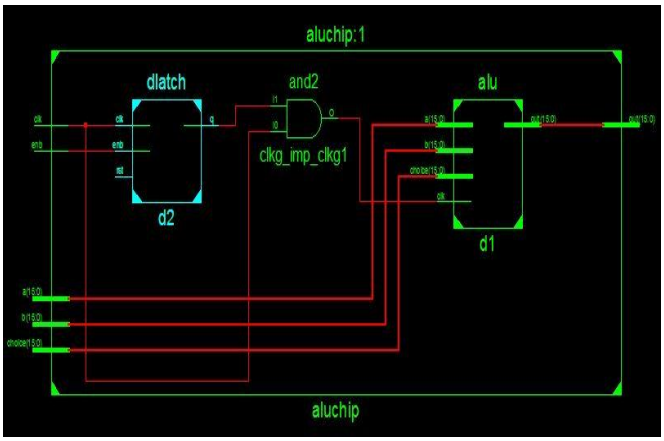

Figure 4. Rtl module of latch based clock gating

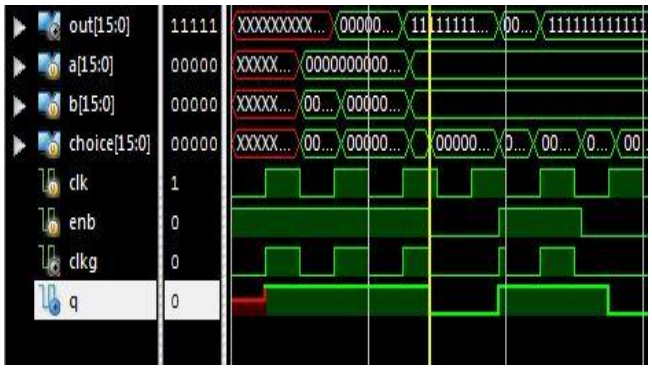

Figure 5. Simulation of latch based clock gating

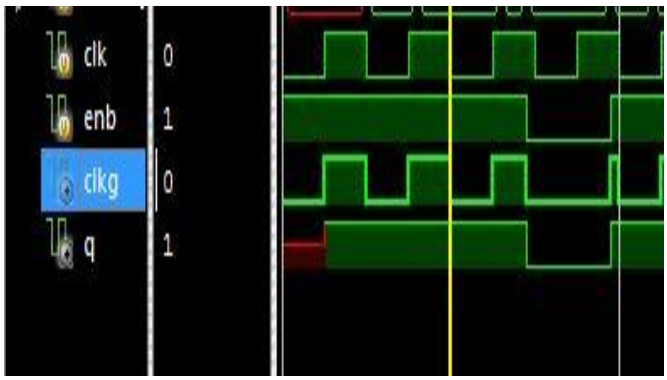

Figure 6. Overcome from the glitches

Disadvantage of latch based clock gating

In latch based clock gating implementation is easy but it having high clock skew rate.

C. FLIP FLOP BASED CLOCK GATING

In flip flop based clock gating, the d flip-flop is used in the place of latch [3][4]. By using flip-flop clock skew is more manageable.

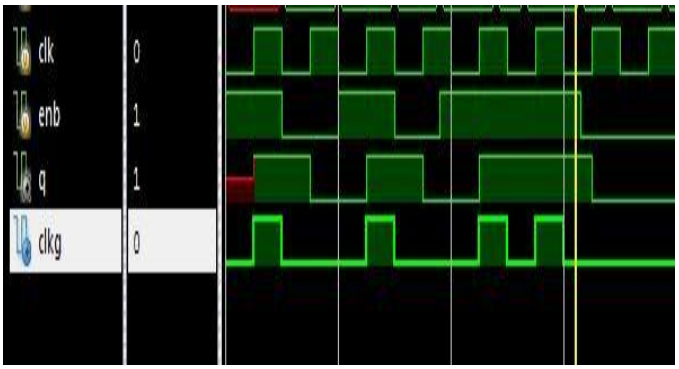

Figure7. The clock skew more managleble

D. NEW APPROACH CLOCK GATING

In this technique, using a flip-flop circuit in such a way that even target device clock is ON, the controlling device clock is OFF [3][4].

It works when input signal "ENB=1" and "GEN=0" then XOR will produce "X=1" for first clock generation logic that generates a clock for the flip-flop. In the first clock the AND gate which have a global clock as input to the other input of AND gate. The logic will generate a clock pulse, which drives to controlling flip-flop when "X=1". The next clock pulse, "GEN=1" in second clock generation logic which is OR gate which has Q and global clock at its input. And when "Q=0", it generates clock pulse that goes to target device [2][3]. Since "GEN=1" the XOR will produce "X=1". Thus OR will produce at CCLK, constant low until "ENB=0" this way GCLK will be running and CCLK will be at constant 0. This states that the means OFF will hold its state without switching [3][4].

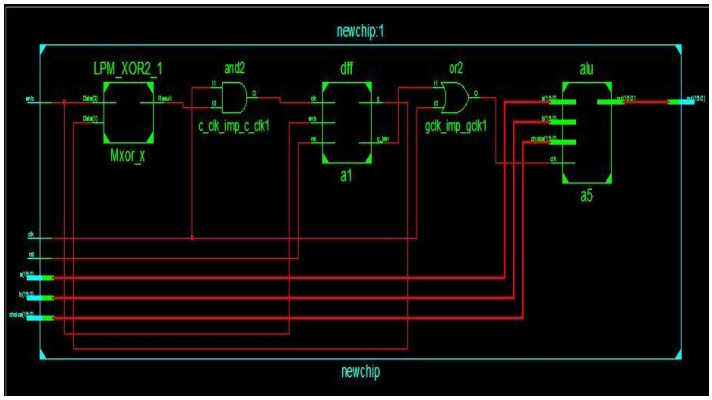

Figure 8. Top level design of new approach clock gating

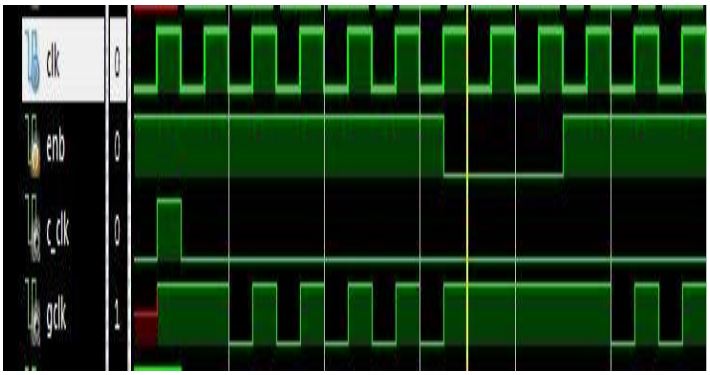

Figure9. Simulation of gclk holds the state

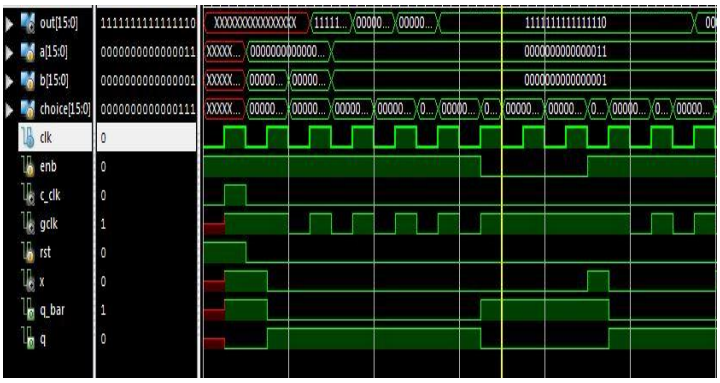

Figure 10. Simulation of new approach design

RESULTS

The power consumption results of the mentioned clock gating design.

Table1. Comparison table for power consumption through clock gating

	DYNAMIC POWER (W)	STATIC POWER (W)	TOTAL POWER (W)
LATCH FREE	11.135	0.114	11.249
LATCH BASED	11.121	0.114	11.235
FLIP-FLOP BASED	2.381	0.085	2.467
NEW APPROACH	1.458	0.084	1.542

CONCLUSION

In this paper, the four different clock gating techniques are done fsrom power saving point of view. The first one AND gate or latch free gating technique is done in which the glitches are seen in its simulation. Then, the design is made by taking a latch which removes the glitches but having high clock skew. The flip-flop clock gating is more manageable for controlling skew rates. The new approach clock gating is most suitable design for reducing the power consumption as it not only gated the clock on controlling device but also gated the clock for targeting device. It saves more power than other previous clock gating design. The new approach design fulfilled all the parameters that we want. It gated the clock not only to the target device but also the controlling device and showing the low power consumption in all design made in this paper

REFERENCES

[1]. Harpreetsingh, Dr. Sukhwinder Singh "A Review on clock gating methodologies for power minimization in VLSI circuits. International journal of scientific engineering and applied science volume 2, issue-1, January.2015.

[2]. V. Prasanth, p. Srisuresh"design and implementation of low power 16-bit ALU using clock gating". International journal of latest trends in engineering and technology vol.3, issue September 2013.

[3]. Vandana Prajapati, Uday Panwar "comparative analysis of existing clock gating ALU". International journal of scientific and research publication, vol.6, issue 5 may 2016

[4]. Jagrit Kathuria, M. Ayoubakhan and are nor "A review of clock gating techniques. MIT international journal of electronics and communication engineering vol.1, no. 2 august 2011 pp 106-114.

[5] M. Devendra, m. Naresh "clock gating based low power ALU design". International journal of science and research ISSN vol-4, issue 8 august

