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Fundamentals of Reversible Logic Gates and Their Applications

Piyush Singh
M. Tech, Dept of ECE, IEC College of Engineering and Technology, U.P., India
Singhpiyush999@gmail.com

Abstract: In current time, reversible logic gates are being used very fast due to its ability to design a more complex circuit with less power dissipation. Power consumption is the main factor in low-power VLSI design. Reversible logic gates reduce power in a big amount by eliminating the power loss during the loss of one bit of data in simple operations during conventional logic gates. The main purpose of this paper is to provide fundamentals of few reversible logic gates, the comparison between their operations and their applications.

Keywords: Reversible Logic, Power Dissipation, Reversible Gates, Quantum Cost, CMOS.

1. INTRODUCTION

In digital design, there are many logic gates being used in large numbers. But in current time power consumption is the main factor, which is taken very seriously. All the simple logic gates are reversible. According to Launderer's principle, during the loss of one bit of data, it will dissipate kT*ln2 joules in form of energy, where k (1.38x10 -23 J/k) is Boltzmann's constant and T is the absolute temperature in kelvin [1].

IN 1973, Bennett mentioned that if data is lost in logic operation it can be recovered from output by using reversible logic circuits [2].In combinational or irreversible logic circuits, if once data is lost, cannot be recovered. This problem has been removed in reversible logic designs [3].

According to Moore's law, after every eighteen months, a number of transistors will be doubled. Therefore the amount of energy dissipation will grow exponentially. In this case, reversible logic is much effective to reduce a large amount of power dissipation. In reversible logic design, there is k no of output fork no of inputs. This advantage of reversible circuits over combinational circuits makes it more efficient. If anyhow once data is lost you can easily determine in reversible logic. We can also determine its input combinations by analyzing its present outputs. So this is called reversible. Energy dissipation can be removed if design behaves as information-lossless. Fanout is increased and design formed with feedback. It has wide applications in low-power CMOS design, DNA technology, Quantum computing, and nanotechnology.

2. BASIC DEFINITIONS REVERSIBLE LOGIC

A. Reversible function

An output function F (m_1, m2…….m) of m number of variables with n number of input variables is said to be reversible if:

(a)The number of input variables is equal to a number of output variables.

(b)Every input pattern should make unique output pattern.

In other words, reversible function output pattern should be a permutation of its input.

B. Reversible logic gate
In any reversible logic gates, if m, n are numbers of input and output respectively then m must be equal to one. We can get inputs with the help of available output and output with the help of input.

C. Constant input
It means that in m number of inputs, few or one input set at either 0 or 1.But there should be a minimum number of constant inputs.

D. Garbage output
This refers to numbers of output added to make a function of m input and n output reversible or garbage output is a number of output that is not used in operation. Constant input is a number of the input set as constant, this way we find a relation between constant input and garbage output [4, 5].

Input + constant input = output + garbage output

E. Quantum cost

This refers to the cost of the circuit in terms of cost of primitive gates(1*1 or 2*2) .the cost of primitive gates starts with 2*2.The cost of the 1*1 primitive gate is 0 and cost of any 2*2 primitive gate is 1[6].

F. Flexibility

Flexibility refers that given reversible logic how efficient to perform different functions [7].

G. Gate level

Gate level refers to a number of level in a circuit to realize a function.

H. Density of circuit

Density in the circuit is a number of operation involved to realize a function e.g.: AND, OR and EXOR.

I. Design constraints

Design constraints of reversible logic gates are given below.

(1)There should be a minimum quantum cost in the reversible logic gate.

(2)This should not allow fan-outs.

(3) There should be minimum garbage output and minimum constant input.

(4)There should be minimum gate level and complexity.

3. BASIC REVERSIBLE GATE DEFINITION

1. Feynman gate
Feynman gate is 2*2, so its quantum cost is 1.Input is f (A, B) and output is f (P, Q). The outputs are defined by P=A, Q=A⊕B. This gate is used to get a copy of output [9].

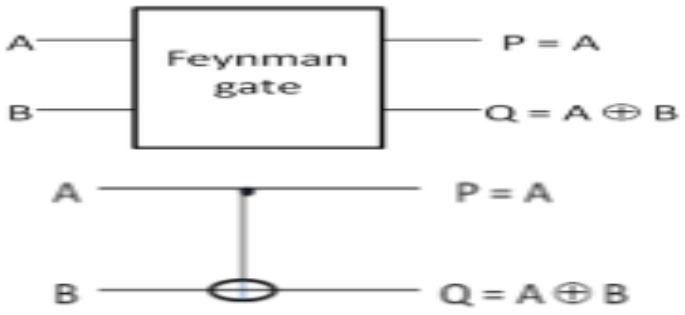

Figure 1: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1: Truth table of Feynman gates

2.Double Feynman gate(F2G)

It is 3*3 and its quantum cost is 2.The input and output vector is given by I(A, B,C) and O(P, Q,R)respectively. The outputs are defined by P = A, Q=A⊕B, R=A⊕C [10].

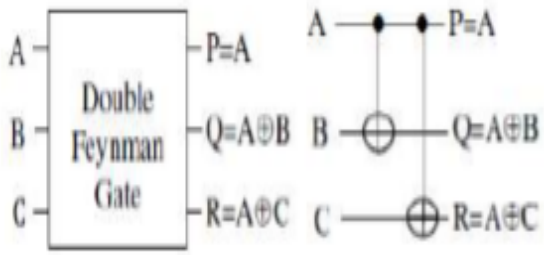

Fig 2: Double Feynman Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table 2: Truth Table of Double Feynman Gate

3. Toffoli gate

It shows 3*3 Toffoli gate. It's quantum cost is 5. The input and output vector is given by I(A, B,C) and O(P, Q,R)respectively. The outputs are defined by P=A, Q=B, R=AB⊕C [11].

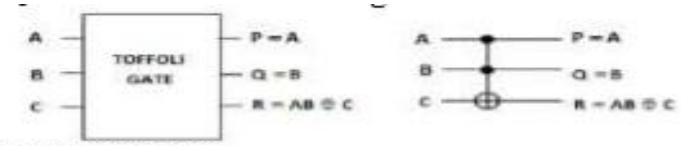

Fig 3: Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 3: Truth Table of Toffoli Gate

4.Fredkin Gate

It shows 3*3 Fredkin gate .It's quantum cost is 5. The input and output vector is given by I(A, B,C) and O(P, Q,R)respectively. The output is defined by P=A, Q=A′B⊕AC, and R=A′C⊕AB[12].

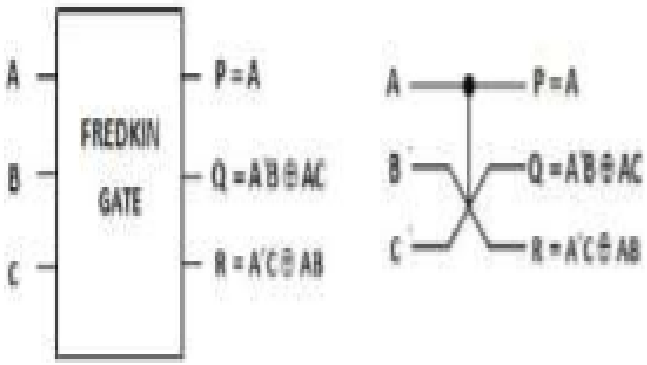

Fig 4: Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 4: Truth Table of Fredkin Gate

5. Peres Gate

It shows 3*3 Peres gate. It's quantum cost is 4. The input and output vector is given by I(A, B, C) and O(P, Q, R)respectively.The output is defined by P = A, Q = A⊕B and R=AB⊕C[13].

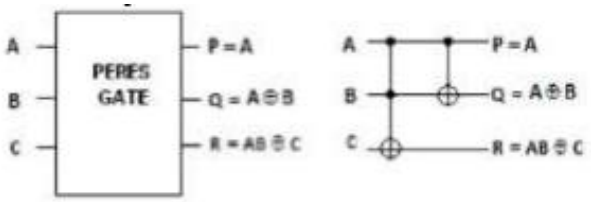

Fig 5: Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 5: Truth Table of Peres Gate

6. TSG Gate

It shows 4*4 TSG gate. It's quantum cost is 4. The input and output vector is given by I(A, B,C,D) and O(P, Q,R,S)respectively. The output is defined by P = A, Q = A'C'⊕B', R = (A's'⊕B') ⊕ D and S = (A's'⊕B').D⊕ (AB⊕C)[14].

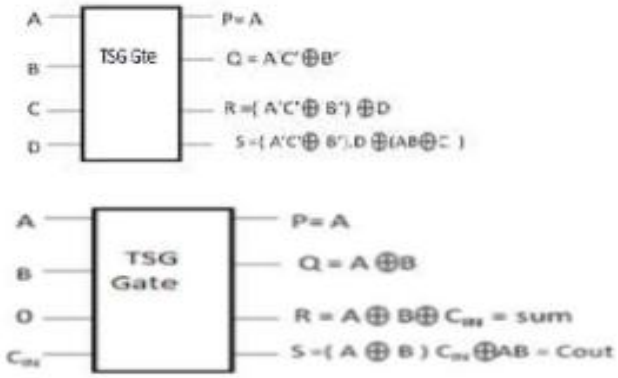

Fig 6: TSG Gate

7. Sayem Gate

It shows 4*4 Sayem gate. Its figure and function is given below.

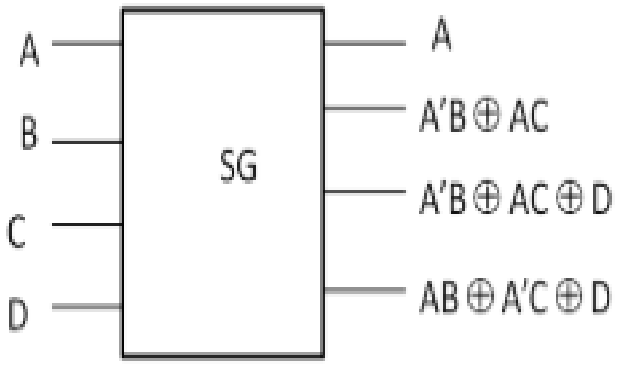

Figure 7: Sayem Gate

4. COMPARISON AMONG REVERSIBLE GATES

The difference among types and their quantum cost is given in following table [15].

Table 6

Reversible gates	Quantum cost	Types
Feynman gate[23]	1	2*2
Toffoli gate[24]	5	3*3
Fredkin gate[6]	5	3*3
Peres gate[7]	4	3*3
TSG gate[25]	4	4*4
URG gate[26]	unknown	3*3
System gate[27]	unknown	4*4
TR gate[26]	6	3*3
NFT gate[26]	5	3*3
BJN gate[26]	5	3*3
MTSG gate[25]	6	4*4
BME gate[26]	5	4*4
Sayem gate[13]	unknown	4*4
VB-1 gate[28]	unknown	4*4
VB-2 gate[28]	unknown	4*4
MKG gate[29]	unknown	4*4

5. APPLICATIONS OF REVERSIBLE LOGIC GATES

The application of reversible logic gates is given following.

1. Computer security.
2. Transaction processing.
3. Field Programmable Gate Arrays (FPGAs) in CMOS technology.
4. Computer graphics.
5. The design of low power arithmetic and data path for digital signal processing (DSP).
6. Low power CMOS.
7. Quantum computer.
8. Nanotechnology.
9. Optical computing.
10. DNA computing.
11. Computer graphics.
12. Communication.

6. CONCLUSION AND FUTURE SCOPE

This paper refers basic reversible logic gates with their literature, function, building block and table. This works highly in the field of low power CMOS, computer security, DNA technology, and many other research oriented fields. This paper can be extended further in the development of advanced work of digital design.

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