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Design and Verification of MPSOC on FPGA with Built-In Self Test

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Abstract: ***Multiple Processor System on Chip (MPSoC) which uses multiple processors mainly used in embedded applications due to their high processing speed and low power consumption. This paper focuses on the design and implementation of MPSoC on FPGA. Multiple single processors are interconnected by shared bus. This paper also provides a technique to solve a major challenge of handling faults in its main components i.e. processors and interconnect with built in test structure on every processor. By using this testing structure the faults occurred in processing elements (PE's) during the communication between the master and slave can be identified automatically. The functionality is analyzed and verified using Questasim and Quartus tool. The output of the proposed model is compared with MPSoC architecture without a testing structure to estimate the functionality improvement.***

Keywords: MPSoC, BIST, Shared bus, Fault detection, Quartus, Questasim.

I. INTRODUCTION

An MPSoC is a system on a chip that incorporates most or all the components necessary for an application – that uses multiple programmable processors as a system component. It has emerged in past decade as an important class of Very Large Scale Integration (VLSI) system. MPSoC's are widely used in networking, communication, signal processing and multimedia among other application.

With increasing device sizes and decreasing component sizes, the number and types of defects that can occur during manufacturing increase drastically, thereby increasing the cost of testing. Due to the growing complexity of VLSI devices and system PCBs, the ability to provide some level of fault diagnosis (information regarding the location and possibly the type of the fault or defect) during manufacturing testing is needed to assist Failure Mode Analysis (FMA) for yield enhancement and repair procedures. This is why BIST (Built In Self Test) is needed.

BIST can partition the device into levels and then perform testing. It offers a hierarchical solution to the testing problem such that the burden on the system level test is reduced. The same testing approach could be used to cover wafer and device level testing, manufacturing testing as well as system level testing in the field where the system operates. Hence, BIST provides for Vertical Testability.

In MPSoC architecture, homogeneous processors are considered as masters. It consists of a controller which includes the program counter, adder, multiplexer, accumulator, ALU and data path which includes instruction memory and read memory. The processor is the active part of the computer which does all the work of data manipulation and decision-making. The data path is the hardware that performs all the required operations. The controller is the hardware that tells the data path what to do, in terms of switching, operation selection, data movement between ALU components, etc.

Here memory is used as slaves. The information in the processor is randomly accessed by these memories. The communication between the master and slaves is done through shared bus interconnect. The shared bus architecture consists of arbiter, decoder, and a multiplexer. Arbiter decides which request signal should access the memory based on priority. The decoder decodes the address sent by the master and control for transaction goes to the memory. The multiplexer provides grant signal.

This paper is organized as follows. Section II discusses literature survey. Section III describes the existing work of MPSoC architecture and BIST testing structure. The proposed model of MPSoC architecture with built-in testing structure is discussed in section IV. The FPGA prototyping and experiment results will be presented in section V. Finally, conclusions are drawn.

II. LITERATURE SURVEY

The multiprocessor system-on-chip (MPSoC) uses multiple CPUs along with other hardware subsystems to implement a system. A wide range of MPSoC architectures has been developed over the past decade. "Multiprocessor System-On-Chip (MPSoC) technology" surveys the history of MPSoCs to argue that they represent an important and distinct category of computer architecture [6]. It considers some of the technological trends that have driven the design of MPSoCs. It also surveys computer-aided design problems relevant to the design of MPSoCs.

Wayne Wolf et al. argued that MPSoCs constitute a unique branch of evolution in computer architecture, particularly multiprocessors, that is justified by the requirements of these systems: real-time, low-power, and multitasking applications. Thus, in this paper, the authors presented a short history of the MPSoCs as well as an analysis of the driving forces that motivate the design of these systems. It also uses this opportunity to outline some important computer-aided design (CAD) problems related to MPSoCs and describe previous works on those problems.

An MPSoC FPGA prototype based on hierarchy bus using 4 ARM processor cores was presented in "Design of a Hierarchy-Bus Based MPSOC on FPGA". Wei Zhang et al. proposed a platform with the hierarchy-AHB bus as the communicate network in order to minimize the contention of a shared bus [5].

The basic concept of BIST involves the design of test circuitry around a system that automatically tests the system by applying certain test stimulus and observing the corresponding system response. Because the test framework is embedded directly into the system hardware, the testing process has the potential of being¬ faster and more economical than using an external test setup [4].

The basic architecture of BIST includes Test Pattern generator (TPG), Circuit Under Test (CUT) and Output Response Analyzer (ORA) and BIST controller is explained in [1][3][4].

Susha C Baby et al. have illustrated an implementation of BIST logic using VHDL [4]. LFSR is used as a pseudorandom sequence generator. Signature analysis is used to make verification of the circuit. Signature mismatch with the reference signature means that the circuit is faulty. However, there is a small probability that the signature of a bad circuit will be the same as a good circuit. When longer sequences are used, the signature analysis gives high fault coverage.

The fault coverage that we obtain for various fault models is a direct function of the test patterns produced by the Test Pattern Generator (TPG) and applied to the CUT. [3] Presents an overview of some basic TPG implementation techniques used in BIST approaches.

The replacement of the test pattern generator with low transition test pattern generator gives low power result because of the decrease in a number of transitions in the pattern generation [1].

III. EXISTING METHOD

The increasing system resources available on Field-Programmable Gate Arrays (FPGA) enable the integration of complex system on one programmable chip. [12] The paper focuses on the design and implementation of a hierarchy-bus based Multi-processor System-on-Chip (MPSoC) integrating 4 ARM processors on FPGA.

The MPSoC platform is based on Symmetric - Multiprocessor-like (SMP) architecture, and has shared memory and semaphore memory controller to enable the atomic operation to shared memory. To avoid shared memory contention and bottlenecks, every processor has its own local memory. The hardware architecture of the platform is depicted in Fig.1.

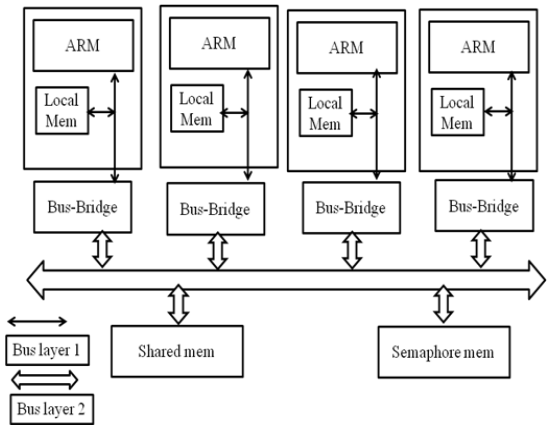

Fig.1 MPSoC Architecture

The two arbitration mechanisms considered by Akash Kumar et al. are static order and Round Robin (with skipping) [2].

- Static order: Actors - as defined in SDF model – are repeatedly executed in a strict order specified by a predefined list. If an actor is not ready (its input data has not yet arrived) to execute, the processor will halt and wait.
- Round Robin: Actors are repeatedly executed in an order specified by a pre-defined list. If an actor is not ready to execute, the arbiter will skip the actor and proceed to the next actor in the list.

The author observed that round robin has a lower run-time and design-time overhead and also handles dynamism in the tasks more efficiently. When a new job arrives in the system, round-robin has a little overhead for reconfiguration. It, however, suffers, heavily from the lack of performance predictability in the design - one of the most important requirements for a resource manager in an MPSoC. For proposed system, round-robin is preferred as the basic arbitration mechanism and build upon it in order to realize a resource manager.

IV. PROPOSED SYSTEM

The given block diagram is the software prototype design of the MPSoC architecture with Built-in self-test. The main component of the software prototype model is processor and testing structure. The function of the system is the fault identification of processor. The general block diagram for MPSoC architecture with BIST is shown in Fig.2. The four homogeneous processors are built to act as master of MPSoC. It will perform the desired operation based on the inputs given.

The actual response of processor is compared with the desired response generated by BIST. Based on faults occurred, the request signal is provided to the arbiter, which is present in the shared bus architecture. It will decide priority and provide grant signal to the respective slave i.e., RAM memory.

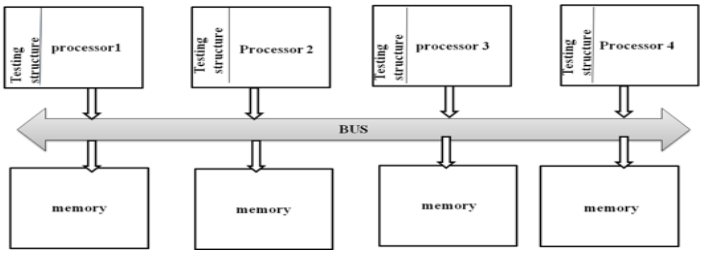

Fig.2 General Block Diagram

The low power BIST structure is modeled within the processor to outweigh the disadvantages like area consumption and other added risk. The designing of low power BIST can be achieved by using a low transition test pattern generator. The replacement of the test pattern generator with low transition test pattern generator gives low power result because of the decrease in a number of transitions in the pattern generation. The dynamic power of a circuit mainly depends on the switching activity of the output. The switching activity can be reduced by improving the correlation between the bits of successive outputs. One way to improve the correlation between the bits of the successive vectors is to avoid frequent transitioning of the logic levels (1→0 or 0→1) of the primary inputs. A serial input signature register can only be used to test logic with a single output. The idea of a serial input signature register can be extended to multiple-input signature register (MISR). There are several ways to connect the inputs of LFSRs to form a MISR. Since the XOR operation is linear and associative, (A xor B) xor C = A xor (B xor C), as long as the result of the additions are the same then the different representations are equivalent.

The signature analysis is the technique to analyze the obtained signature from MISR output with the expected output. For this purpose, a 32-bit comparator is used to compare the obtained signature with the expected signature. Whenever the unexpected output is obtained, then there will be a fault in the circuitry and the output shows that circuit is faulty. By considering the output of this signature analyzer, the fault is to be detected.

V. EXPERIMENTAL RESULTS

The proposed system can be verified using Questasim tool and results are simulated. The software code is developed for 32-bit processor and 1024 bytes RAM. Test Pattern Generator (TPG), LFSR, MISR are coded for low transition test pattern generator. The verification results obtained using Questasim tool is shown in Fig.3. The functionality is analyzed by implementing on Altera board (cyclone IV) using Quartus tool.

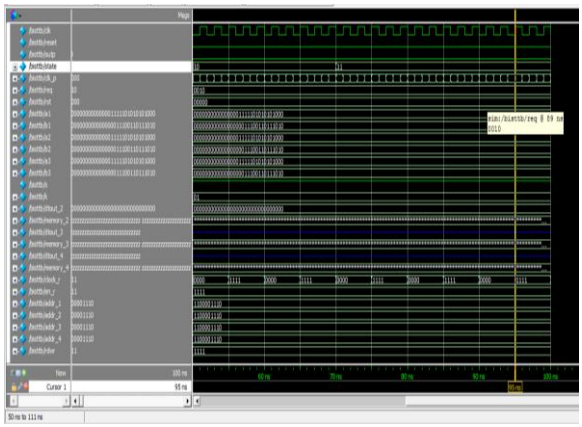

Fig.3. Simulation Result

CONCLUSIONS

An MPSoC FPGA software prototype based on shared bus using 4 homogeneous processor cores with fault identifying structure was presented and simulated. From the comparison made between the results of MPSoC without built-in test structure and proposed model having BIST, we can get the conclusion that the platform works more efficiently with fault detection. As far as the future work is concerned, the prototype can be extended with fault recovery technique.

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