INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume3, Issue2)
Available online at www.ijariit.com

Design & Optimization of Finfet Based Schmitt Trigger Using Leakage Reduction Techniques

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Abstract: ***In this proposed work we are applying valuable power gating schemes to FinFET based Schmitt trigger to enhance its performance by reducing the leakage current in standby mode (off-state mode). The power gating schemes like Sleep Transistor approach and Multi-Threshold CMOS (MTCMOS) and Double-Threshold CMOS (DTCMOS) have been analysed and simulated which shows the tremendous reduction in the leakage current thus increasing the stability of the design. In this paper, different consecutive designs of PULL-UP and PULL-DOWN networks of NMOS and PMOS are applied to FinFET based Schmitt trigger one after another. Due to this treatment of PULL-UP and PULL-DOWN network, controlled voltage supply is obtained and the current driving capability of the design is increased, the hence less Gate leakage current is formed. This provides the motivation to explore the design of low leakage FinFET based Schmitt trigger. Simulation is performed on the cadence virtuoso tool in 45nm technology and simulation results revealed that there is a significant reduction in leakage current for this proposed design.***

Keywords: ***MTCMOS, DTCMOS, Sleep Transistor, Leakage Current, Low Power, Leakage Reduction.***

INTRODUCTION

With each technology generation as the device, the dimension is scaled down the complexity and performance estimation of the VLSI ICs is increased. The present scaling scenario exploits the fact that at sub-nanometer regime leakage of current in standby mode will become a major limiting factor to present available technologies. Even for the idle circuit Metal Oxide Semiconductor (MOS) devices will not able to properly turn-off, as a result of which "off-state current" will flow through the circuit. The major sources for this off-state current: (1) Sub-threshold leakage, (2) Gate leakage current and (3) Band-to- Band tunneling leakage current. In order to maintain the dynamic power dissipation under the limit, supply voltage V_{dd} has to be scaled down. This results in maintaining the high drive current and performance. In this paper, we propose three circuit techniques to control the off-state current.Due to this treatment of PULL-UP and PULL-DOWN network, controlled voltage supply is obtained and the current driving capability of the design is increased, the hence less Gate leakage current is formed.

CIRCUIT DESCRIPTION OF FinFET BASED SCHMITT TRIGGER

Schmitt Trigger is a comparator that compares the input signal with some certain chosen threshold value. In this circuit, when the input goes higher than the certain chosen higher threshold value, the output goes high. Similarly, when the input goes lower than lower chosen threshold value, the output goes low. With the application of planar technologies in Power- gating circuits, leakage power reduces up to a greater extent. By disconnecting the power rail when the design is not operating in standby mode, leakage

power became negligible. Fig. 1 shows the design of FinFET based Schmitt trigger circuit which is basically the cascade of two FinFET inverters. The output of the first inverter is the input for the second inverter which produces some output and that output is again positive feedback to the input section of the design.

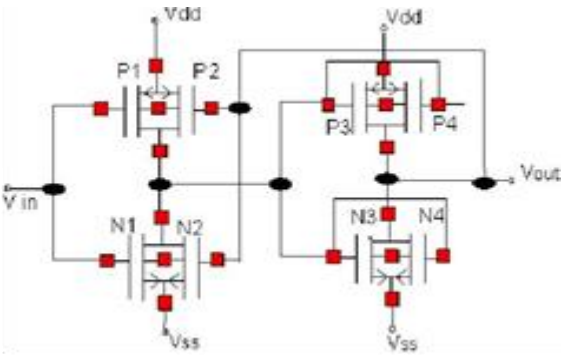

Fig. 1 FinFET Based Schmitt Trigger Circuit.

LEAKAGE REDUCTION SCHEMES

Leakage power dissipation in any VLSI circuit can be alleviated when the standby power supply is turn off. For this reason, sub-circuit is subjected to connect by one PMOS and one NMOS transistor to form virtual power supply and a virtual ground. But the above scheme is for the theoretical purpose only. As NMOS transistor offers lower on-resistance than PMOS transistor practically single NMOS transistor is used.

A. Sleep Transistor Approach

The functioning of sleep transistors can be understood as in the active m mode the sleep transistors are ON while in the standby mode sleep transistors are OFF. Thus the circuit works normally in active mode and saves power in standby mode by cutting the power supply to the circuit. Extra power can be saved by taking the smaller width of sleep transistors. Most commonly used power gating methods are Dual VCMOS or MTCMOS (Multi-Threshold) techniques. In the above-mentioned techniques, low V_{TH} transistors are used to design the logic circuit while high V_{TH} are used for sleep transistors. The size of sleep transistor should be carefully chosen as it can result to decrease voltage drop across it and can also increase the threshold voltage level of pull-down network due to the body effect. This will cause an increment of delay in the circuit while going from high to low transition. This problem can be resolved by using larger sleep transistors but this will cost more dynamic power for switching the circuit ON to OFF (vice-versa) and area overhead. One transistor for each logic block requires a large area and leads to power overhead. So for this, we can use only one transistor f or each group of logic gates which can be seen in F ig.5. In this technique, a sleep transistor is connected between virtual ground (ground of logic circuit) and actual ground which cuts off the leakage path of the circuit from the ground. The main idea of this technique is that the application of the conventional power gating technique to the power supply can cause the virtual ground rail to increase its value almost close to the actual supply voltage V_{dd} which can restrain the leakage current hence reducing the leakage power. A conventional power gating technique is shown in Fig.5 in which sleep transistor is turned ON in saturation during the transition from sleep mode to active mode.

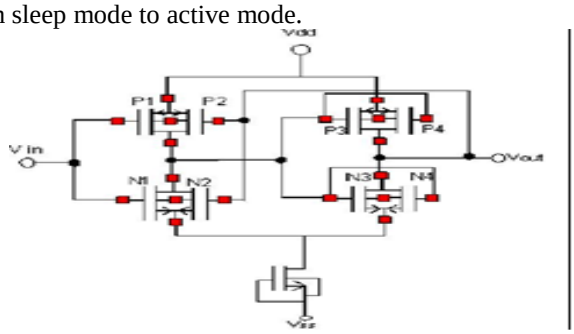

Fig .2 FinFET Based Schmitt Trigger Using Sleep Transistor Approach.

SIMULATION RESULTS

(SLEEP TRANSISTOR)

Leakage current waveforms using Sleep Transistor
Approach from 0.6 to 1 volts

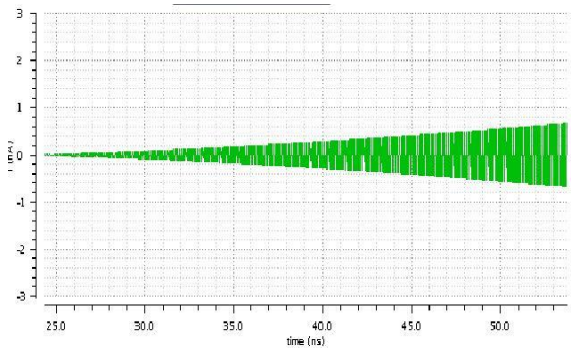

Fig. 4 Leakage Current Waveform of FinFET Based Schmitt triggers using sleep transistor technique at 0.6 volt

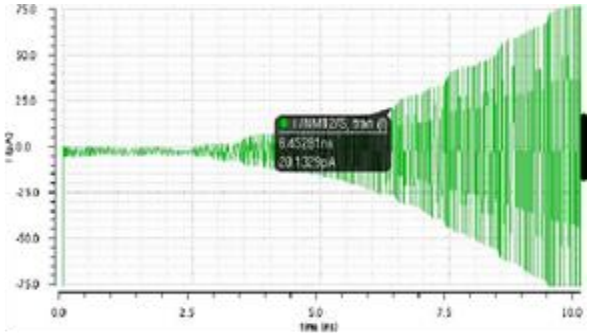

Fig. 5 Leakage current waveform of FinFET based Schmitt trigger using sleep transistor technique at 0.7 volts.

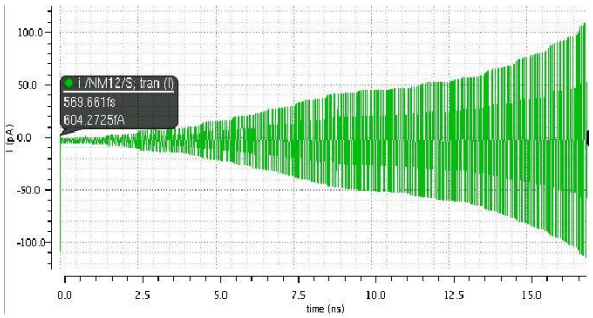

Fig. 6 Leakage current waveform of FinFET based Schmitt trigger using sleep transistor technique at 0.8 volts

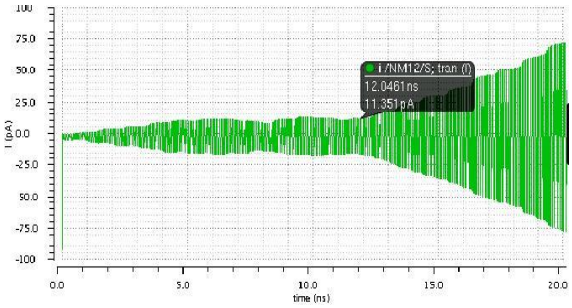

Fig. 7 Leakage current waveform of FinFET based Schmitt trigger using sleep transistor technique at 0.9 volts.

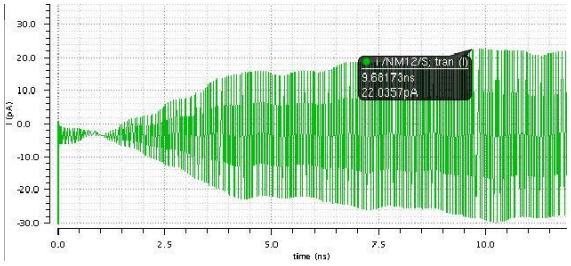

Fig. 8 Leakage current waveform of FinFET based Schmitt triggers using sleep transistor technique at 1.0 volts.

Leakage Current Achievement Using Sleep Transistor

Voltage (volts)	Leakage current (pA)
0.6	2.509
0.7	2.733
0.8	2.967
0.9	3.192
1	3.408

B. MTCMOS Technique

The leakage current is needed to be further reduced so another design has been implemented called Multi –Threshold CMOS or MTCMOS. This is shown in Fig. 3 With the use of high V_t sleep transistors which are the gateway of the power supply and ground to the low V_t logic block results in a decrease of the leakage power along with the overall power consumption in the circuit [10]. This is built by incorporating two sleep transistors in the FinFET based Schmitt Trigger circuit. However when the input sine pulse is applied and the sleep signal become low than transistors with sleep and sleep bar inputs of high threshold voltages are used which get turn ON in active mode and connect the power supply and ground to the low threshold logic block [12]. With the addition to this in Standby mode, the sub-threshold leakage current conduction path cut OFF effectively to the low V_t circuit. The sub-threshold leakage during the standby mode is reduced by high threshold transistors through disconnecting the low threshold transistors from direct connection to the power supply and ground while in active mode high threshold transistors are turned ON causing low threshold transistors to implement the operation by using virtual supply and virtual ground. This type of implementation shows drastically changed parameters as illustrated in simulation results.

SIMULATION RESULTS

(MTCMOS TECHNIQUE)

Leakage current waveforms using MTCMOS Technique Approach from 0.6 to 1 volts

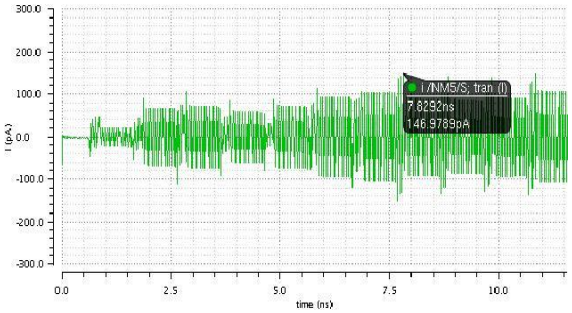

Fig. 9 Leakage current waveform of FinFET based Schmitt Trigger using MTCMOS technique at 0.6 v

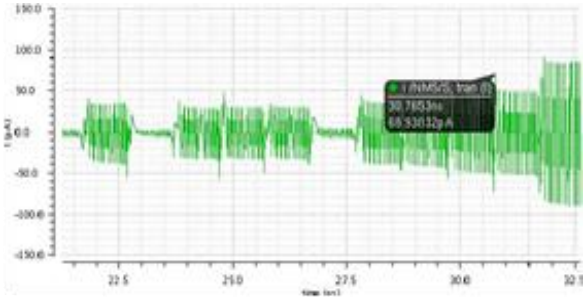

Fig.10 Leakage current waveform of FinFET based Schmitt trigger using MTCMOS technique at 0.7 volts

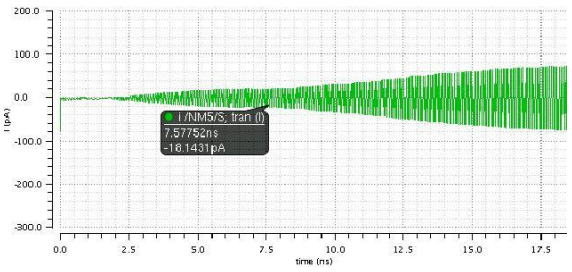

Fig.11 Leakage current waveform of FinFET based Schmitt trigger using MTCMOS technique at 0.8 volts

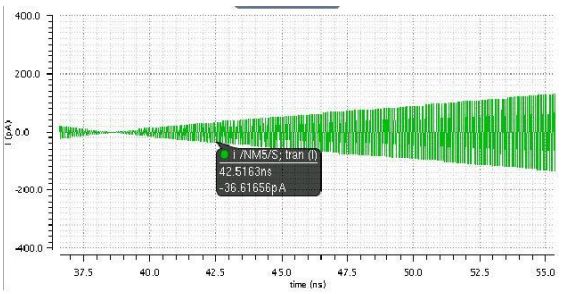

Fig.12 Leakage current waveform of FinFET based Schmitt trigger using MTCMOS technique at 0.9 volts

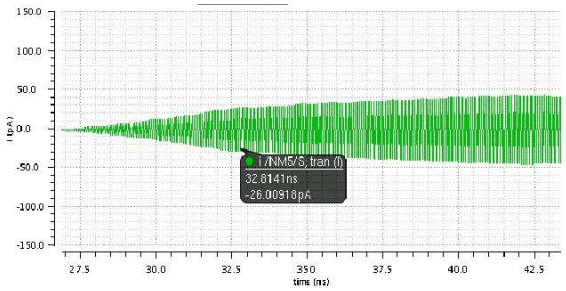

Fig.13 Leakage current waveform of FinFET based Schmitt trigger using MTCMOS technique at 1.0 volts

DTCMOS Technique

DTCMOS is an implementation of robust source coupled technique i.e. Dynamic threshold source coupled logic with a push-pull amplifier at the output stage. In dynamic threshold MOS (DTMOS) topology, the gate of the transistor is connected to its substrate. Therefore, the substrate voltage continuously changes with the gate voltage of the transistor. The change in the substrate voltage dynamically alters the threshold voltage. The DTMOS behaves exactly like a normal transistor in the OFF state i.e. VIN=VDD (VIN=0) for PMOS (NMOS). Both exhibit exactly same parameters such as off current, threshold voltage etc. However, in the ON state as a gate to source voltage (VGS) increases, the substrate to source voltage (VBS) also increases. This further decreases the threshold voltage of DTMOS transistor. The reduction in the threshold voltage is due to reduced body charges that increase the carrier mobility. This, in turn, lowers the effective normal field. All these effects collectively lead to a higher ON current in the DTMOS transistor

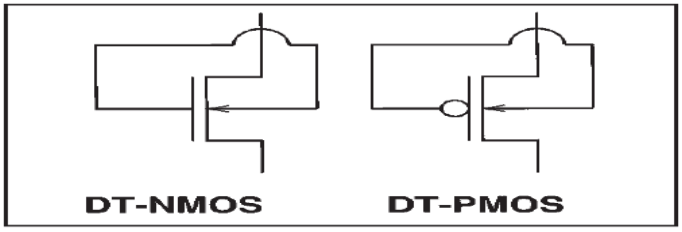

Fig: Circuit Symbol for DT-NMOS and DT-PMOS

CONCLUSION

We have analyzed a Sleep Transistor Approach and MTCMOS schemes to reduce the leakage current in FinFET based Schmitt trigger circuit. These power gating techniques offer reduced standby leakage, without any significant effect on the system performance. Due to better device features of FinFET based Schmitt trigger in low voltage operation these power-gating techniques are becoming a most promising for lower VDD operation in FinFET technologies. Implementation based on DTCMOS techniques has been proposed in this paper, we are getting faster operation speed with the low power voltage supply. All of these techniques used in the proposed work, the DTCMOS technique have shown improvement in terms of leakage power over remaining other two techniques. Noise Analysis is also performed over the FinFET based Schmitt trigger circuit.

ACKNOWLEDGMENT

The authors would like to thank cadence design system, Bangalore for offering 45nm VLSI Domain for simulation used in this work.

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