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Skew Minimization with Low Power for Wide Voltage Range Using Course Grain Technique

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Abstract: ***Skew is one of the most important parameter that decides the performance of the system. Though skews are reduced using two-stage(low and high voltage levels) serially connected power mode aware buffers(PMABs) using two power gating techniques-Fine grain technique at high voltage level and Coarse grain technique at low voltage level, the power consumption and area is large incase of fine grain technique. So, in the proposed system, coarse grain minimization is used at both stages which will effectively reduce power consumption and area. The course- grained approach implements the grid style sleep transistors which drive cells locally through shared virtual power networks. This approach is less sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller area overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the power gating transistor is a part of the power distribution network rather than the standard cell.***

Keywords: Coarse Grain Technique, Level up Shifter, Power Mode Aware Buffers, Power Gating, Power Minimization.

I. INTRODUCTION

Even though the two stage power mode aware buffers (PMABs) [1] reduces clock skew, power consumption becomes overhead. The two power gating techniques are used to reduce the power consumption of the aware buffers. Multi power mode designs are used to reduce power consumption but it makes the skew minimization part very difficult [2].Since the supply voltage is reduced to ultra-low voltage level [3], the range of voltage becomes wide [4]. The architecture of MPMAB [5] cannot efficiently eliminate the skew completely so, the two voltage stage PMAB architecture [1] is designed for wide voltage range multi power mode designs. In the low voltage stage, coarse grain Clock skew minimization technique is used. In the high voltage stage, Fine grain clock skew minimization technique is used. Comparing with Coarse grain technique, Fine grain technique requires more power consumption and also area.

In this brief, we propose a modification in the design. Both the low voltage and high voltage levels are designed using Coarse Grain clock skew minimization technique. This can more efficiently reduce power consumption and the area along with the clock skew. The two stage PMAB architecture overcomes the drawbacks faced by the MPMAB architecture [5] and also the use of Dynamic-Voltage-Scaling (DVS) controller [6] is avoided since the voltage is fixed. This two stage PMAB can completely reduce the skew along with the reduction of power consumption and area.

The Table I given below describes the clock latencies and the clock skew obtained when the multi power mode aware buffers (MPMAB) are used in the design.

TABLE I
CLOCK LATENCIES OF MPMAB BASED CLOCK TREE

Power Mode	Clock Latency (ns)		Clock Skew (ns)
	Domain PD1	Domain PD2	
Mode 1	0.70	0.75	0.05
Mode 2	9.30	9.35	0.05
Mode 3	6.30	6.60	0.30
Mode 4	17.70	18.00	0.30

II. DESIGN METHODOLOGY

a) POWER MODE AWARE BUFFER (PMAB)

The design methodology comprises of two parts.One is the PMAB architecture and the other one is the PMAB clock tree. The clock tree is used to provide, less clock skew. Thus the clock tree includes Level-Up-Shifters for converting low voltage to high voltage.

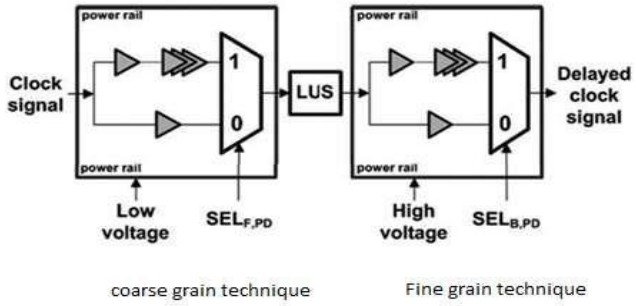

Fig.1. Two voltage stage PMAB architecture

The architecture includes front sub PMAB and back sub PMAB. The front part requires a low voltage supply and it consists of clock buffers to implement alignment delay. SELF,PD and SELB,PD are the selection signals for the multiplexers in the front and back sub PMABs. The values of SELF, PD, and SELB, PD are generated according to the power domains PD.

b) LEVEL UP SHIFTER (LUS)

The level-up shifter is used to shift the voltage level to high. It is used between two PMAB tree - structure. The topology in below fig 2 uses diode-connected PMOS transistors between the drains of M1 and M2. Each diode acts a current limiter to the PMOS pull-up devices. However, this design limits the output swing between *VDD* and *VTP*, without adding M7 and M8. The authors fix this by adding M7 and M8 at the drain of M3 and M4. M7 and M8 are controlled by *V*in and Vin b to pull the output to ground. When the input is 0, M4 could have a *VGS* other than 0 due to a voltage drop across M5. This could leave M4 in weak inversion, allowing a static current to pass through M8 and M4. The same is true when the input is high, but M5 and M7 are now creating a static current. Variation in the diode connected devices has a strong impact on the reliability of the solution. Our design uses a combination of circuit methods to ensure reliable, fast, and energy efficient operation. Specifically, we use sizing, threshold voltage selection, and diode-based voltage degradation to enable reliable conversion across variation and temperature. This brief combines several techniques to reduce the number of power supplies and extend the conversion range relative to existing sub-threshold level converters [7]

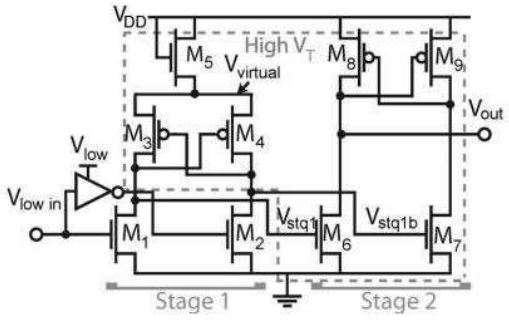

Fig 2. Level Up Shifter (LUS)

c) PMAB CLOCK TREE

Fig.3 shows the two-stage PMAB clock tree in which PMAB 1' and PMAB 2' makes the first stage and the second stage includes PMAB 1" and PMAB 2". Two power domains PD1 and PD2 for the two stages are used. Level Up Shifters LUS1 and LUS2 are inserted into the clock path for converting the voltage levels.

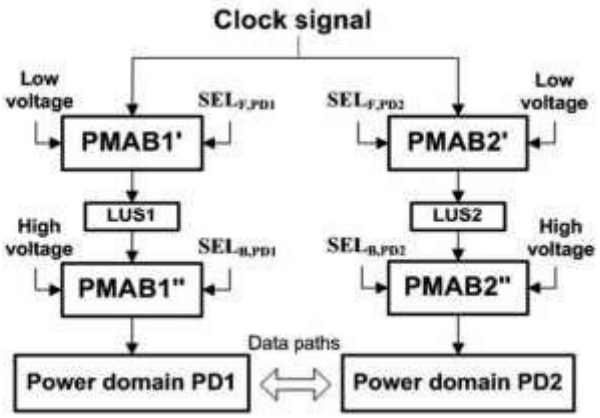

Fig 3. PMAB Clock tree structure

The Table II given below gives the clock latencies when the power mode aware buffers (PMAB) are used and also the clock skew is mentioned.

TABLE II
CLOCK LATENCIES OF TWO-STAGE PMAB CLOCK TREE

Power Mode	Clock Latency (ns)		Clock Skew (ns)
	Domain PD1	Domain PD2	
Mode 1	12.75	12.75	0.00
Mode 2	12.75	12.75	0.00
Mode 3	12.75	12.75	0.00
Mode 4	12.75	12.75	0.00

III. PROPOSED SYSTEM

Fig 4 shows the proposed architecture of two stages PMAB. In the proposed system, only the power gating technique used for the design differs. Power gating technique is the technique used for the reduction of power consumption.

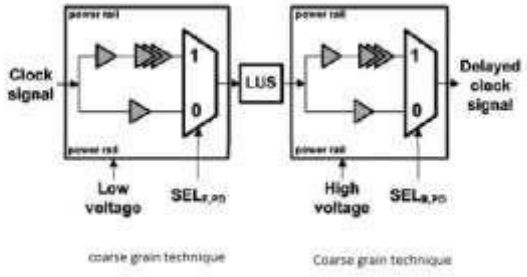

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Fig 4. Two stage PMAB architecture – Proposed System

a. POWER GATING

Power gating is the technique wherein circuit blocks that are not in use are temporarily turned off to reduce the overall leakage power of the chip. This temporary shutdown time can also call as "low power mode" or "inactive mode". When circuit blocks are required for operation once again they are activated to "active mode". These two modes are switched at the appropriate time and in a suitable manner to maximize power performance while minimizing impact to performance. Thus the goal of power gating is to minimize leakage power by temporarily cutting power off to selective blocks that are not required in that mode. Power gating effects design architecture more compared to the clock gating. It increases time delays as power gated modes have to be safely entered and exited. The possible amount of leakage power saving in such low power mode and the energy dissipation to enter and exit such mode introduces some architectural trade-offs. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is the other option. An externally switched power supply is a very basic form of power gating to achieve long-term leakage power reduction. To shut off the block for small interval of time internal power gating is
Suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. The output of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off. Two of the most critical parameters are the IR-drop and the penalties in silicon area and routing resources. Power gating can be implemented using cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach.

i. Fine Grain Power Gating Technique

Adding a sleep transistor to every cell that is to be turned off imposes a large area penalty, and individually gating the power of every cluster of cells creates timing issues introduced by inter- cluster voltage variation that is difficult to resolve. Fine-grain power gating encapsulates the switching transistor as a part of the standard cell logic. Switching transistors are designed by either library IP vendor or standard cell designer. The size of the gate control is designed with the worst case consideration that this circuit will switch during every clock cycle resulting in a huge area impact as well.

ii. Coarse Grain Power Gating Technique

The coarse-grained approach implements the grid style sleep transistors which drive cells locally through shared virtual power networks. This approach is less sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller area overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the power-gating transistor is a part of the power distribution network rather than the standard cell.

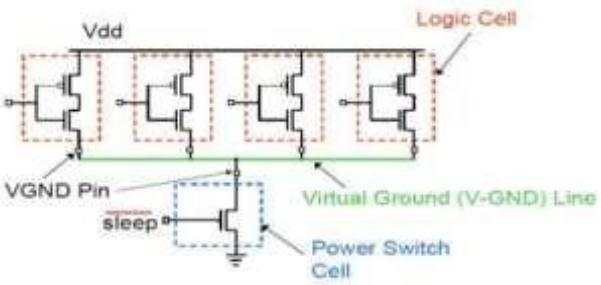

Fig 5. Coarse Grain Technique- block diagram

There are two ways of implementing a coarse-grain structure:

1) Ring-based
2) column-based

- **Ring-based methodology**: The power gates are placed around the perimeter of the module that is being switched-off as a ring. Special corner cells are used to turn the power signals around the corners.

- **Column-based methodology**: The power gates are inserted within the module with the cells abutted to each other in the form of columns. The global power is the higher layers of metal, while the switched power is in the lower layers.

Gate sizing depends on the overall switching current of the module at any given time. Since only a fraction of circuits switches at any point of time, power gate sizes are smaller as compared to the fine- grain switches. Dynamic power simulation using worst case vectors can determine the worst case switching for the module and hence the size. IR drop can also be factored into the analysis. Simultaneous switching capacitance is a major consideration in coarse-grain power gating implementation. In order to limit simultaneous switching daisy chaining the gate control buffers, special counters are used to selectively turn on blocks of switches

RESULTS

The below shown *Table III* gives the comparison of different Clock trees which includes the clock skew and power consumption. The proposed system can reduce the power even more and provides better skew minimization with low power consumption.

TABLE III
Comparison of Skew and Power of Different Clock Trees

	CONV		MPMAB		PMAB	
	Skew (ns)	Power (nW)	Skew (ns)	Power (nW)	Skew (ns)	Power (nW)
CKT1	0.30	5327	1.02	333	0.29	254
CKT2	0.30	5956	0.30	385	0.30	388
CKT3	0.30	3880	1.02	373	0.30	378
CKT4	0.27	6027	0.30	384	0.05	201
CKT5	0.29	3214	0.39	393	0.28	192
CKT6	0.30	5883	1.02	444	0.29	408
IND1	0.30	7514	0.78	935	0.30	504
IND2	0.30	482623	0.85	12671	0.30	10236
IND3	0.30	517200	0.50	14788	0.30	11849

CONCLUSION

In this brief, we propose a two stage PMAB architecture, in which both are designed using Coarse Grain power gating method which when compared with Fine grain technique, utilizes less power and area. This, in turn, helps in minimizing the skew with low power consumption and provides better performance. Different from the other techniques, the proposed system can produce better results and show improvement in the power consumption part.

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