INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact factor: 4.295
(Volume3, Issue1)
Available online at: www.ijariit.com

Design & Performance Analysis of Instrumentation Amplifier at Nanoscale

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Abstract:- In this research work, simulation and comparative analysis of Instrumentation Amplifier at different voltages. DC voltage gain is 133.4 dB, average power is 589 mW, bandwidth is 3.87 MHz have been computed using HSPICE Software at 0.5V. DC voltage gain is 77.84 dB, average power is 290mW, bandwidth is 164MHz have been computed using HSPICE Software at 1.5V. The proposed Instrumentation is efficient in medical applications due to high gain and high bandwidth. Instrumentation Amplifier based on CMOS has been designed and simulated using 32nm CMOS technology. In this design, care has been taken in selection of the values to maintaining the gain and bandwidth of the Instrumentation Amplifier.

Keywords – Instrumentation Amplifier, CMOS technology, Low voltage, Low power, Output resistance, Bandwidth. DC Gain.

I. INTRODUCTION

Instrumentation amplifiers are actually made up of 2 parts: a buffered amplifier using OP AMP1, OP AMP2 and a basic differential amplifier OP AMP3. The differential amplifier part is often essential when measuring sensors. A sensor produces a signal between its terminals. However, for some applications, neither terminal may be connected to the same ground potential as your measuring circuit. The terminals may be biased at a high potential or riding on a noise voltage. The differential amplifier rescues the signal by directly measuring the difference between the sensor's terminals.

The buffered amplifier OP AMP1 and OP AMP2 not only provides gain, but prevents the sensor resistance from affecting the resistors in the op amp circuit, and vice-versa. The realization of high speed and high accuracy Instrumentation Amplifier has proven. Optimizing the circuit design for both requirements leads to conflicting demands. The realization of high speed and high accuracy opamps has proven to be very challenging task. Optimizing the circuit design for both requirements leads to conflicting demands [1]. A single-stage folded cascode topology is a popular approach in designing high speed op-amps. Besides large unity gain frequency, it offers large output swing. However, it has limitation to provide high DC gain which is required for high settling accuracy. In 1990, Bult and Geelen proposed the folded cascode op-amp with gain boosting technique [3]. This technique help to increase the op-amp DC gain without sacrificing the output swing of a regular cascade structure [3]. The pushing up the doublet can raise stability problem [5], [6].

Advantages of Three Op-amp Instrumentation Amplifier

- The gain of a three op-amp instrumentation amplifier circuit can be easily varied and controlled by adjusting the value of Rgain without changing the circuit structure.
- The gain of the amplifier depends only on the external resistors used. Hence, it is easy to set the gain accurately by choosing the resistor values carefully.
- The input impedance of the instrumentation amplifier is dependent on the non-inverting amplifier circuits in the input stage. The input impedance of a non-inverting amplifier is very high.
- The output impedance of the instrumentation amplifier is the output impedance of the difference amplifier, which is very low.
- The CMRR of the op-amp 3 is very high and almost all of the common mode signal will be rejected.

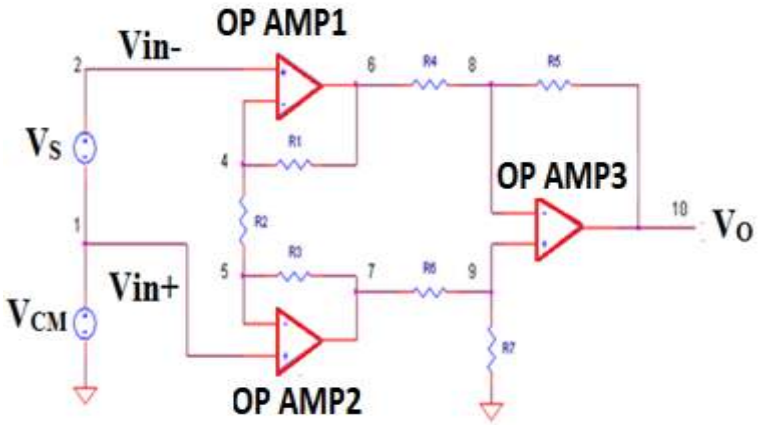

Figure.1-Proposed Instrumentation Amplifier

Simulated Data of Proposed Instrumentation Amplifier at 1.5 V

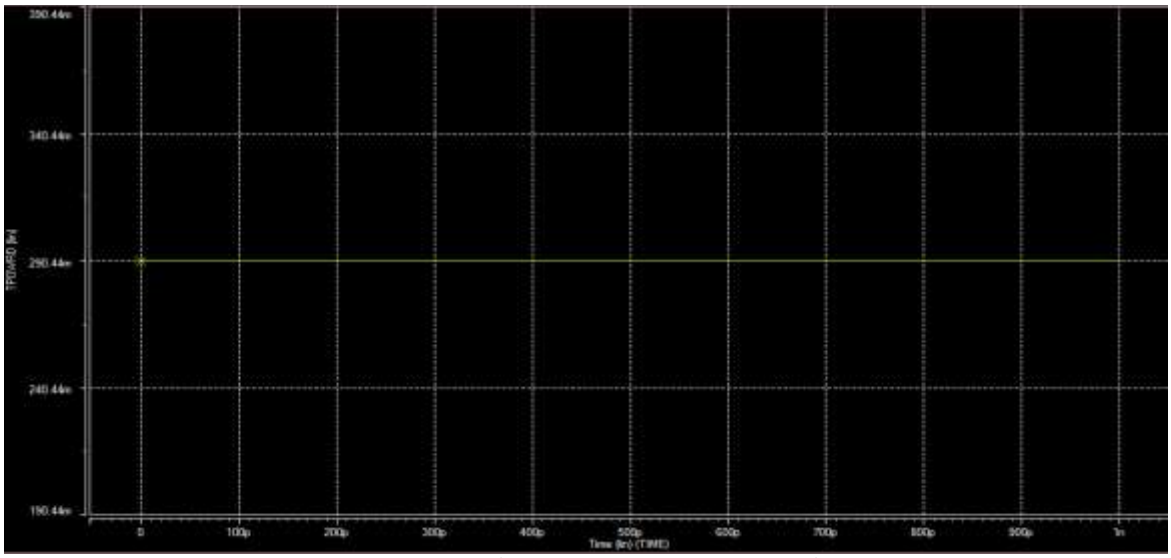

Figure.2-Average Power of Proposed Instrumentation Amplifier at 1.5V

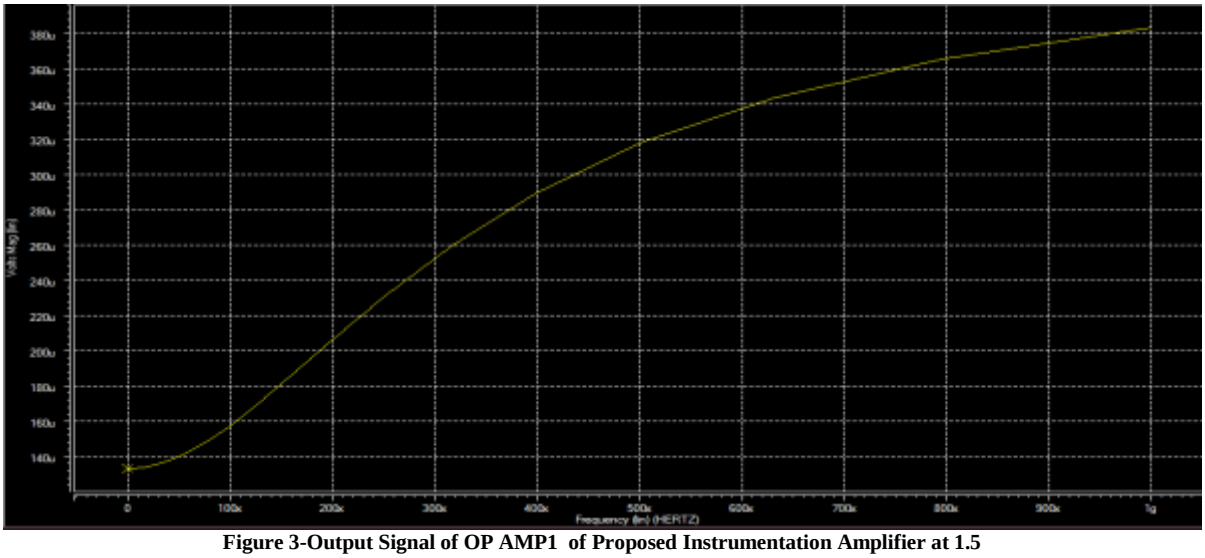

Figure 3-Output Signal of OP AMP1 of Proposed Instrumentation Amplifier at 1.5

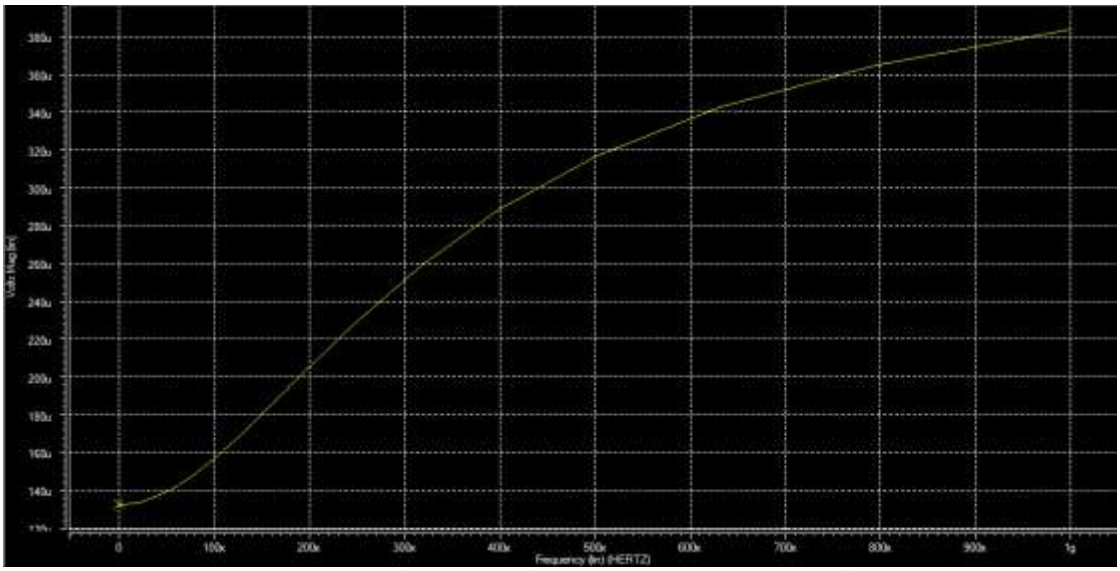

Figure 4-Output Signal of OP AMP2 of Proposed Instrumentation Amplifier at 1.5V

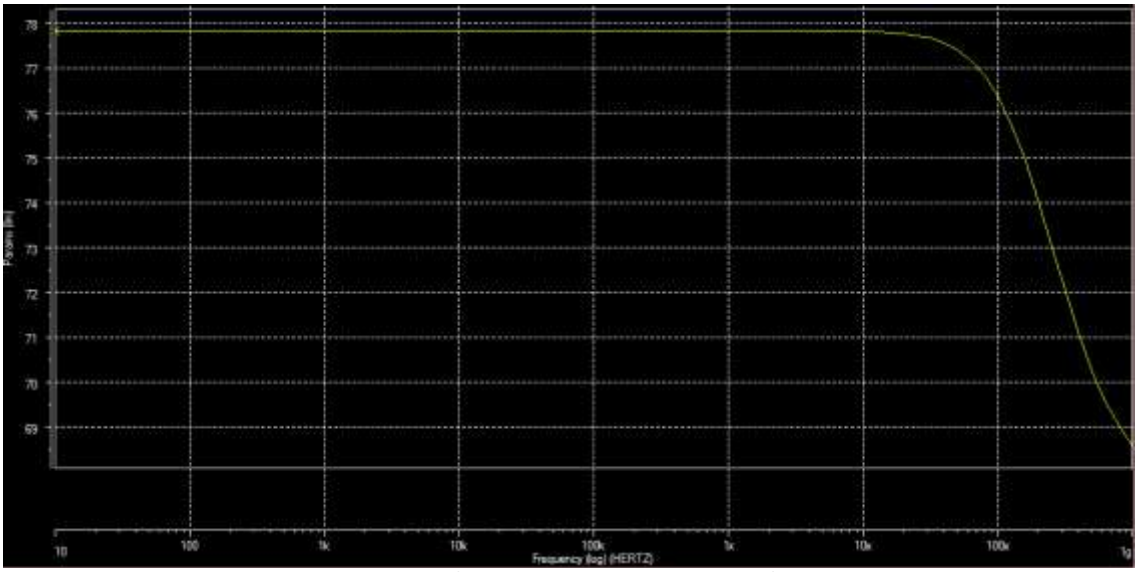

Figure 5-DC Gain of Proposed Instrumentation Amplifier at 1.5V

Simulated Data of Proposed Instrumentation Amplifier at 0.5V

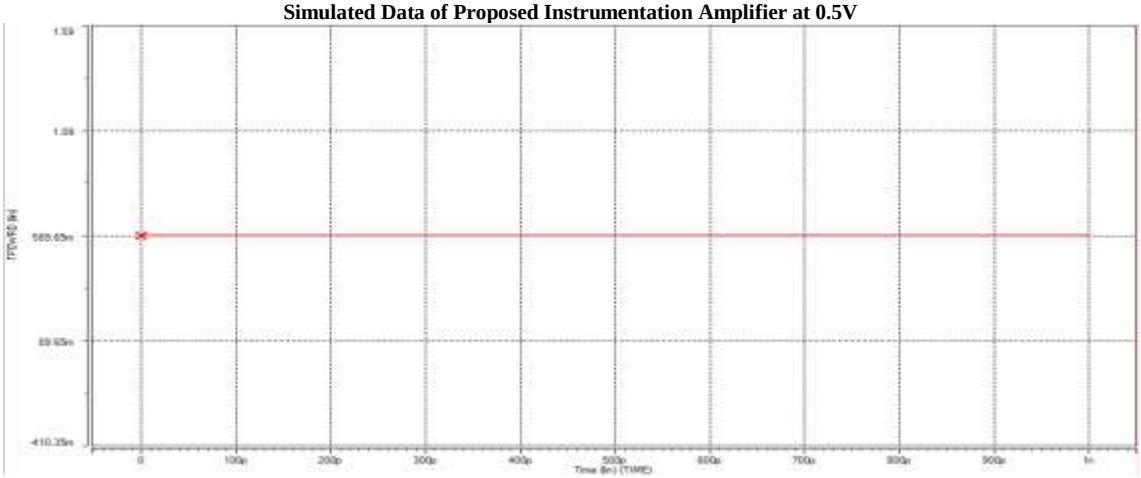

Figure 6-Average Power of Proposed Instrumentation Amplifier at 0.5V

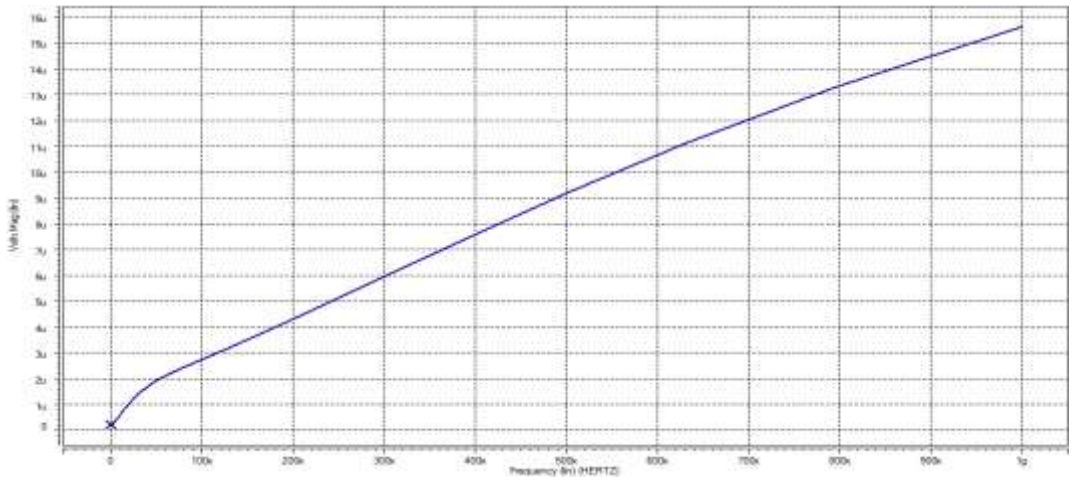

Figure 7-Output Signal of OP AMP1 of Proposed Instrumentation Amplifier at 0.5V

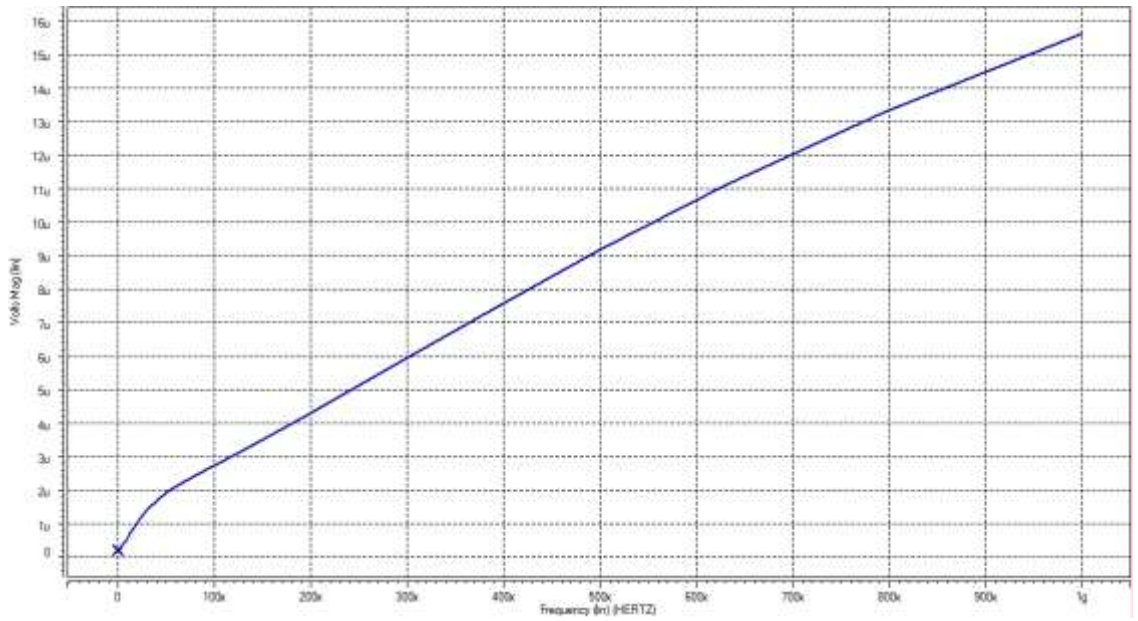

Figure 8-Output Signal of OP AMP2 of Proposed Instrumentation Amplifier at 0.5V

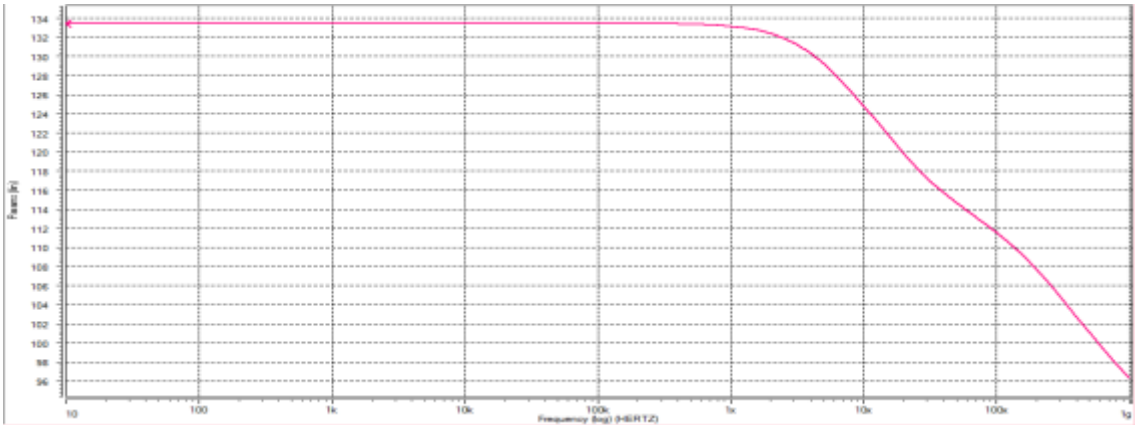

Figure 9-DC Gain of Proposed Instrumentation Amplifier at 0.5V

Table 1: Comparative analysis of Instrumentation Amplifier at different voltages using 32 nm tech. node.

S. No.	Parameters	Instrumentation Amplifier at 0.5V	Instrumentation Amplifier at 1.5V
1	DC GAIN	133.4 dB	77.84 dB
2	3- dB Bandwidth	3.87 MHz	164MHz
3	Average Power	589 mW	290mW

Table 2: Parameters used in the proposed Instrumentation Amplifier

S. No.	Parameters	Value
1	Channel Length	32nm
2	Channel Width	763nm
3	Supply Voltages	0.5V and 1.5V
4	NMOS TRANSISTORS	39
5	PMOS TRANSISTORS	27
6	Number of Operational Amplifiers	03
7	Technology File	PTM 32nm Metal Gate / High-K

CONCLUSION

In this research work, simulation and comparative analysis of Instrumentation Amplifier at different voltages. DC voltage gain, average power, bandwidth etc have been computed using HSPICE Software. The proposed Instrumentation is efficient in medical applications due to high gain and high bandwidth. Instrumentation Amplifier based on CMOS has been designed and simulated using 32nm CMOS technology.

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