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Simulation Study of Low Power Comparator for A-D Converter

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Abstract- Analog-to-Digital Converters (ADCs) translate the analog quantities into digital language, used in information processing, computing, data transmission and control systems. ADCs are key components for the design of power limited systems, in order to keep the power consumption as low as possible. Implantable Medical electronics, such as Pacemakers and cardiac defibrillators are typical examples of devices where ultra-low-power consumption is paramount. This paper presents design of CMOS comparator based on a preamplifier circuit. Design is intended to be implemented in for Analog-to-Digital Converter (ADC). The design is simulated in 1 µm CMOS Technology with HSPICE. Proposed design exhibits low power consumption. Simulation results are presented and the design has DC Gain of 68dB, power dissipation of 1.25 mW at 5 V.

Keywords-CMOS Comparator, Low Power, High Speed, ADC and HSPICE.

I. INTRODUCTION

This paper presents design of CMOS comparator based on a preamplifier circuit. Design is intended to be implemented in Analog-to-Digital Converter (ADC). In the A/D conversion process, it is necessary to first sample the input. This sampled signal is than applied to a combination of comparators to determine the digital equivalent of the analog signal [1] and it compare the analog signal with another reference signal and outputs are binary signal based on the comparison. Low power and high speed ADCs are the main building blocks in the front-end of a radio-frequency receiver in most of the modem telecommunication systems. As the comparator is one of the block which limits the speed of the converter, its optimization is of utmost importance. The preamplifier stage amplifies the input signal to improve the comparator sensitivity and isolate the input of the comparator from switching noise coming from positive feedback stage [2]. The latch stage is used to determine which of the input signals is larger and extremely amplifies their difference. The out-put buffer amplifies the information from latch and out-puts a digital signal [3]. One of the critical parts of an ADC greatly influenced by the process variation and mismatch is the comparator. In some ADCs, the offset voltage can be tolerated [4-5].

The comparator is an essential part in the SAR ADC to perform the binary search algorithm. Comparator in the SAR ADC takes more power consumption than the other blocks. A comparator generates a logic output high or low based on the comparison of the analog input with a reference voltage. In an ideal comparator, with infinite gain, for input voltages higher than the reference voltage, the comparator outputs logical one and for the input voltages lower than the reference voltage it produces zero at the output. [5-11].

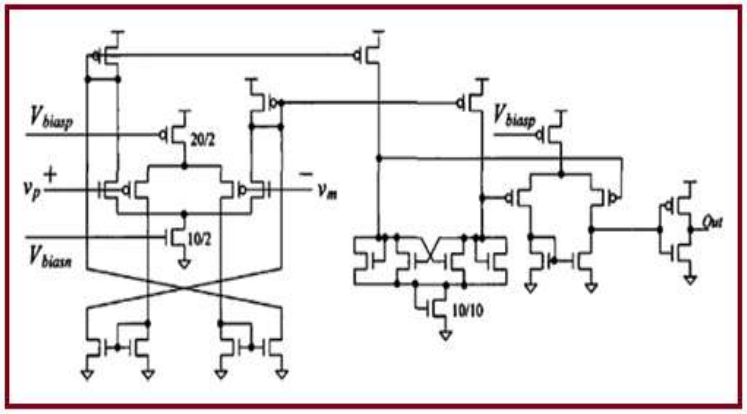
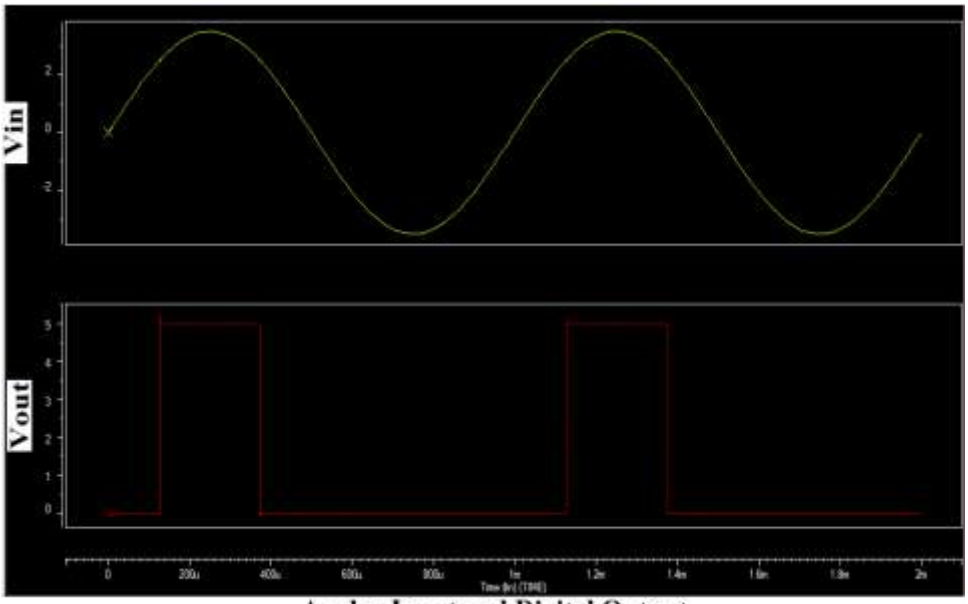


Figure1- Proposed Comparator

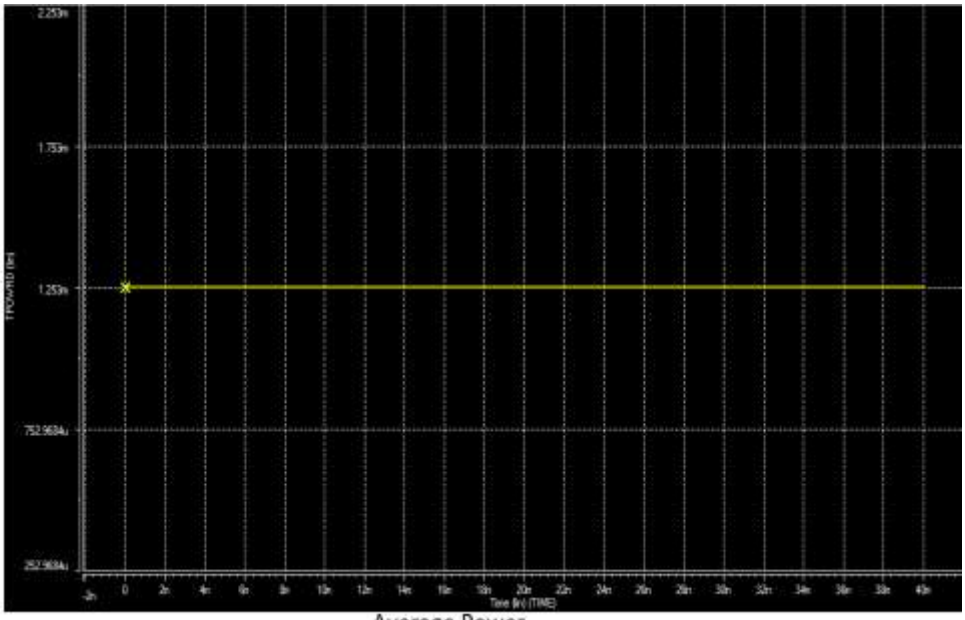
Analysis of the Proposed Comparator

Simulation results are presented and the design has DC Gain of 68dB, power dissipation of 1.25 mW at 5 V. In Transient Analysis input pulse is applied to obtain the desired output apart from AC Analysis to cheek the overall performance of the comparator. The performance limiting blocks in ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. To reduce the power consumption and the area of comparators, dynamic comparators are proposed.

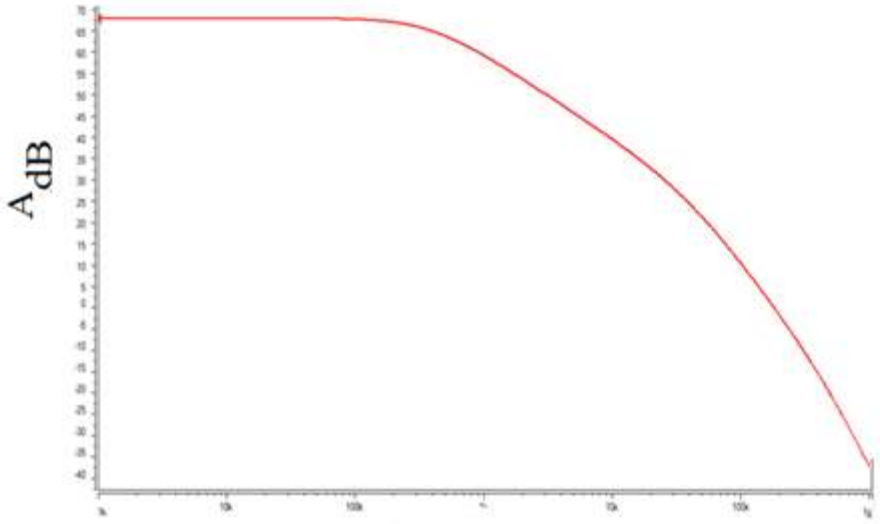
II. SIMULATION RESULTS



Analog Input and Digital Output



Average Power



DC Gain in dB

CONCLUSION

This paper presents a method for design of CMOS comparator based on a preamplifier. Design is intended to be implemented in Analog-to-Digital Converter (ADC). Simulation results are presented and the design has DC Gain of 68dB, power dissipation of 1.25 mW at 5 V using HSPICE software.

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