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## An Approach for Reduction in Power Consumption in Low Voltage Dropout Regulator

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**Abstract**— a low-dropout or LDO regulator is a DC linear voltage regulator which can control the output voltage even when the supply voltage is very close to the output voltage. The advantages of a low dropout voltage regulator include the absence of switching noise ( as no switching takes place), smaller device size ( as neither large inductors nor transformers are needed), and greater design simplicity (usually consists of a reference, an amplifier and a pass element). A significant adiabatic logic with 180 nm CMOS technology is proposed to reduce impact of power supply reductions well as a simple symmetric operational trans-conductance amplifier is used as the error amplifier (EA), with a current splitting method adopted to increase the gain and also improves the bandwidth of the LDO regulator.

**Keywords**— Error Amplifier, LDO, Gain, Regulator.

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### I. INTRODUCTION

A Power management system requires low drop-out in circuit. Therefore a battery operated device requires low dropout voltage regulators to increase the power efficiency. They are similar to linear voltage regulators but with constant voltage at the output and better power efficiency. A power management system constitutes of control logic, linear regulators and switching regulators. Linear regulators depending upon the type of orientation of pass device different types of LDO can be made. Different types of regulators are there: conventional by using BJT or PMOS type, linear regulator with source follower for improve version of source follower or Replica, with common source driver.

One of the most challenging problems in designing LDO is the power consumption problems due to the closed loop and the parasitic components associated with the pass transistor and the error amplifier. In fact to compensate the reduction in power consumption a large external capacitor is often connected at the output. Here for reduced power consumption the adiabatic logic is used.

The term “adiabatic” describe the thermodynamic processes in which no energy exchange with the environment, and therefore no dissipated energy loss. But in VLSI, the electric charge transfer between nodes of a circuit is considered as the process and various techniques can be applied to minimize the energy loss during charge transfer event. Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component.

In conventional CMOS logic circuits, from 0 to VDD transition of the output node, the total output energy drawn from power supply and stored in capacitive network. Adiabatic logic circuits reduce the energy dissipation during switching process, and utilize this energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source

power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage. The equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with

the constant current source to charge and discharge the output load capacitance. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source. Adiabatic Logic does not abruptly switch from 0 to VDD (and vice versa), but a voltage ramp is used to charge and recover the energy from the output.

Adiabatic circuits are low power circuits which use “reversible logic” to conserve energy. A 2.8-V LDO Voltage regulator with a 200mV dropout in 180 nm CMOS technology with a load current of 50mA is proposed to be simulated in the presence of 100 pF load on chip.

Hence, for getting the desired results we have to work on the following modules.

## II. Design of Error Amplifier

An **error amplifier** is most commonly encountered in feedback unidirectional voltage control circuits where the sampled output voltage of the circuit under control is fed back and compared to a stable reference voltage. Any difference between the two generates a compensating error voltage which tends to move the output voltage towards the design specification.

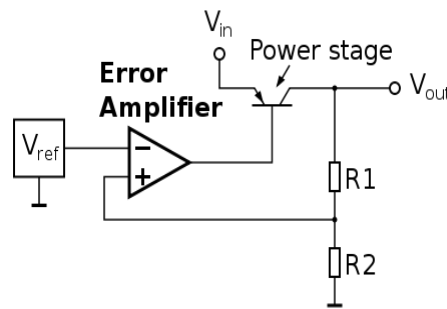


Fig.1 Error Amplifier

The gain of the EA (AEAO) is as follows:

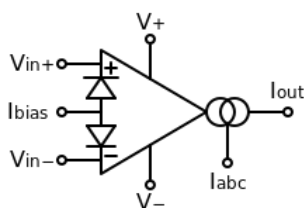
$$\begin{aligned} AEAO &= g_{m2} \times A \times (r_{O7} || r_{O9}) \\ &\approx g_{m2} \times A \times r_{O9} \\ &= (2I_{d2} / V_{ov2}) \times A \times (1/\lambda_9 \times A \times I_{d2}) \\ &= 2 / (V_{ov2} \times \lambda_9) \end{aligned}$$

The gain of the modified EA (AEAM) is boosted by a factor of 1/B as follows:

$$\begin{aligned} AEAM &\approx g_{m2} \times A \times r_{O9} \\ &= 2I_{d2} / V_{ov2} \times A \times (1/\lambda_9 \times A \times B \times I_{d2}) \\ &= AEAO / B. \end{aligned}$$

## III. Transconductance Amplifier

The transconductance amplifier or operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.



[https://en.wikipedia.org/wiki/Negative\\_feedback](https://en.wikipedia.org/wiki/Negative_feedback)

Fig.2 Schematic symbol for the OTA.

Like the standard operational amplifier, it has both inverting (-) and non-inverting (+) inputs; power supply lines ( $V+$  and  $V-$ ); and a single output. Unlike the traditional op-amp, it has two additional biasing inputs,  $I_{abc}$  and  $I_{bias}$ .

#### IV. Low Voltage Dropout Regulator

A **low-dropout** or **LDO** regulator is a DC linear voltage regulator which can regulate the output voltage even when the supply voltage is very close to the output voltage [1]. The advantages of a low dropout voltage regulator over other DC to DC regulators include the absence of switching noise (as no switching takes place), smaller device size (as neither large inductors nor transformers are needed), and greater design simplicity (usually consists of a reference, an amplifier, and a pass element). A significant disadvantage is that, unlike switching regulators, linear DC regulators must dissipate power across the regulation device in order to regulate the output voltage.

And this disadvantage we are going to overcome by using the adiabatic logic.

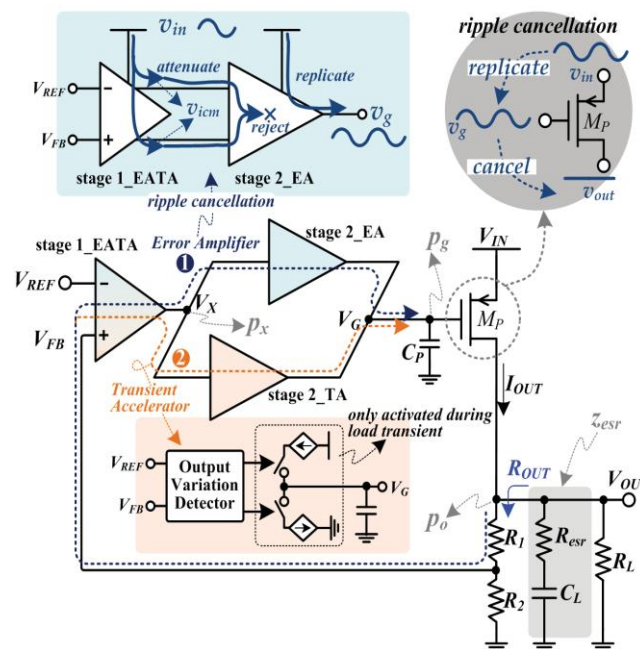


Fig.3 Block Diagram of conventional LDO regulator

#### V. The Proposed Work

In the current design the researchers has concentrated mainly on achieving high current efficiency, but did not focus on the power efficiency factor of the circuit. This will reduce the efficiency of the system by consuming more power. More power consumption will lead to reduced performance of the system which will reduce the current efficiency due to losses in the system under long running conditions.

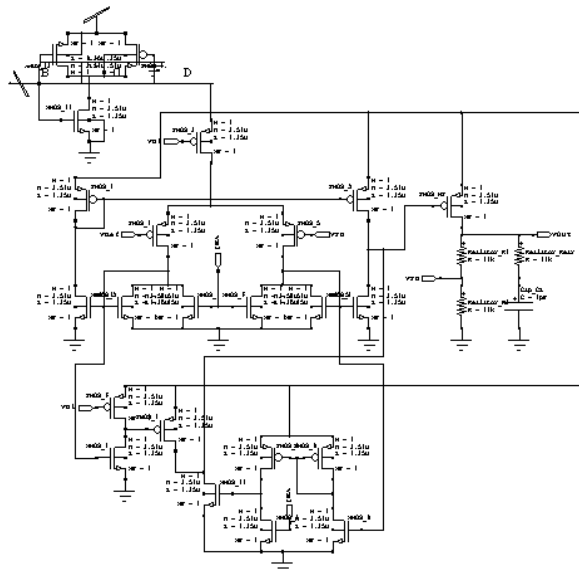


Fig.4 Schematic of proposed LDO regulator with adiabatic logic

To reduce the impact of power consumption on the system we introduce an adiabatic logic design for the system which will reduce the power consumption by half and thereby allowing the circuit to run for a higher duration and improve the overall efficiency of the system. The adiabatic circuit is built on a very specific power supply connected hardware which runs during the positive clock cycle and charges the circuit, while during negative clock cycle the power supply is cut-off and the stored charge is used for running or performing operation of the circuit thereby, reducing the power consumption.

### VI. Experimental Results and The Performance Evaluations

The proposed LDO regulator is fabricated using a 180-nm CMOS process. The core area is near about 0.001296 nm<sup>2</sup> and the maximum load current is approximately 2.21 mA.

Sr. no	Design	2008	2009	2010	2012	2013	2014	Proposed work	
1	Para met- Technology(CMOS)	SMIC 0.18- $\mu$ m	TSMC 0.35 $\mu$ m	-	90nm	TSMC 0.35 $\mu$ m	90nm	180nm	
2	ers	Vdd/Vout (V)	1.2	1.5	2.7	-	1.2	1/0.85   1/0.5	1.8/1.1
3		Load cap.C <sub>L</sub> ( $\mu$ f)	1		-	-	100nF	1	1nf
4		Resistor ( $\Omega$ )	No	No	-	-	-	1	No
5		Max I <sub>out</sub> (mA)	200	100	2.5	-	50	100	2.218
6		Area( mm <sup>2</sup> )	-	0.14	0.038	-	-	0.0041	0.001296 $\mu$ m <sup>2</sup>
7		Power Dissipation(mw)	-	-	0.154	-	-	-	2.4448

### Conclusion

This paper presented an LDO regulator with 180nm CMOS technology using a simple logic of the gate which can work energetically reversible without the need to be logically reversible i.e. the Adiabatic logic with load capacitance of 1pF ,VDD of 1.8V and power dissipation near about of 2.4448mW which may achieve an efficient operation with very less average power approximately around 2.4837mW, and the area also reduces accordingly upto 0.001296nm<sup>2</sup> under a wide range of operating conditions. The experimental results verified the feasibility of the proposed LDO regulator.

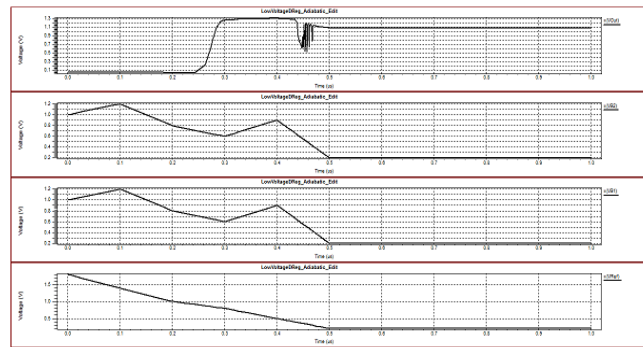


Fig.5 Simulation result of LDO regulator with adiabatic logic

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