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Optimization, Analysis and Comparison of 4 and 16 bit Carry look Ahead Adders using 0.3µm Process Technology for SCMOS

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Abstract - A method illustrated in this is to design carry look ahead adders using SCMOS technology, also analyzed the effect of various parameters on the characteristics of adders, using 50 nm, spice model for CMOS technology. The design was implemented for 16 bit and then extended for 32 bit also. Here parameters are computed and response curves are computed between all characteristics, DC and transient characteristics. The design and simulations are carried out to achieve these values approximately. Design will be carried out in Electric CAD and Xilinx. Simulation results are verified using Model sim and LTSpice. The DRC, LVS/NCC, transient checks are performed in the proposed design. Noise analysis is also done. In comparison with the existing full adder designs, the present implementation will offer significant improvement in terms of frequency.

Key Words: Full adder, CMOS Circuit, C5 Process, Carry looks ahead adder, Transient analysis.

I. INTRODUCTION

An adder is a combinational digital circuit which performs addition of number. In many computers and other processors adders are used in arithmetic logic units and other parts of processors where they are used to calculate addresses, increment and decrement operators, and table indices. They can also be constructed for many numerical representations such as binary coded decimal or excess-3, the most common adders operate on binary numbers. In case where two's complement or one's complement is being used to represent negative number. Adders are the elemental units in various electronic circuits especially in circuits used for performing arithmetic operations. An optimized is needed to avoid any degradation at the circuit level in the output voltage, less delay in critical path, and consume less power.

II. FULL ADDER

A Full adder is a logical circuit that performs an addition operation on three one bit binary numbers. The Full Adder produces a sum of the two inputs and carries value. It can be combined with other full adders or work on its own. Full adders are one of the most fundamental building block for circuit applications, remain a key focus domain of the researchers over the years. Different logic styles, each having its own merits and bottlenecks, was investigated to implement reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart. These designs exploit the features of different logic styles to improve the overall performance of the full adder**.** There are two types of full adders in case of logic structure. One is static and the other is dynamic style. Static full adders are commonly more reliable, simpler and are lower power consuming than dynamic ones. Dynamic is an alternative logic style to design a logic function. It has some advantages over the static mode such as faster switching speeds, no static power consumption, nonrated logic, full swing voltage levels, and lesser number of transistors. An N input logic function requires N+2 transistors versus 2N transistors in the standard CMOS logic.

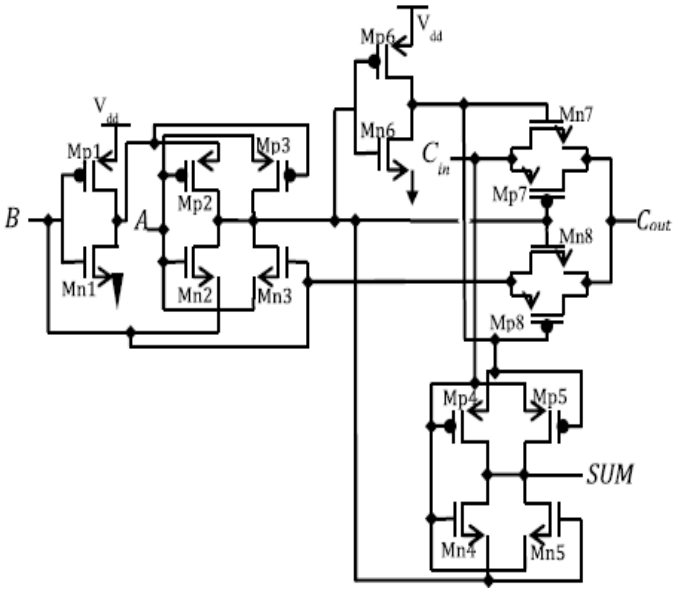

Figure.1 – Full Adder Cell

Many full adder cells designed with the help of static logic style in 180 nm CMOS technology. One is the Pseudo-nMOS Full Adder and other is the Conventional CMOS Full Adder. The Pseudo-nMOS Full Adder cell is worked by Pseudo-nMOS logic or rationed logic. The CMOS pull up network is substituted by a single pMOS transistor with its gate grounded. The pMOS is always 'on' because it is not driven by signals. Vdd is the effective gate voltage seen by the pMOS transistor. When the nMOS is turned 'on', static power will be drawn in the transistor because direct path between supply and ground exists. It uses 18 transistors to make a single full adder circuit. The operation is executed by negative addition. The advantages of using Pseudo-nMOS logic is that it gives less number of transistors than CCMOS with high speed performance and disadvantage is that it is more susceptible to noise, has increased power consumption of pull up transistor and reduced output swing. The Conventional CMOS Full Adder is based on regular CMOS structures known as pull-up and pull-down networks but it uses 28 transistor. Complementary transistor pairs construct the circuit layout to be very straight forward. It generates carry through a static gate. The advantage of using CCMOS is that it has stability at low voltage due to complementary transistor pair, layout regularity, high noise margins and smaller number of interconnecting wires. The disadvantage is that it produces an unwanted additional delay, has weak output driving capability due to series transistors in output stage, requires large silicon area and consumes more power.

2.1 Others Complex Adders using full adder

Full adder circuits can be divided into two groups on the basis of output. The first group of full adders has full swing output. C^2CMOS, CPL, TGA, TFA, Hybrid, 14T, and 16T etc. belong to the first group. The second group comprises of full adders 10T, 9T and 8T without full swing outputs. These full adders usually have low number of transistors usually3 based XOR-XNOR circuit, decreased power consumption as well as dissipation, and less chip area occupation. The non full swings full adder circuits are pretty handful in designing larger arithmetic mixed signal circuits as multi bit input adder and multipliers mainly. There are standard styles of arithmetic circuit implementations for the full adder cells which are used as the basis of comparison previous adder's single bits in this dissertation. Some of the standard implementations are as follows.

CMOS logic styles have been mainly considered or used to design and implement the low power single bit adder cells. Generally, they can be broadly seen into two major groups: Complementary CMOS logic and the Pass-Transistor or transmission logic circuits. The complementary CMOS full adder shown in below Figure 1 is based on the regular CMOS structure. The benefit of complementary CMOS style is its heftiness against voltage scaling and transistor sizing mainly for submicron or deep submicron technologies like the one mentioned in this thesis, which are necessary to provide reliable operation at low voltage or power with suitable small transistor sizes.

In many computers and other kinds of processors, Carry-look ahead adder (CLA) or fast adder is a type of adder used in digital logic. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits [1]. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The Kogge-Stone adder and Brent-Kung adder are examples of this type of adder.

A ripple-carry adder works in the same way as pencil-and-paper methods of addition. Starting at the rightmost (least significant) digit position, the two corresponding digits are added and a result obtained. It is also possible that there may be a carry out of this digit position (for example, in pencil-and-paper methods, "9+5=4, carry 1"). Accordingly all digit positions other than the rightmost need to take into account the possibility of having to add an extra 1, from a carry that has come in from the next position to the right. The

advantages of standard complementary (CMOS) style-based adders with twenty eight transistors are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers. Full adders are one of the most fundamental building block for circuit applications, remain a key focus domain of the researchers over the years. Different logic styles, each having its own merits and bottlenecks, was investigated to implement reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart.

The advantages of standard complementary (CMOS) style-based adders with twenty eight transistors are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers. Another complementary type smart design is the mirror adder with almost same power consumption and transistor count but the maximum carry Propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder. On the other hand, CPL shows good voltage swing restoration employing thirty two transistors.

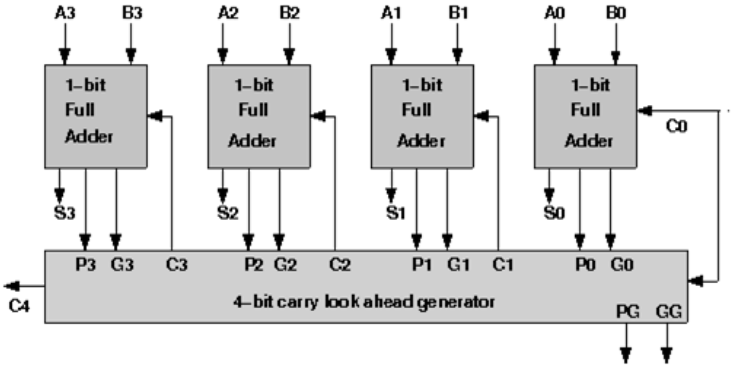

Figure 2 -Block diagram of Carry Look ahead adder

III. DESIGN RESULTS

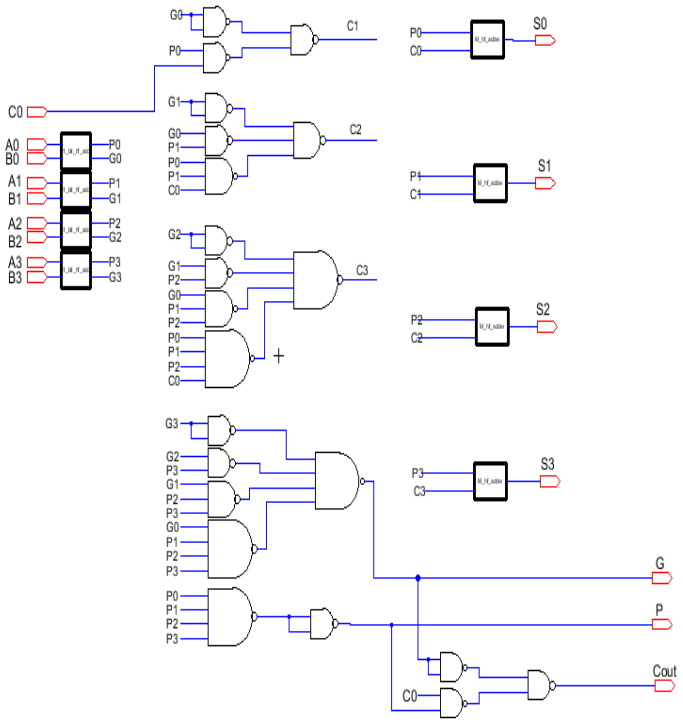

Figure 3 -Schematic design for 4 bit Carry look ahead adder

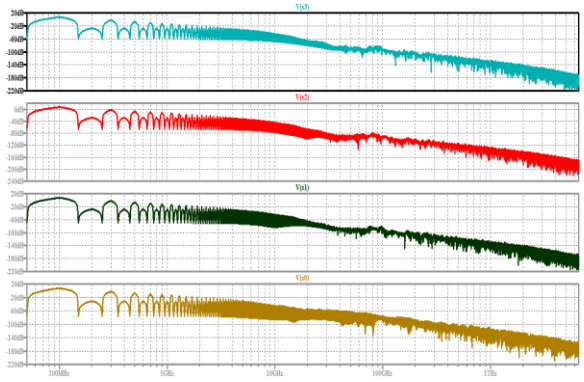

Figure 4.10 FFT plots for sum signals in 4 bit CLA

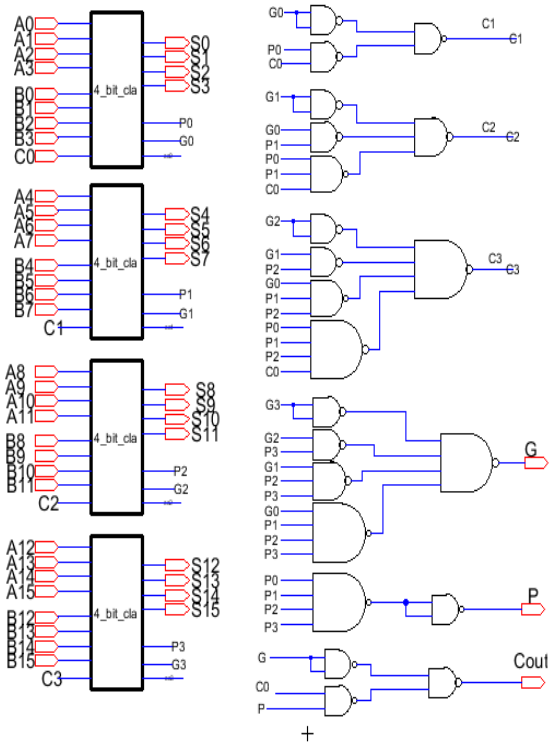

Figure 5 Schematic designs for 16 bit Carry look ahead adder

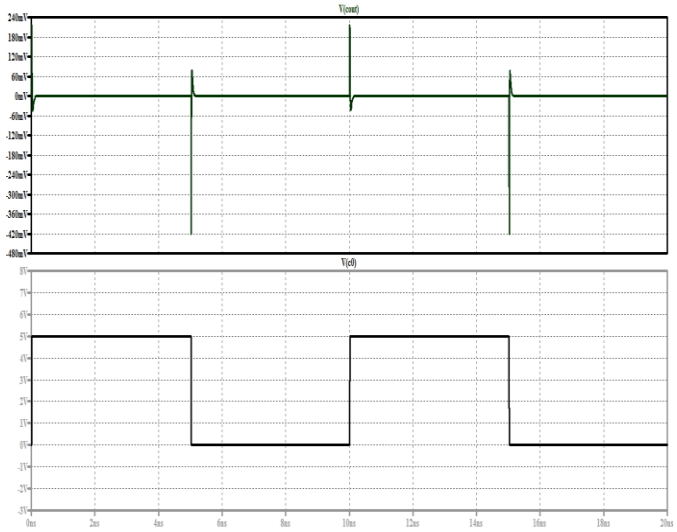

Figure 6 Transient analysis plots for Carryout

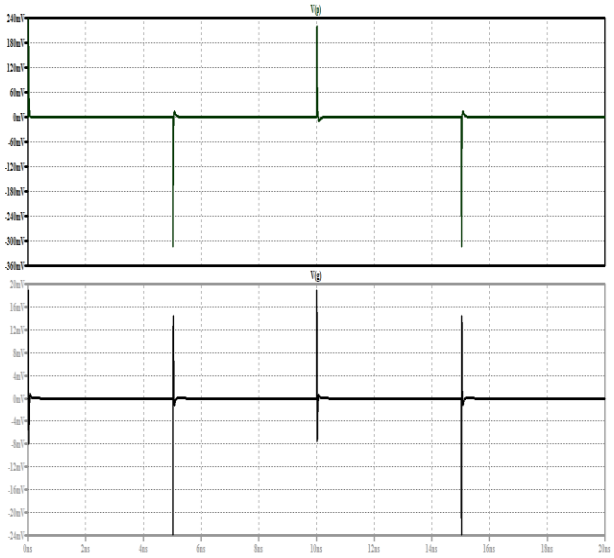

Figure 7 Transient analysis plots for propagate and generate signals in 16 bit CLA

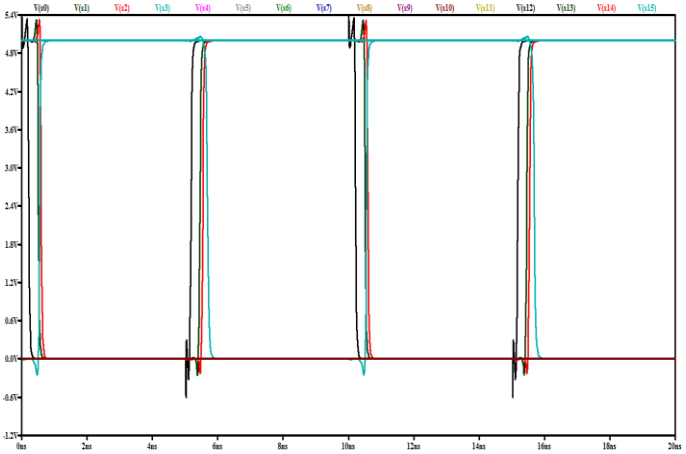

Figure 8 Transient plot for Sum signals in 4 bit CLA

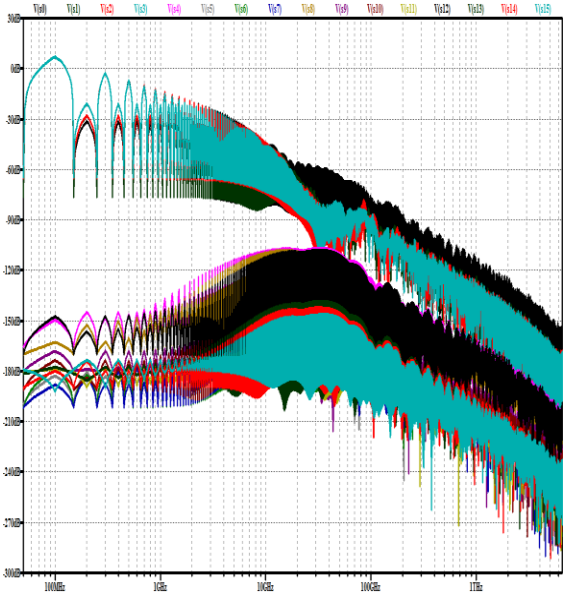

Figure 9 FFT plots or Noise Index plot for Sum Signals in 16 bit CLA design

IV. FFT PLOTS COMPARISON BETWEEN 4 BIT CLA AND 16 BIT CLA

The performance analysis of adders 4 bits and 16 bits in erms of their FFT profile is shown in above section and tabulation and comparison of FFT and transient parameters is illustrated here and drawn in table- 1, shows different,. Thus, there exists tradeoff between these parameters. The results are helpful in selection of an adder according to desired result and application.

Table 1

FFT Index Results for 4 bit CLA (Sum Signals)

FFT plot parameters for signal S_0			
S.No.	**Frequency**	**Magnitude**	**Delay**
1.	10MHz	94.59 dB	213.17 ps
	100 MHz	6.27 dB	49.76 ns
	100 GHz	111.9 dB	179.90 ps
FFT plot parameters for signal S_1			
2.	**Frequency**	**Magnitude**	**Delay**
	10MHz	91.13 dB	522.8 ps
	100 MHz	6.27 dB	7.82 ns
	100 GHz	115.57 dB	567.45 ps
FFT plot parameters for signal S_2			
3.	**Frequency**	**Magnitude**	**Delay**
	10MHz	86.51 dB	603.75 ps
	100 MHz	6.277 dB	49.30 ns
	100 GHz	12.43 dB	116.10 ps
FFT plot parameters for signal S_3			
4.	**Frequency**	**Magnitude**	**Delay**
	10MHz	81.8 dB	698.35 ps
	100 MHz	6.277 dB	49.20 ns
	100 GHz	109.98 dB	808.22 s

Table 2

FFT Index Results for 16 bit CLA (Sum Signals)

FFT plot parameters for signal S_0			
S.No.	**Frequency**	**Magnitude**	**Delay**
1.	100MHz	6.99 dB	4.78 ns
	1THz	127.32 dB	2.5 ns
FFT plot parameters for signal S_1			
2.	**Frequency**	**Magnitude**	**Delay**
	100MHz	6.96 dB	4.46 ns
	1THz	131.55dB	457.57 ps
FFT plot parameters for signal S_2			
3.	**Frequency**	**Magnitude**	**Delay**
	100MHz	6.99 dB	4.39 ns
	1THz	131.36 dB	2.7 ns
FFT plot parameters for signal S_3			
4.	**Frequency**	**Magnitude**	**Delay**
	100MHz	7.02 dB	575.40ps
	1THz	138.157 dB	1.05 ns
FFT plot parameters for signal S_4			
	Frequency	**Magnitude**	**Delay**
5.	100MHz	149.10	149.89 ps
	1THz	166.049 dB	1.89 ns
FFT plot parameters for signal S_5			
6.	**Frequency**	**Magnitude**	**Delay**
	100MHz	186.98 dB	101.89 ps
	1THz	199.19 dB	386.01 ps
FFT plot parameters for signal S_6			
7.	**Frequency**	**Magnitude**	**Delay**
	100MHz	179.27 dB	5.05 ns

	1THz	202.24 dB	3.26 ns
FFT plot parameters for signal S_7			
8.	**Frequency**	**Magnitude**	**Delay**
	100MHz	188.17 dB	5.04 ns
	1THz	208.60 dB	153.78 ps
FFT plot parameters for signal S_8			
	Frequency	**Magnitude**	**Delay**
9.	100MHz	162.83 dB	66.49 ps
	1THz	175.61 dB	3.88 ns
FFT plot parameters for signal S_9			
10.	**Frequency**	**Magnitude**	**Delay**
	100MHz	168.09 dB	5.09 ns
	1THz	196.16 dB	2.77 ns
FFT plot parameters for signal S_{10}			
11.	**Frequency**	**Magnitude**	**Delay**
	100MHz	174.05 dB	4.53 ns
	1THz	199.97 dB	3.99 ns
FFT plot parameters for signal S_{11}			
12.	**Frequency**	**Magnitude**	**Delay**
	100MHz	100.07 dB	58.34 ps
	1THz	204.57 dB	186.18 ps
FFT plot parameters for signal S_{12}			
	Frequency	**Magnitude**	**Delay**
13.	100MHz	147.51 dB	5.081 ns
	1THz	176.16 dB	3.17 ns
FFT plot parameters for signal S_{13}			
14.	**Frequency**	**Magnitude**	**Delay**
	100MHz	177.68 dB	56.266 ps
	1THz	206.44 dB	3.08 ns
FFT plot parameters for signal S_{14}			

15.	**Frequency**	**Magnitude**	**Delay**
	100MHz	179.96 dB	5.09 ns
	1THz	211.35 dB	2.73 ns
FFT plot parameters for signal S_{15}			
16.	**Frequency**	**Magnitude**	**Delay**
	100MHz	192.05 dB	75.21 ps
	1THz	217.46 dB	1.01 ns

CONCLUSION

Keeping in view different applications the carry look ahead adder design has been designed. For this first a selection is made for the active device used. The development of a design procedure provides a quick, well integrated and effective mechanism for estimation and calculation of various parameters. The steps highlighted make it easy to redesign the circuit for various set of specifications. The responses are simulated using LTSpice and Electric VLSI CAD design tool. The simulated results of the carry look ahead adder will be in compliance with the theoretical values. The responses are simulated using LTSpice and Electric VLSI CAD design tool.

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REFERENCES

1. Bhattacharyya, Partha, Bijoy Kundu, Sovan Ghosh, Vinay Kumar, and Anup Dandapat. "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit." IEEE Transactions on very large scale integration (VLSI) systems 23, no. 10 (2015): 2001-2008.

2. Han, Liu, Hao Zhang, and Seok-Bum Ko. "Area and power efficient decimal carry-free adder." Electronics Letters 51.23 (2015): 1852-1854.

3. Mohanty, Basant Kumar, and Sujit Kumar Patel. "Area–Delay–Power efficient carry-select adder." IEEE Transactions on Circuits and Systems II: Express Briefs 61.6 (2014): 418-422.

4. Pan, Yu, and Pramod Kumar Meher. "Bit-level optimization of adder-trees for multiple constant multiplications for efficient FIR filter implementation." IEEE Transactions on Circuits and Systems I: Regular Papers 61.2 (2014): 455-462.

5. Manju, S., and V. Sornagopal. "An efficient SQRT architecture of carry select adder design by common Boolean logic." Emerging Trends in VLSI Embedded System, Nano Electronics and Telecommunication System (ICEVENT), 2013 International Conference on. IEEE, 2013.

6. Ramkumar, B., and Harish M. Kittur. "Low-power and area-efficient carry select adder." IEEE transactions on very large scale integration (VLSI) systems 20.2 (2012): 371-375.

7. Wey, I-Chyn, et al. "An area-efficient carry select adder design by sharing the common Boolean logic term." Proceedings on the International Multiconference of Engineering and computer scientist, IMECS. 2012.

8. Prashanth, P., and Prabhu Swamy. "Architecture of adders based on speed, area and power dissipation." Information and Communication Technologies (WICT), 2011 World Congress on. IEEE, 2011.

9. Zavarei, Mohammad Javad, et al. "Design of new full adder cell using hybrid-CMOS logic style." Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on. IEEE, 2011.

10. Aguirre-Hernandez, Mariano, and Monico Linares-Aranda. "CMOS full-adders for energy-efficient arithmetic applications." IEEE transactions on very large scale integration (VLSI) systems 19.4 (2011): 718-721.

11. Han, Liu, et al. "Nonspeculative decimal signed digit adder." 2011 IEEE International Symposium of Circuits and Systems (ISCAS). IEEE, 2011.

12. Wairya, Subodh, et al. "Design analysis of XOR (4T) based low voltage CMOS full adder circuit." 2011 Nirma University International Conference on Engineering. IEEE, 2011.

13. Aranda, Monico Linares, Ramon Báez, and Oscar Gonzalez Diaz. "Hybrid adders for high-speed arithmetic circuits: A comparison." Electrical Engineering Computing Science and Automatic Control (CCE), 2010 7th International Conference on. IEEE, 2010.

14. Hassoune, Ilham, et al. "ULPFA: a new efficient design of a power-aware full adder." IEEE Transactions on Circuits and Systems I: Regular Papers 57.8 (2010): 2066-2074.

15. Navi, Keivan, et al. "A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter." Microelectronics Journal 40.10 (2009): 1441-1448.

16. Jaberipur, Ghassem, and Saeid Gorgin. "A nonspeculative maximally redundant signed digit adder." Advances in Computer Science and Engineering. Springer Berlin Heidelberg, 2008. 235-242.

17. Chandrakasan, Anantha P., Naveen Verma, and Denis C. Daly. "Ultralow-power electronics for biomedical applications." Biomedical Engineering 10 (2008).

18. Tung, Chiou-Kou, et al. "A low-power high-speed hybrid CMOS full adder for embedded system." 2007 IEEE Design and Diagnostics of Electronic Circuits and Systems. IEEE, 2007.

19. Moskal, John, Erdal Oruklu, and Jafar Saniie. "Design and synthesis of a carry-free signed-digit decimal adder." 2007 IEEE International Symposium on Circuits and Systems. IEEE, 2007.

20. Alioto, Massimo, Giuseppe Di Cataldo, and Gaetano Palumbo. "Mixed Full Adder topologies for high-performance low-power arithmetic circuits." Microelectronics Journal 38.1 (2007): 130-139.

21. Goel, Sumeer, Ashok Kumar, and Magdy A. Bayoumi. "Design of robust, energy-efficient full adders for deep-sub micrometer design using hybrid-CMOS logic style." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 14.12 (2006): 1309-1321.

22. HE, Weste Neil. Cmos Vlsi Design: A Circuits And Systems Perspective, 3/E. Pearson Education India, 2006.

23. Chang, Chip-Hong, Jiangmin Gu, and Mingyan Zhang. "A review of 0.18-/spl mu/m full adder performances for tree structured arithmetic circuits." IEEE Transactions on very large scale integration (VLSI) systems 13.6 (2005): 686-695.

24. Nikmehr, Hooman, Braden Phillips, and Cheng-Chew Lim. "A decimal carry-free adder." Smart Materials, Nano-, and Micro-Smart Systems. International Society for Optics and Photonics, 2005.

25. Zhang, Mingyan, Jiangmin Gu, and Chip-Hong Chang. "A novel hybrid pass logic with static CMOS output drive full-adder cell." Circuits and Systems, 2003. ISCAS'03. Proceedings of the 2003 International Symposium on. Vol. 5. IEEE, 2003.

26. Goel, Sumeer, Mohamed A. Elgamel, and Magdy A. Bayoumi. "Novel design methodology for high-performance XOR-XNOR circuit design." Integrated Circuits and Systems Design, 2003. SBCCI 2003. Proceedings. 16th Symposium on. IEEE, 2003.

27. Rabaey, J. M., A. Chandrakasan, and B. Nikolic. "Digital Integrated Circuits, A Design Perspective, 2nd Prentice Hall." Englewood Cliffs, NJ (2002).

28. Shams, Ahmed M., Tarek K. Darwish, and Magdy A. Bayoumi. "Performance analysis of low-power 1-bit CMOS full adder cells." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 10.1 (2002): 20-29.

29. Bui, Hung Tien, Yuke Wang, and Yingtao Jiang. "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates." IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing 49.1 (2002): 25-30.

30. Kim, Youngjoon, and Lee-Sup Kim. "64-bit carry-select adder with reduced area." Electronics Letters 37.10 (2001): 1.+ Radhakrishnan, D. "Low-voltage low-power CMOS full adder." IEE Proceedings-Circuits, Devices and Systems 148.1 (2001): 19-24.

31. Vesterbacka, Mark. "A 14-transistor CMOS full adder with full voltage-swing nodes." Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop on. IEEE, 1999.

32. Wang, Jyh-Ming, Sung-Chuan Fang, and Wu-Shiung Feng. "New efficient designs for XOR and XNOR functions on the transistor level." IEEE Journal of solid-state Circuits 29.7 (1994): 780-786.

