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Intelligent Real Time Data Scan Module for Improved System Performance of Distributed Flight Test Instrumentation System Architecture

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ABSTRACT—Configuring and designing on-board flight test instrumentation for a modern fighter aircraft is a real challenge. Flight Test Instrumentation (FTI) System has to acquire data from large number of sensors on aircraft. It demands distributed acquisition and centralized processing based flight test instrumentation as the sensors and data acquisition units are spread across large area of the aircraft. Acquisition of data in real time from large numbers of sensors, formatting minor frames as per telemetry standards, and real time data telemetry is a critical task as load on process is very high.

This paper brings out a technique for relieving great extent processor load from processor participating to exchange the minor frame data and on-board storage data between remote acquisition unit (RAU) and data center (DACENT) with the help of Intelligent Real Time Data Scan Module(IRDSM). This paper also brings out the detail design approach adopted for IRDSM and significant performance improvement gained.

Common design methodology adopted for DACENT and RAU are also brought out here. Self test capabilities of the module, component count reduction for better reliability, design of registry structure, process of screening at the module level for better reliability, extensive testing of modules with different configurations, etc, are also discussed. Issues encountered during the development phase are brought in this paper.

Keywords— Flight Test Instrumentation (FTI), Intelligent Real Time Data Scan Module(IRDSM), Fighter Aircraft, Open System Architecture (OSA), remote acquisition unit (RAU), data center(DACENT), VME and cPCI, Signal Conditioning and Data Acquisition (SCADA), High data integrity, Ground Support Equipments (GSE), Telemetry, minor frame and major frame.

I. INTRODUCTION

Arriving at an optimum architecture is an important part of the on-board system design. System architecture decides the overall reliability and performance. It is essential for the system designer to pay extra attention during system architecture finalization to reap the additional benefits of good system architecture.

Fighter aircrafts are in general complex platforms hosting large number of state of art subsystems/systems. Flight testing is an important stage of certification process of a development aircraft. To assess functionality of all subsystems, health of the aircraft and also to carryout test points during the flight testing of development aircraft, it is required to

instrument the aircraft with suitable on-board flight test instrumentation. Flight test instrumentation system (FTI) is one of the complex systems on-board the aircraft catering to acquire large number of sensors data, aircraft subsystems sensors tapped data and digital bus data. Number of parameters varies from 15000 to about 30000. The sensors are spread across large area on the aircraft. These factors drive the flight test instrumentation system to a distributed configuration with centralized processing for real time telemetry transmission and on-board storage.

There are more off the shelf proprietary architecture based flight test instrumentation systems available in the market. These are high cost systems and maintenance or system up gradation or modifications during the flight test phase is tied to vendor support. Flight testing phase is significantly increasing as fighter aircraft complexity and weapon configurations are growing. Therefore Open System Architecture(OSA) based Flight test instrumentation gives significant advantages due to multivendor support for technology insertion, maintenance, up gradation, modifications, lower cost of ownership, etc,. Open System Architecture based Flight Test Instrumentation system configured for Modern fighter Aircraft is shown in fig 1. This system uses RS485 and RS422 buses for data exchange between DACENT and RAUs.

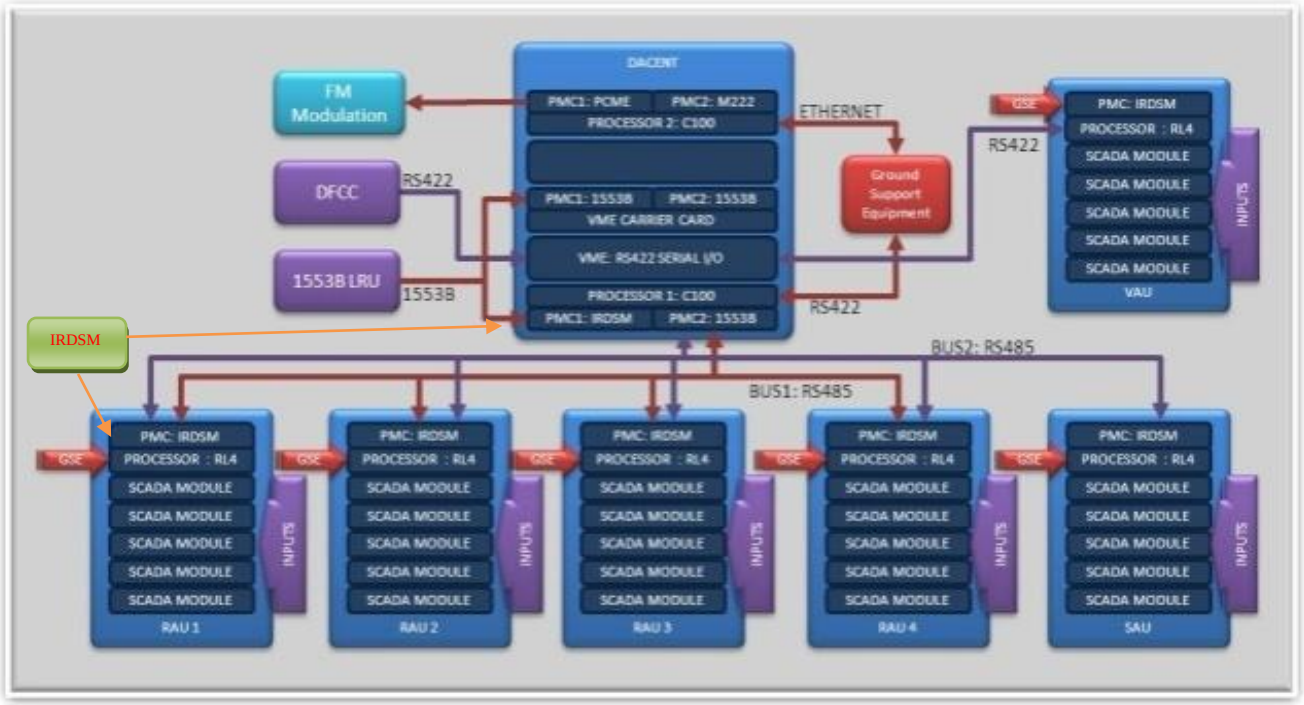

Fig. 1 Open system architecture based flight test instrumentation

II. PERFORMANCE IMPROVEMENT THROUGH SYSTEM ARCHITECTURE OPTIMIZATION

Large number of IOs connected to RAU results in huge data acquisition and transfer to DACENT. Data integrity is an essential part of flight test instrumentation system. To enable real time telemetry of selected parameters from large data acquired and storage of complete data onboard needs efficient way of data exchange between RAUs and DACENT. Real time telemetry data is as per IRIG-106 frame format, in which data is transferred in terms of minor frames in a major frame. The minor frames are constructed with the data coming from various RAUs. Real time formatting of this data is a great challenge, while system is handling various other critical functions. Data from RAUs need to be sent in a predefined format periodically. This is a computational intensive activity and over head on RAUs computation is significantly high.

To off load RAUs from this activity to the great extent and concentrate on prime responsibility of acquiring data from various sensors with high degree of data integrity/without data loss, Intelligent Real time Data Scan Module (IRDSM) is introduced into System Architecture. System is configured such way that it is used in DACENT and in RAU for scanning

and collecting data from different RAUs. At RAU end, IRDSM relieves RAU. participating from bus management activities, formatting of data as required, packetizing, transferring, etc,. In DACENT, it manages system level initialization of various RAUs, scheduling of commands for minor frame data collection from various RAUs and also scheduling commands for on-board storage, verification of data received with data integrity checks, performing bus management functions, etc,. IRDSM on DACENT has reduced the processor over head and improved significantly overall system performance.

III. INTELLIGENT REAL TIME DATA SCAN MODULE (IRDSM)

Intelligent Real Time Scan Module (IRDSM) with RS485 bus interface is based on PMC (PCI mezzanine Connector) bus. IRDSM resides on PowerPC controller module of DACENT and RAUs. To support the scanning of the data from RAUs by DACENT, IRDSM is configured for DACENT, i.e. IRDSM-D and for RAU, IRDSM-R. Hardware is common and firmware is specific for each of this functionality. Each IRDSM has two RS485 buses (Ref Fig1) one for scanning data for online telemetry and another for scanning data for onboard storage. Through IRDSM is programmable for scan interval, it is being used 80 micro seconds with word interrupt and 12,5 mSec with frame interrupt for the current application. This can be programmable for specific application requirement. On board storage, scan interval is 1 sec

A. IRDSM in DACENT Mode

The functionality of the IRDSM in DACENT Mode (IRDSM-D) is to scan data from RAUs connected on RS485 bus. The IRDSM is provided with on board dual port memories to maintain transmit/receive buffers. IRDSM-D acquires parameters from RAUs in the form of packets. The PowerPC controller module loads the scan information data for the complete major frame. On initiation from the DACENT controller, IRDSM scans the RAUs and collects the parameter data from RAUs and stores in the on board dual port memory. Transmit/receive buffers are maintained in IRDSM-D dual port buffers and at the end of each sequence the buffer is handed over to the PowerPC by interrupt mechanism. Multiple buffering is used to enable scanning for RAUs for next cycle (minor frame), while previous buffers are being processed for transmission. Similarly, scan sequence for on-board storage is loaded accordingly for collecting RAU data periodically (one second interval, large data) on 2nd RS485 bus.

B. IRDSM in RAU Mode

The functionality of IRDSM-R is to read RAU acquired data from appropriate memory locations and transmit the data in the form of packets on RS485 bus, on request from DACENT. The hardware sequencer provided on the IRDSM-R automatically identifies the request from DACENT to transmit data or status. The IRDSM-R relieves the PowerPC in RAU from decoding the command packet, forming the data packet and transmitting data packet on RS485 for both real time and onboard storage.

C. IRDSM Specifications

The detailed specifications for IRDSM are given TABLE I.

TABLE I. IRDSM SPECIFICATIONS

Sl No	Specifications	Sl No	Specifications
Hardware Specifications		**Functional Requirements-IRDSM-D**	
1	PCI Mezzanine Card (PMC) compatible with IEEE 1386.1 Specifications	1	Test/Maintenance Mode
2	Burst Transfer Mode.	2	Configuration Mode
3	512KB DPRAM	3	Online Mode a. OLT(On line Telemetry) and b. On-Board Storage (OBS)
4	Configurable buffer Size	**Test/Maintenance Mode**	
5	Multiple frames buffering for transmit and receive data	1	Power On Self Test (POST)
6	Status registers for pending interrupt, Status registers for pending interrupt, Pending buffers, buffer status, RAU status, time out, error frame.	2	Memory Test
7	Hardware handling of all RS485 communication and related protocol.	3	Loopback Test

8	FPGA based implementation	4	Built In Test (BIT)
9	I/O interface: 32 bit/ 33 MHz PCI interface Compatible.	5	Maintenance Built In Test (MBIT)
10	Compatible with VITA 20-200X (Conduction Cooled).	6	Discrete I/Os read/write.
11	Configuration to select board for DACENT or RAU	**Configuration Mode**	
12	Modes of Operation: a. Configuration Mode. b. OFP (Operational Flight Program) Mode. c. Maintenance Mode with loop back.	1	Downloading configuration data and general purpose data to IRDSM in RAU
13	Scan rate Selection in OFP mode in Sync with word clock or Frame clock.	2	Collect configuration checksum from IRDSM in RAU
14	Complete functionality to be implemented in FPGA except RS485 drivers.	**Online Mode**	
15	Power: <3 Watts.	1	OFP command generation and data scanning with frame interval
16	MTBF : > 5000 Hours	2	OFP command generation and data scanning with word interval
Software Specifications		3	OBS command generation and data scanning
1	Device Drivers for VxWorks RTOS	4	OFP-mode and OBS-mode command generation and data scanning
2	Device Drivers support for a). Real time telemetry, b). On-board storage, c). Configurability for DACENT or RAU.	**Functional Requirements-IRDSM-R : Test and Maintenance Mode**	
Environmental Specifications		1	Power On Self Test (POST)
1	Operating Temperature : -40^{o} to +85^{o} C	2	Memory and loop back test
2	Altitude : 65,000 feet	3	Built In Test (BIT)
3	Humidity : 0 to 95% Non–condensing	4	Maintenance Built In Test (MBIT)
4	Vibration : 0.04 g^2 /Hz(20-2000Hz)	5	Collect BIT and MBIT results from IRDSM-R
5	Shock : 40G (as per Mil-STD-810E)	6	Discrete I/Os read/write
6	Conduction Cooling : as per IEEE1101.2	**Configuration Mode**	
7	EMI/EMC : as per Mil-Std-461D	**Online Mode**	

D. Hardware Design

Design of IRDSM was a great challenge towards addressing all technical specifications, harsh environmental requirements, and stringent functional requirements. Design concept adopted is based on minimum chip count with open system architecture (PMC) interface to use across sub-systems or developments. PMC (PCI Mezzanine Connector) interface based design which provides high bandwidth for large data exchange/transfer. Soft core for PMC is developed and ported to FPGA to address non availability of PCI chip set components in required temperature range (-40^{o}C to 125^{o}C). The component building blocks of the design are FPGA, SRAM, PMC interface connectors, LDO regulator, Oscillators, RS485 drivers, Octal buffers, Relays, etc,. Complete functionality has been implemented using Actel FPGA APA600PQ208M device. This is a flash based CMOS FPGA powered by 3.3V supply. The core voltage is 2.5V. It has a maximum of 600,000 system gates, 21,504 logic tile cells and 126K bits of RAM. Its operational clock is 33 MHz (PCI CLK). The FPGA is programmed via JTAG port.

Interface Details of FPGA: IRDSM block schematic is given in Fig.2, and following are interface design details of FPGA

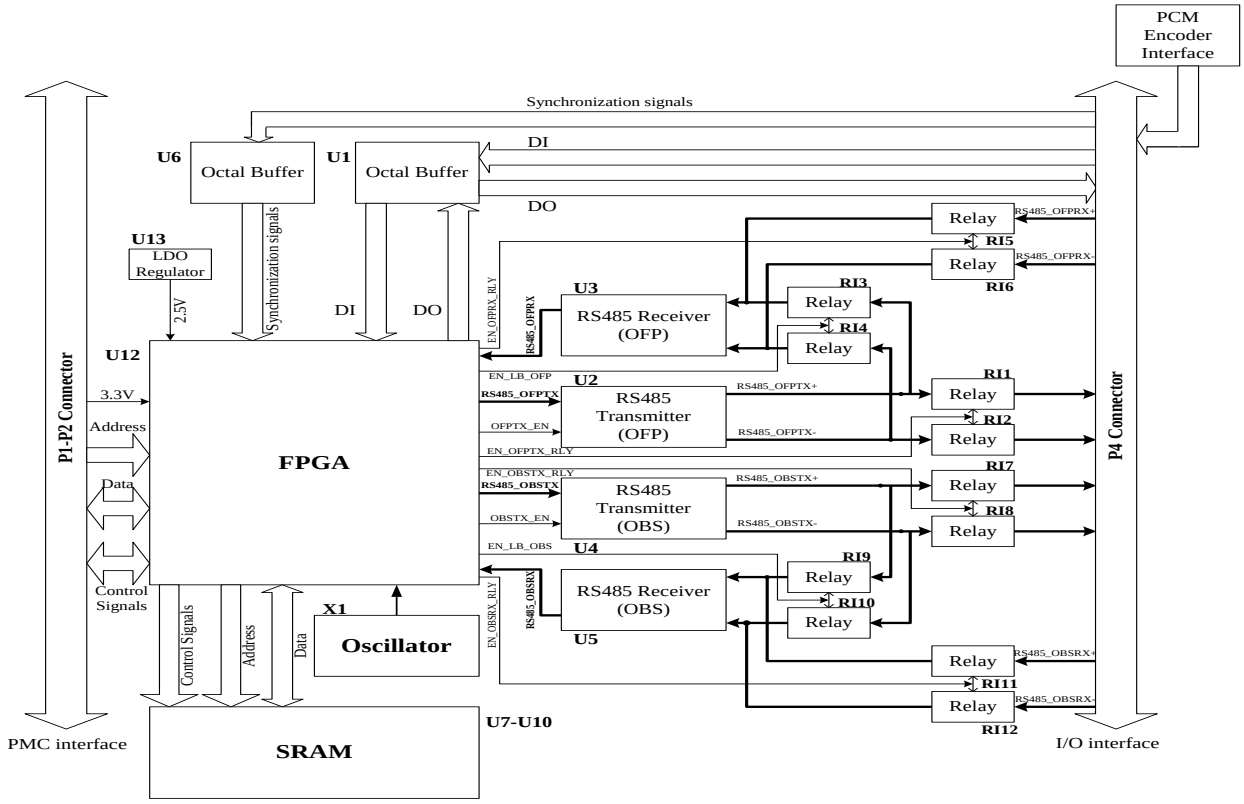

Fig. 2 IRDSM Architecture block schematic

1) The FPGA is interfaced with the PMC bus (PMC connectors P1 and P2). The input supply of 3.3V is supplied from the PMC bus. This interface includes the address lines, data lines and the PCI control signals. The PCI bridge is implemented in the FPGA firmware.
2) The FPGA core voltage (2.5V) is supplied by the LDO regulator LP3874ES-2.5.
3) The address lines, data lines, chip select, write enable and output enable signals of the SRAM (four) are interfaced with the user I/Os of the FPGA.
4) The FPGA is fed with an external clock of 39.3216 MHz using which the necessary baud rates for data communication are generated by the firmware.
5) The FPGA is interfaced with two transmit/receive drivers. The FPGA provides the driver enable signal and the data (OFP and OBS) to the transmit/receive drivers.
6) The FPGA provides the enable signals to the twelve relays using which the data communication path can be controlled for online or loopback.
7) The FPGA is interfaced with two octal buffers to read synchronization signals, read discrete inputs and write discrete outputs.

The FPGA interface details are provided in Fig. 3.

The IRDSM needs onboard memory to store Test/Maintenance mode results, configuration/general purpose data and command/data during online mode. The design has four Static Random Access Memory (SRAM) K6X4008T1F-VF70 with each SRAM organized as 512Kx8 bit. Therefore the onboard memory is 2Mb. The SRAM is interfaced with FPGA for write/read operation. The interface has 19 unidirectional address lines, 8 bidirectional data lines, active low chip enable, active low write enable and active low output enable signals.

Detailed design analysis like power budget analysis, thermal analysis, derating analysis, MTBF calculations, etc, has been carried out for IRDSM module. Analysis results meet all technical specifications of IRDSM.

E. IRDSM Software/functional Implementation

IRDSM software has two different modules to support IRDSM-D and IRDSM-R. It is complex software consisting of all functional modules/device driver functions to provide full envisaged functionality. Software development environment is VxWorks. The software architecture is given in Fig. 4.

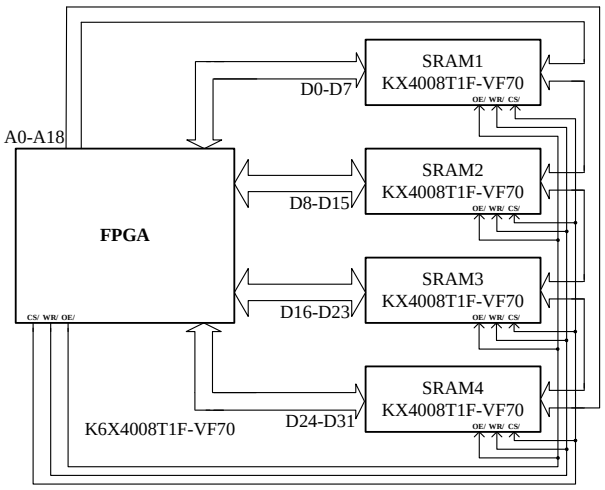

Fig. 3 FPGA and SRAM interface details

F. Software Layers

Software has been built on layered Architecture with the following layers:

1) *Core Hardware Layer (CHL):* This comprises the device driver components interacting directly with hardware. The components are designed as modular functions with error limit checks and are callable by intermediate layered components. The scope of the device driver is limited to the initialization of devices; transmit/receive data on discrete/communication links and verification of transmission errors.

2) *Utility Services Layer (USL):* This layer provides a link between the hardware and the application.

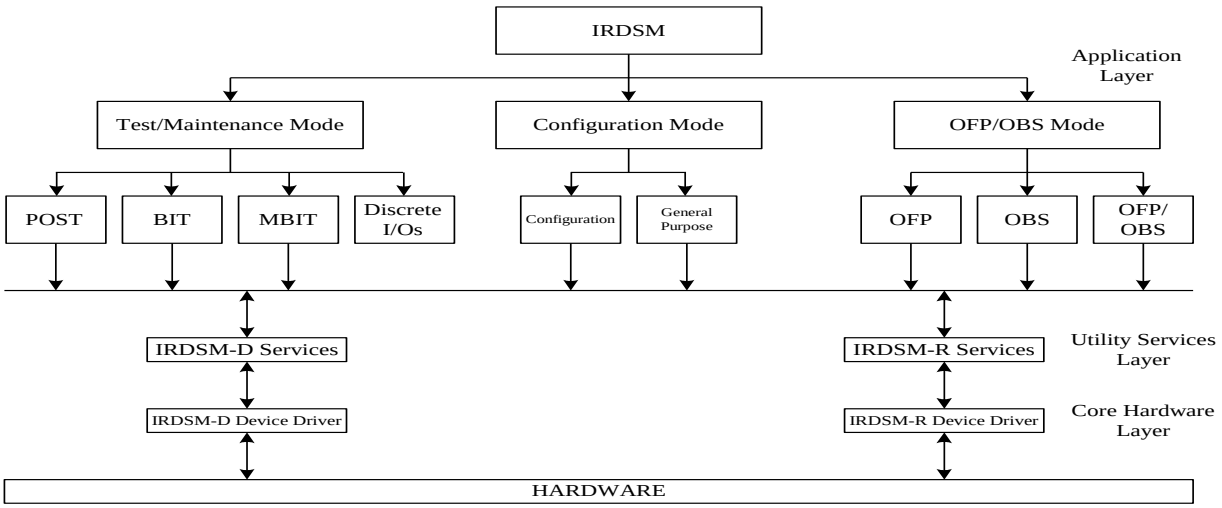

Fig. 4 Software Architecture of IRDSM

The layer comprises the utility components via IRDSM-D and IRDSM-R services. It calls the Device Driver Routines and gives results to Application User Interface.

3) *Application layer (APL):* This is the layer where system application software interacts with Utility Services Layer The main Computer Software Configuration Item-CSCI (IRDSM) consists of the following modules: 1. IRDSM-DACENT (IRDSM-D) and 2. IRDSM-RAU (IRDSM-R).

G. IRDSM Top level CSC's(Computer Software Component)

IRDSM-DACENT Top level CSC's are given in TABLE I.

TABLE II. IRDSM-D FUNCTIONAL FLOW

SI. No	Function Name	Description	SI. No	Function Name	Description
1	test_DacentPostResult	This function is to read the POST results from the POST result location (0x104h) of the DACENT memory.	11	test_ResCltCmdBITTest	This function is to send command to RAU to collect the BIT results.
2	test_MemoryTest	This function is to perform memory test from 0x100 to 0x1fffff location.	12	test_ResCltCmdMBITTest	This function is to send command to RAU to collect the MBIT results.
3	test_DacRelayInit	This function is to select either online or loop back relays.	13	test_ConfigurationDownload	This function is to download configuration data to RAUs.
4	test_DacRS485LoopBackTest	This function is to perform loop back test on both OFP and OBS channel.	14	test_GeneralPurCmd	This function is to download general purpose data to RAUs.
5	test_POSTTest	This function is to perform Power On Self Test for the module.	15	test_ResCltCmdChkSumTest	This function is to send command to collect check sum.
6	test_BITTest	This function is to perform Built In Test for the module.	16	test_OFPDacentTest	This function is to send the OFP frame interval command and receive the OFP data from RAUs.
7	test_MBITTest	This function is to perform Maintenance Built In Test for the module.	17	test_DacentWordIntervel	This function is to send the OFP word interval command and receive the OFP data from RAUs.
8	test_InitCmdBITTest	This function is to send BIT initiate command to particular RAU.	18	test_OBSDacentTest	This function is to send the OBS command and receive the OBS data from RAUs.
9	test_InitCmdMBITTest	This function is to send MBIT initiate command to particular RAU.	19	test_OBSOFPDacentTest	This function is to send the OFP and OBS command and receive the OFP and OBS data from RAUs.
10	test_ResCltCmdPOSTTest	This function is to send command to RAU to collect the POST results.	20	test_DiscreteInputsandOutputs	This function is to read and write the discrete I/Os

Many more functions have been implemented to meet all functional requirements at IRDSM-D and IRDSM-R.

H. Functional Flow of IRDSM-D

The typical functional flow for IRDSM-D from power on to power off with different states of operation is given in

Fig. 5.

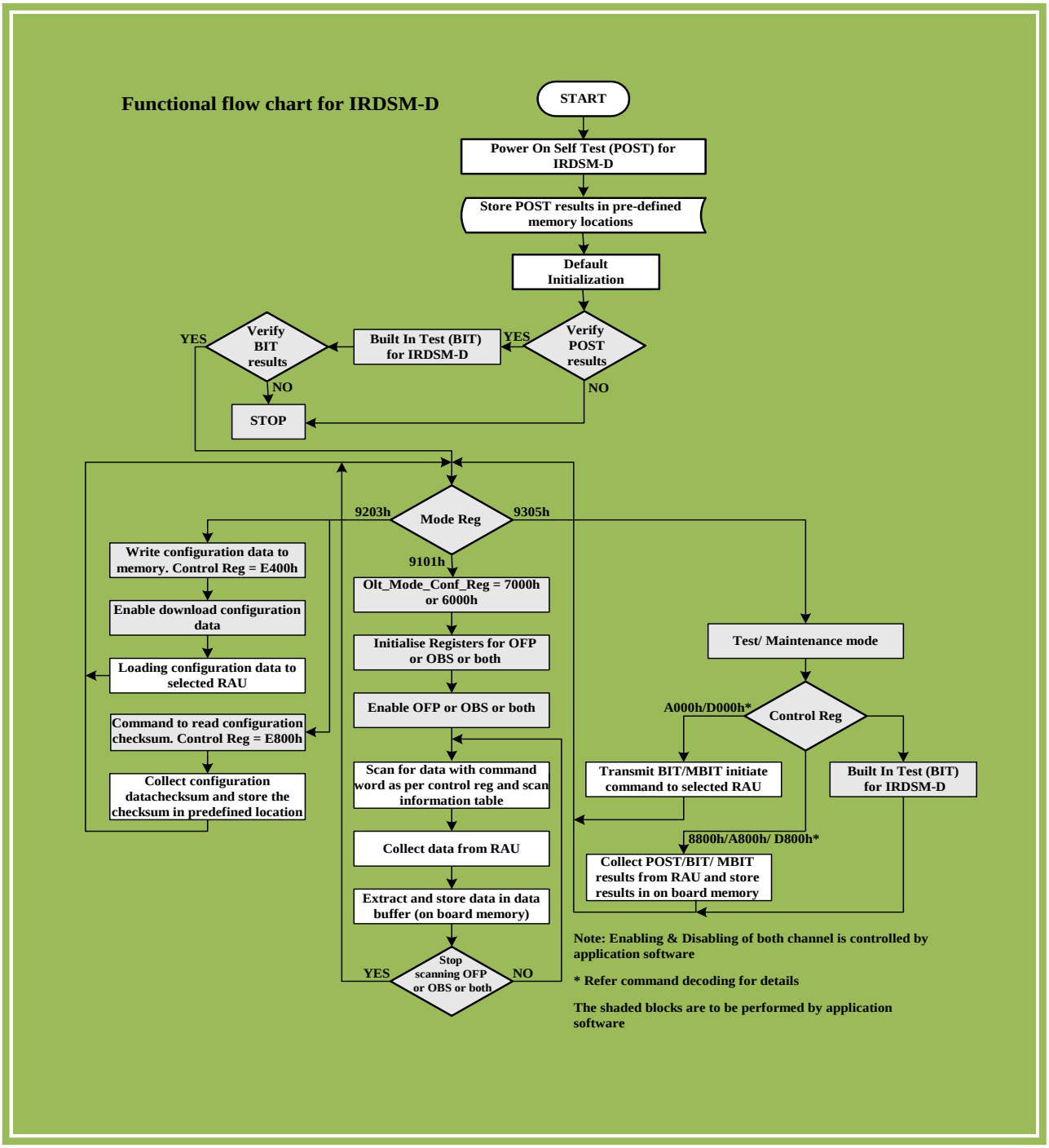

Fig. 5 IRDSM-D functional flow

IV DEVELOPMENT AND TEST ENVIRONMENT

The testing and evaluating IRDSM for its functionality and other requirements is an intensive and involved task. FTI system test facility is used for testing the system with and without IRDSM. Large number of test cases was used for testing IRDSM full functionality. The IRDSM Module with PMC interface is shown in fig 6A. The development environment with DACENT and RAUs.

DACENT System configured with VME bus based PowerPC control and IO modules are developed for on-board FTI application and same is shown in Fig 6B. The aircraft subsystems simulation and acquisition facility with required number of IOs for ground testing has been developed and same is shown in fig 6C. The

user interface developed for running test cases, viewing the test results and testing various FTI sub systems for its functionality and performance is shown in Fig 6D.

Fig. 6A IRDSM-D Module with PMC form factor

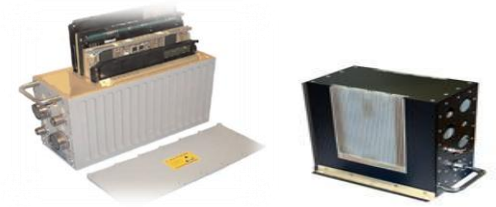

Fig. 6B DACENT with VME Modules and RAU with cPCI

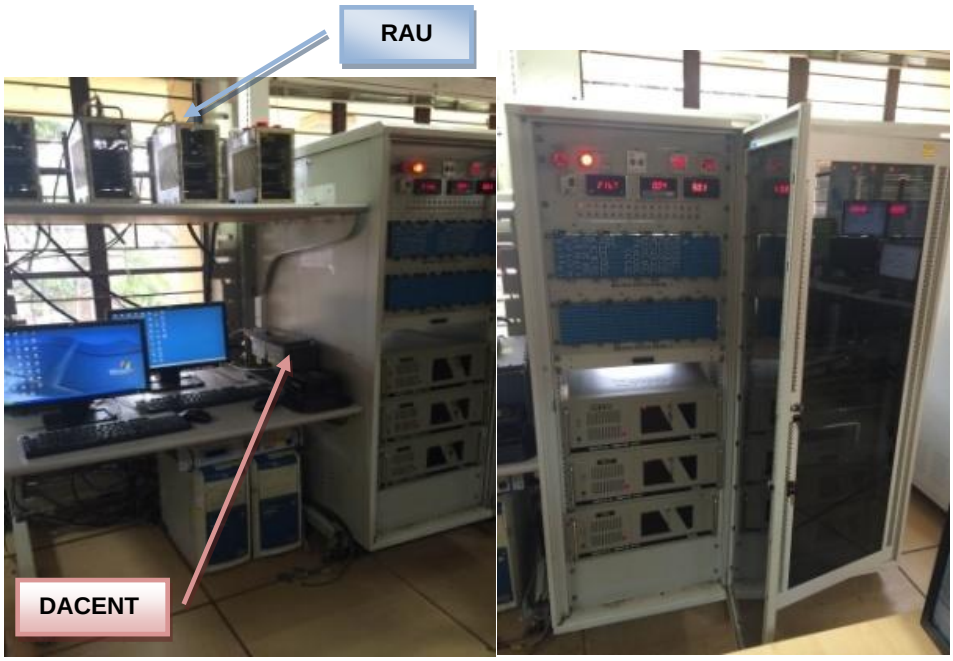

Fig. 6C Aircraft interface simulation and acquisition facility for FTI system with IRDSM.

Fig. 6D User interface set-up for FTI test facility.

V. Architectural Benefits with IRDSM

Designing the system architecture by introducing IRDSM module has enable to handle minor frame pockets for OLT and OBS better resulting improvement in overall system though put. With this timing constraints are met without compromising on performance like data integrity etc. Its autonomous functioning during the operation has enabled to collect the data periodically for every minor frame from RAUs without overloading the processor/ missing the minor frame data, etc. It also enabled to collect large data periodically through 2nd RS485 bus (ref. Fig 1) for on-board storage. IRDSM off loaded the burden of interacting and collecting data from RAUs so that controller module can concentrate on real time processing for telemetry and storage.

VI. Performance figures and benefits

System has been configured without and with IRDSM and performance was evaluated with extensive testing. The following are the performance figures with and without IRDSM in the system.

TABLE III PERFORMANCE BENEFITS

Sl No	**Area**	**Improvement**	
		Without	**With**
1	Data Handling	64Kbytes	>128 Kbytes
2	Timing for full load	Limitation	Comfortably could meet
3	Fault Isolation	60%	95%
4	Computation time	95% loaded	60% loaded
5	Remote Acquisition	Load on CPU	Fully Autonomous
6	Data integrity	Low	Very High
7	Event of RS485 drivers failures	Full PowerPC controller module replacement	Only RS485 module replacement

CONCLUSIONS

OSA based distributed FTI system where real time constraints are large has been realized and tested with and without IRDSM module. It was found that, there is a significant performance improvement of the system with IRDSM. These architectural improvements enhance the system health monitoring with continuous BIT.

It also resulted in increased safety of the platform as data integrity with IRDSM is relatively high for the on-board flight test instrumentation system used for developmental flights of high performance fighter aircraft.

This kind of architectural adaptation can be used for similar kind of applications where system level timing constraints or processor computational power is in demand.

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