INTERNATIONAL JOURNAL OF ADVANCE RESEARCH, IDEAS AND INNOVATIONS IN TECHNOLOGY

ISSN: 2454-132X
Impact Factor: 6.078
(Volume 11, Issue 1 - V11I1-1488)
Available online at: https://www.ijariit.com

Differentiating Fault Current from Leakage Current during IC Testing

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ABSTRACT

Differentiating Fault Current from Leakage Current During IC Testing As integrated circuit technology advances, the intricacies related to fault identification and leakage current evaluation have increased markedly. Although conventional I_DDQ (quiescent supply current) testing protocols exhibit effectiveness in detecting major defects, they often struggle to distinguish between typical leakage currents and those reflective of genuine faults, thereby prolonging testing durations. Consequently, current sensors typically initiate measurements once transitions are finalized. In this investigation, we utilize a simulation technique to corroborate the effectiveness of an innovative methodology articulated in [1], which can be used to improve the throughput of the current testing process by detecting the faults using AC components of the current, thereby overcoming a constraint of traditional methods.

Keywords: *Current Measurement, Current Sensor, Current Testing, IC Testing, I_DQQ testing, Physical Defects, Test Vectors*

1. INTRODUCTION

The predominant benefit of Complementary Metal-Oxide-Semiconductor (CMOS) digital circuits resides in their minimal power consumption, which results from the deployment of p-channel and n-channel MOSFET pairs. Under standard operational parameters, power consumption remains negligible, as current flow transpires primarily during transition events. Nevertheless, faulty circuits consistently affect the anticipated quiescent drain current (I_{DDQ}), highlighting the importance of conducting I_{DDQ}testing as a robust methodology for evaluating the integrity of digital CMOS integrated circuits.

I_{DDQ} testing not only aids in the detection of physical anomalies but also offers a cost-efficient strategy, thereby solidifying its integration as a fundamental aspect of voltage-based testing frameworks. While I_{DDQ} Q serves as an auxiliary diagnostic mechanism, it cannot replace traditional testing approaches, as it does not assess the operational performance of the circuit [1].

The types of defects detectable through of I_{DDQ}testing include node bridges, gate oxide shorts, leaky pn junctions, punch-through (drain-to-source leakage), and parasitic leaks. These defects may be categorized as either pattern-sensitive or pattern-insensitive [2,3,4]. Notably, of I_{DDQ}test vectors do not require fault propagation to the output, which reduces the complexity and effort associated with traditional voltage testing approaches [5].

In submicron technologies, weak inversion current emerges as a predominant contributor to transistor leakage, exhibiting an exponential dependence on both the transistor threshold voltage (V_TH) and temperature. This leakage current escalates with reductions in V_TH and/or increases in temperature. When the drain-source voltage (V_DS) significantly exceeds the thermal voltage (Φ_t), defined as Φ_t = kT/q (where q represents the electron charge, T denotes temperature, and k is Boltzmann's constant. For submicron technologies, the weak inversion current is the main component of transistor leakage current which depends exponentially on the transistor threshold voltage $V_{TH}$and temperature.

It increases as V_{TH} is reduced and/or the temperature is increased. If (V_{DS}) the voltage drain source voltage is much larger than Φ_t the thermal voltage ($\Phi_t = KT/q$, where q the electron charge, T the temperature and K is the constant of Boltzmann, the inversion current is:

$$I_{DS} = \frac{\mu C_{ox} W}{L_{eff}} (\eta - 1) \Phi_t^2 e^{(V_{GS} - V_{TH})/\eta \Phi_t} \quad (1)$$

Where $\eta = 1 + C_{DEP}/C_{ox}$ with C_{DEP} the channel depletion capacitance, L_{eff} is the effective channel length, , W is the width of

transistor, μ is mobility of the carrier and C_{ox} is the capacitance of gate oxide and [6],[7].

For the submicron technologies, one of the problems of I_{DQQ} testing is the variations of I_{DQQ} of an order of magnitude because of the significant variation of (L_{eff}) and (V_{TH}). Another problem is the high background current. Both will increase the difficulty to distinguish the defected I_{DQQ} from the process variation. [8]

On the other hand, the determination of the threshold for pass/fail reference necessitates execution prior to the implementation of the I_{DQQ} test measurement. The sampling of several integrated circuits (ICs) represents an acceptable empirical approach to acquire the threshold value. An alternative methodology involves simulation to quantify the defective current [4], [9]. This procedure is pivotal, as it has the potential to result in the rejection of functional devices or the acceptance of non-functional devices

2. I_{DDQ} TESTING TIME REQUIREMENTS

The duration required for precise measurement acquisition is extended. Sufficient temporal allowance must be allocated for the attenuation of transient currents within the power supply and for the adequate drift of floating nodes to initiate current flow. For instance, a floating node exhibiting 1-pF capacitance may require in excess of 50 milliseconds to transition from 3V to 5V. The economic considerations associated with testing impose constraints on the duration permissible for a singular measurement, alongside the quantity of measurements that can be executed; conventionally, 1 second of testing duration is regarded as excessive. Within such constraining conditions, the fault coverage achieved through I_{DQQ} testing with respect to specific open faults can be significantly diminished. Furthermore, there exist numerous open faults, such as those associated with power supply or drain contact interruptions, which may remain completely undetected. [16],[17],[18].

The I_{DQQ} (comprising its transient element) is ascertained at the conclusion of the specified clock cycle, and it is required to be of lesser magnitude than the minimum anomalous current induced by the existing defect. Consequently, the establishment of an accurate threshold constitutes a critical procedure for identifying the defects through conventional I_{DQQ} methodologies. Numerous factors generate substantial noise within the current testing protocol, which culminates in restricted attainable resolution and a relatively low operational frequency. A multitude of investigative studies scrutinizes techniques aimed at enhancing the discrimination between defective and non-defective I_{DQQ} currents. The reduction of testing temperature, the application of back-biasing strategies, and the segmentation of power source circuits exemplify well-documented methodologies for diminishing the quiescent current. [10], [11], [12], [13], [14], [15].

In this study, researchers aim to delineate the defective current from the quiescent current. A novel fault detection methodology is introduced, derived from the approach documented in reference [1]. This methodology provides a unique benefit: the defective current, which is perceived at the ground of the Circuit Under Test (CUT), exhibits an alternating current (AC) component that remains unobservable in the absence of anomalies. This outcome is accomplished by superimposing a minor sinusoidal signal onto the power supply, which does not perturb the steady-state ground current. Nonetheless, in circumstances where a defect establishes a conductive pathway between the voltage supply (VDD) and ground.

CONTRIBUTION

Verification of the advantages of the new current testing approach introduced in [1]

Using simulation we verified the advantages of the novel approach of I_{DDQ} testing discussed in [1] including the ability to differentiate the fault current from leakage current, thought minimizing the time needed for testing.

FAULT CURRENT SIMULATION

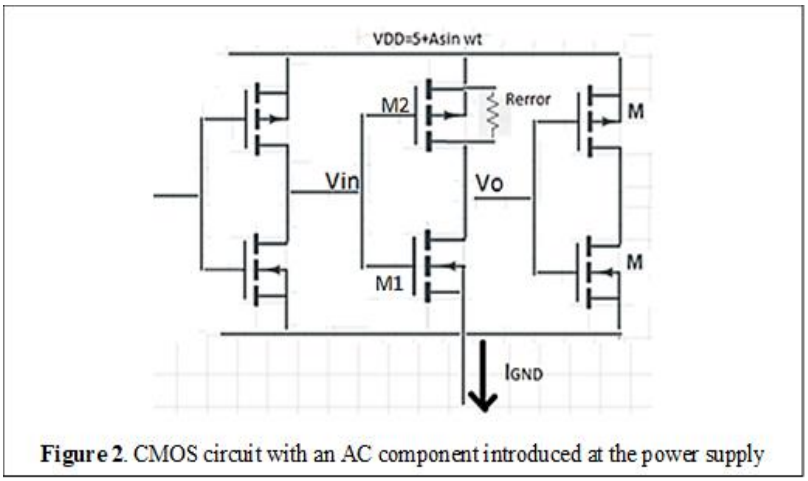

Figure 2. CMOS circuit with an AC component introduced at the power supply

3.1 Example of defective circuit with a short

To illustrate the basic concepts of our approach, we consider the middle inverter of Figure. 2.
An AC with frequency ω is assumed to be superimposed on the power supply VDD.
We assume that the input signal (Vin) of the inverter is coming from similar stage in the circuit and its output (Vo) drives a similar inverter.
We model the fault by a resistance Rerror. For example the source-drain fault in M2 is connected by Rerror as shown in Figure. 2 as an example of the possible faults of the inverter.

For the shown circuit, we have 4 cases to consider:
Case 1. This stage has no fault and its input is low.
Case 2. This stage has no fault and its input is high.
Case 3. This stage has a fault and its input is low.
Case 4. This stage has a fault and its input is high.

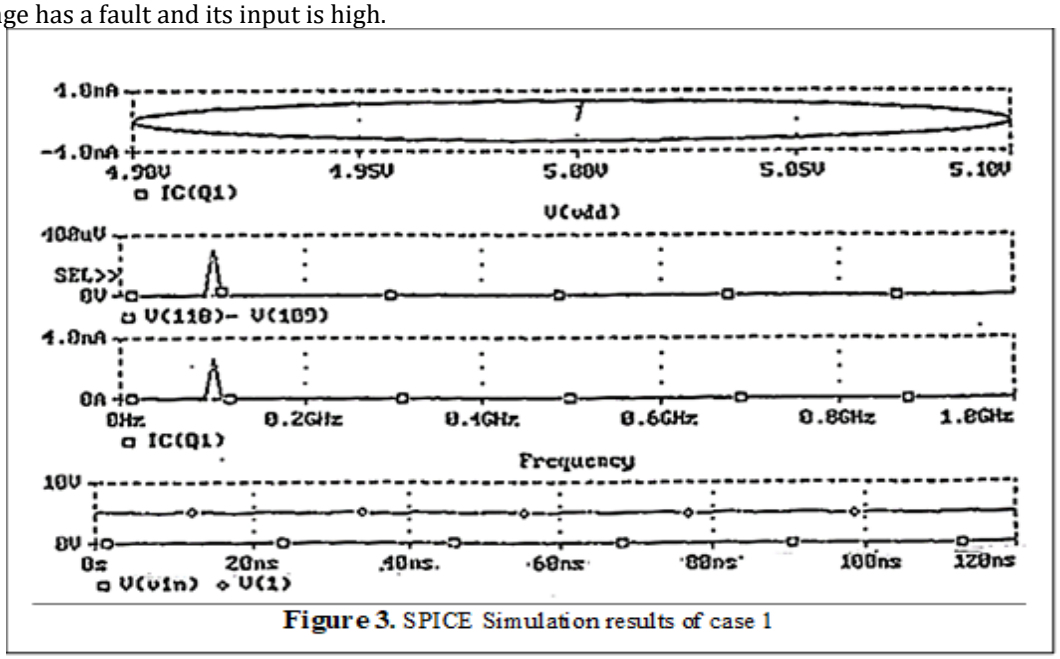

Figure 3. SPICE Simulation results of case 1

3.1.1 Case 1

From the simulation results of case 1 shown in Figure 3, we observe that:

- The figure illustrates that I_{GND} has only a component at frequency ω
- I_{GND} has a 90 degree phase shift with AC signal introduced at VDD
- There is no dc part of the output

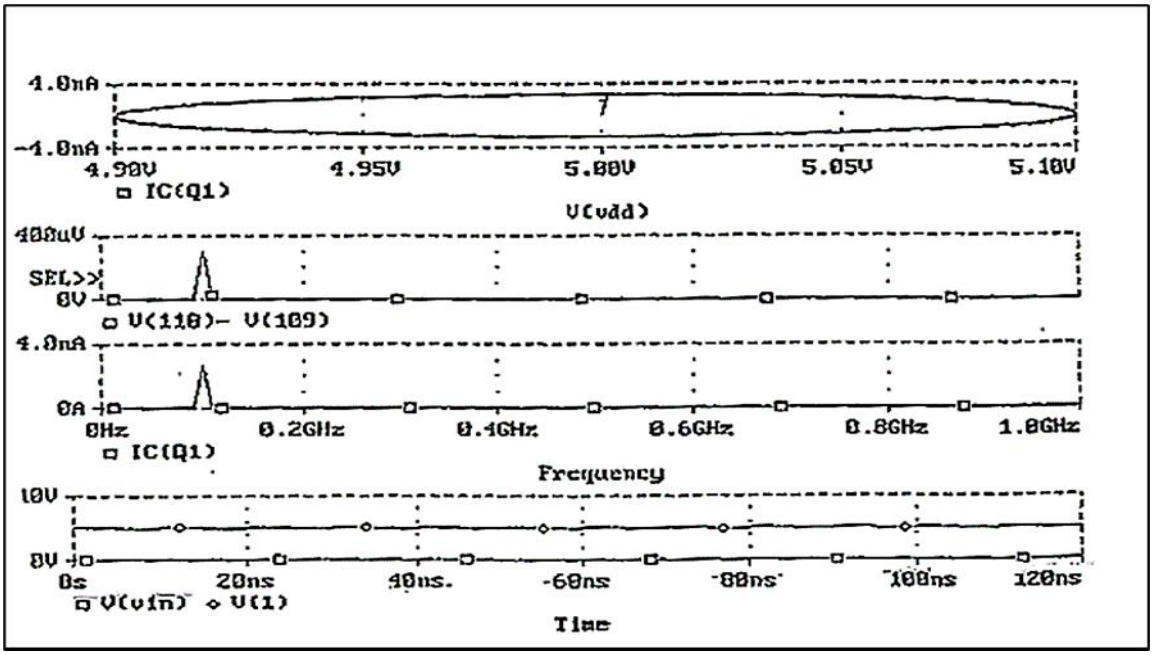

Figure 4. SPICE Simulation results of case 2

3.1.2 Case 2

From the simulation results of case 2 shown in Figure 4, we observe that:

- I_{GND} has only a component at frequency ω
- I_{GND} has a 90 degree phase shift with AC signal introduced at VDD
- There is no dc part of the output

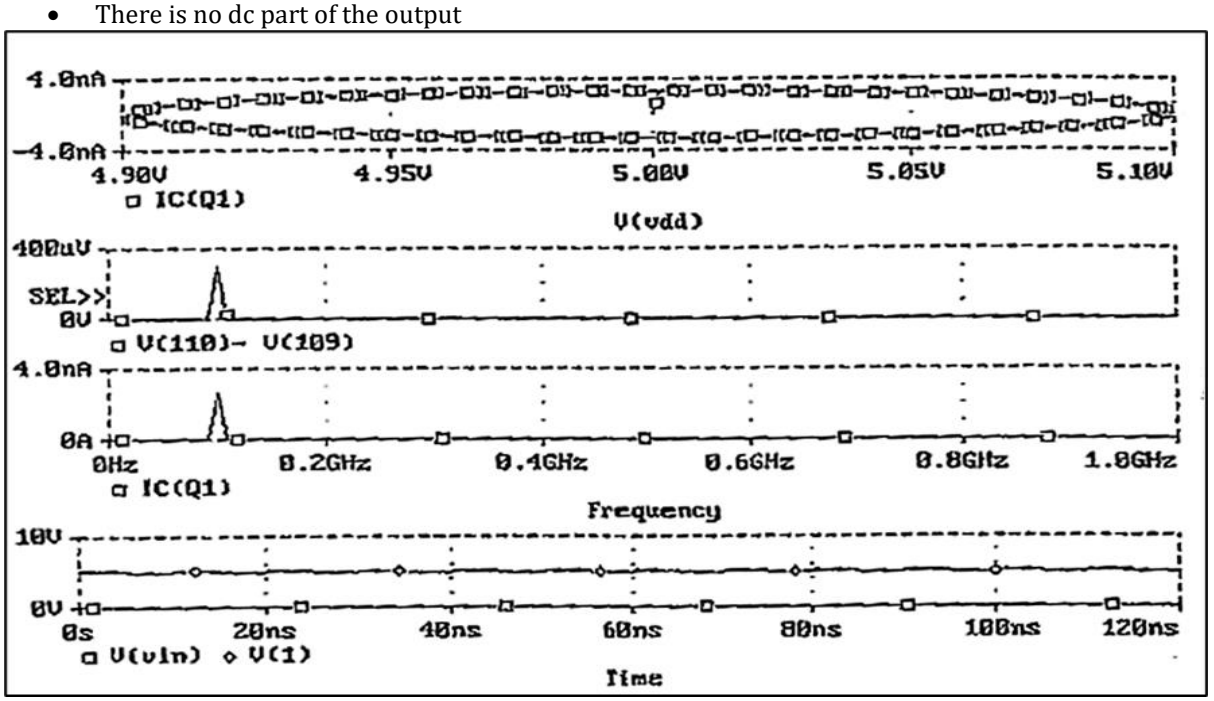

Figure 5. SPICE Simulation results of case 3

3.1.3 Case3

From the simulation results shown in Figure 5. we conclude that:

- The figure illustrates that I_{GND} has only a component at frequency ω with small amplitude (nA)
- I_{GND} has a 90 degree phase shift with AC signal introduced at VDD
- There is no dc part of the output

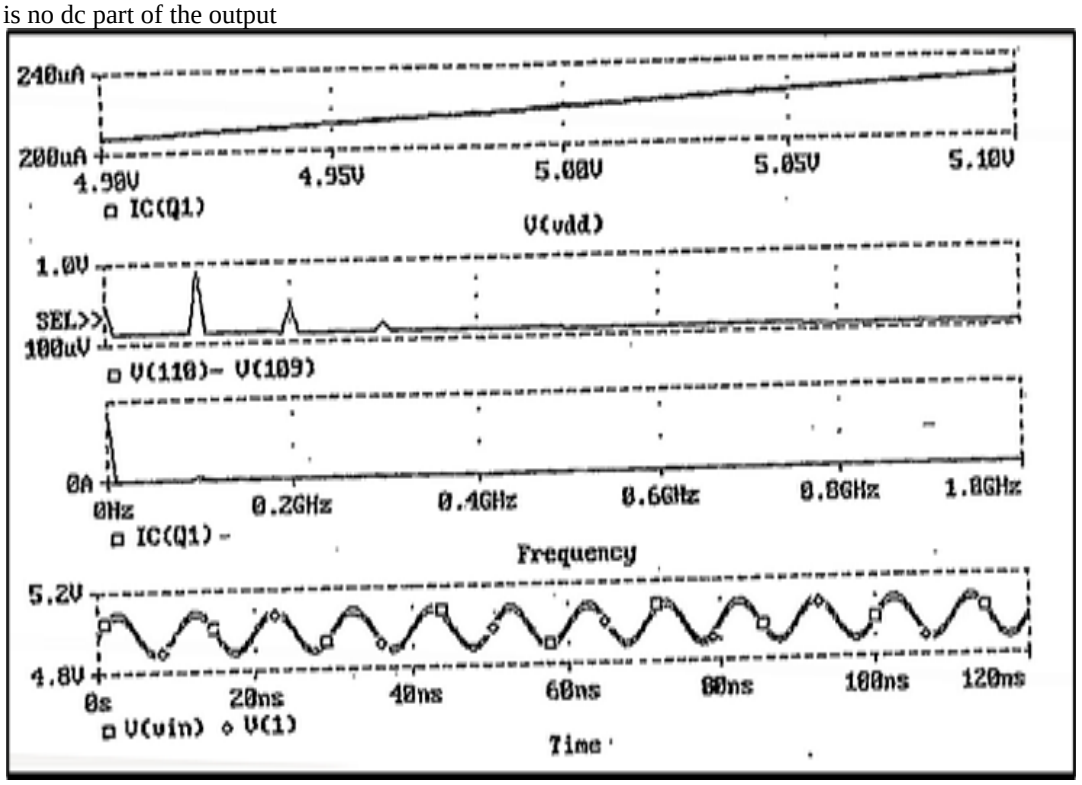

Figure 6. SPICE Simulation of case 4

3.1.4 Case4

From the simulation results of case 4 we observe that:

- I_{GND} has three components at frequencies ω, 2ω and 3ω.
- There is dc part of I_{GND} which agrees with the expected results.

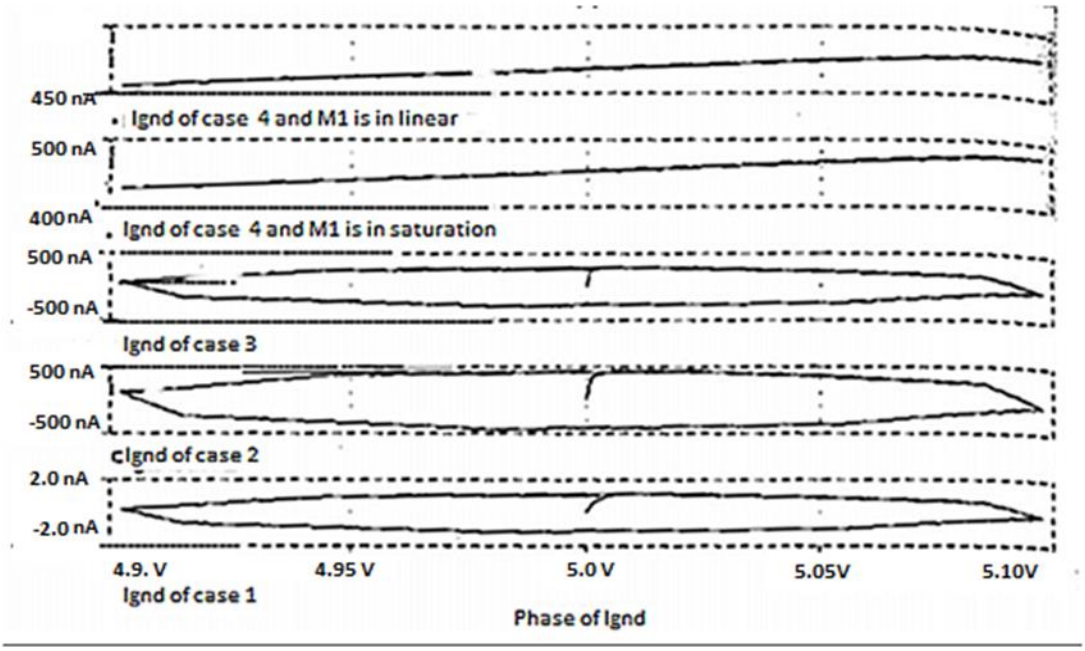

Figure 7. Simulation results of current phase

CONCLUSION

From simulation results we found that we can detect the error case by detecting one of the following:
The dc part of I_{GND} which is the traditional method.
The amplitude I_{GND} component at frequency of the AC part introduced at the power supply.
The amplitude of I_{GND} at higher harmonics (ϕ)
A combination of the above methods.
The methods based on 2, 3 and 4 can run on-line at high speed which is an advantage over the traditional method (dc part of I_{GND})
This advantage enables us to reduce the measuring delay time to minimum.
The new approach can be applied to either off-chip or built in current testing.
For off-chip current testing it overcomes many problems which result in limited achievable resolution

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